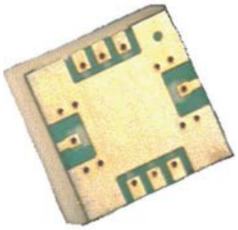
AMMP-6522

7 to 20 GHz GaAs MMIC LNA/IRM Receiver in SMT Package

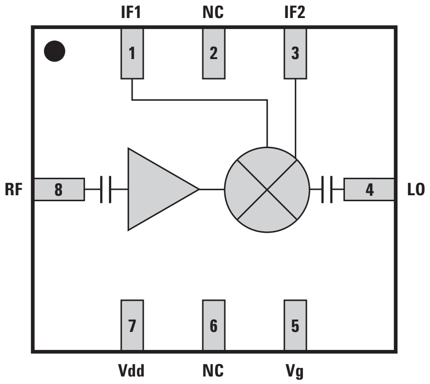
Data Sheet



Description

Avago's AMMP-6522 is an easy-to-use broadband integrated receiver in a surface mount package. The MMIC includes a 3-stage LNA to provide gain amplification and a gate-pumped image-reject mixer for frequency translation. The overall receiver performs Single Side Band down-conversion in the 7 to 20 GHz RF signal range. The LO and RF are matched to 50 Ω. The IF output is provided in 2-port format where an external 90-degree hybrid can be utilized for full image rejection. The LNA requires a 4 V, 75 mA power supply, where the mixer bias is a simple -1 V, 0.1 mA. The MMIC is fabricated using PHEMT technology. The surface mount package allows elimination of "chip & wire" assembly for lower cost. This MMIC is a cost effective alternative to multi-chip solution that have higher loss and complex assembly.

Pin Connections (Top View)



TOP VIEW

PACKAGE BASE: GND

PIN	FUNCTION
1	IF1
2	NC
3	IF2
4	LO
5	Vg
6	NC
7	Vdd
8	RF

Features

- 5x5 mm Surface Mount Package
- Integrated Low Noise Amplifier
- Integrated Image Reject Mixer
- 50 Ω Input and Output Match
- Single Supply Bias Pin

Specifications Vd = 4.0 V (75 mA), Vg = -1.0 V (0.1 mA)

- RF frequency: 7 to 20 GHz
- IF frequency: DC to 3.5 GHz
- Conversion Gain (RF/IF): 13 dB
- Input Intercept Point: -4 dBm
- Image Suppression: 15 dB
- Total Noise Figure: 2.4 dB

Application

- Microwave radio systems
- Satellite VSAT, DBS Up/Down Link
- LMDS & Pt-Pt mmW Long Haul
- Broadband Wireless Access (including 802.16 and 802.20 WiMax)
- WLL and MMDS loops

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A)
ESD Human Body Model (Class 1A)
Refer to Avago Technologies Application Note A004R: *Electrostatic Discharge, Damage and Control.*

Notes:
1. This MMIC uses depletion mode pHEMT devices.
2. Negative supply is used for mixer bias.

Absolute Maximum Ratings[1]

Symbol	Parameter and Test Condition	Unit	Max.
Vdd	Drain to Ground Voltage	V	5.5
Vg	Gate to Ground Voltage	V	+0.8
Idd	Drain Current	mA	100
Ig	Gate Current	mA	1
Pin	RF CW Input Power Max	dBm	10
Tch	Max channel temperature	C	+150
Tstg	Storage temperature	C	-65 +150
Tmax	Maximum Assembly Temp	C	260 for 20s

Note:

1. Operation in excess of any of these conditions may result in permanent damage to this device. The absolute maximum ratings for Vdd, Vg, Idd, Ig, and Pin were determined at an ambient temperature of 25°C unless noted otherwise.

DC Specifications/ Physical Properties[2]

Symbol	Parameter and Test Condition	Unit	Min.	Typ.	Max.
Vdd	Drain Supply Voltage	V	3	4	5
Idd	Drain Supply Current (V_d = 4.0 V)	mA		75	95
Vg	Gate Supply Voltage (I_g = 0.1 mA)	V	-1.2	-1.0	-0.8
θjc	Thermal Resistance(3)	C/W		27	

2. Ambient operational temperature T_A = 25°C unless noted.
3. Channel-to-backside Thermal Resistance ($T_{channel}$ = 34°C) as measured using infrared microscopy. Thermal Resistance at backside temp. (T_b) = 25°C calculated from measured data.

Operating Conditions

Symbol	Parameter and Test Condition	Units	Min.	Typ.	Max.
RFfreq	RF Frequency	GHz	7		20
LOfreq	LO Frequency	GHz	5		22
IFfreq	IF Frequency	GHz	DC[8]		3.5
LO	LO Drive Power	dBm	+10	+15	+22

RF Specifications[4,5,6]

T_A = 25°C, Z_0 = 50 Ω, V_{dd} = 4.0 V, V_g = -1 V, LO = +15 dBm, IF = 2 GHz

Symbol	Parameter	Freq (GHz)	Units	Min	Typ	Max
NF	Noise Figure	RF=8GHz, LO=10GHz	dB		2.6	3.3
		RF=18GHz, LO=20GHz			3	3.3
CG	Conversion Gain	RF=8GHz, LO=10GHz	dB	12	13	
		RF=18GHz, LO=20GHz		12	14	
IIP3	Input Third Order Intercept	RF=8GHz, LO=10GHz	dBm	-8	-6	
		RF=18GHz, LO=20GHz		-5	-0.4	
Sup	Image Rejection	RF=8GHz, LO=10GHz	dB	15	29	
		RF=18GHz, LO=20GHz		15	30	

2. Use IF = DC with caution. Please see "Biasing and Operation" for more details.

All tested parameters are guaranteed with the following measurement accuracy:

RF=8GHz:	±0.6dB for Conversion Gain, ±10dB for IRR, ±0.5dB for NF, ±0.8dBm for IIP3
RF=18GHz:	±1.8dB for Conversion Gain, ±1.6dB for IRR, ±0.6dB for NF, ±1.7dBm for IIP3

AMMP-6522 Typical Performance[1,2]

(T_A = 25°C, Vdd = 4 V, Idd = 75 mA, V_g = -1 V, I_g = 0 mA, Z_{in} = Z_{out} = 50 Ω), IF Freq = 2 GHz, LO Power = +15 dBm unless noted)

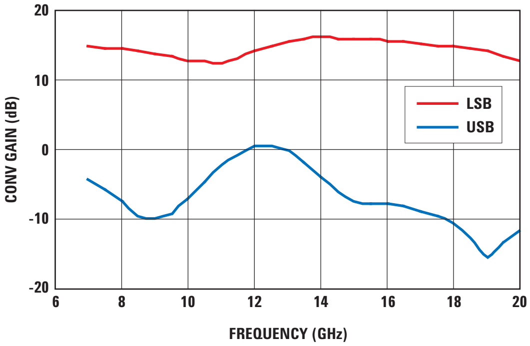


Figure 1. Receiver conversion gain

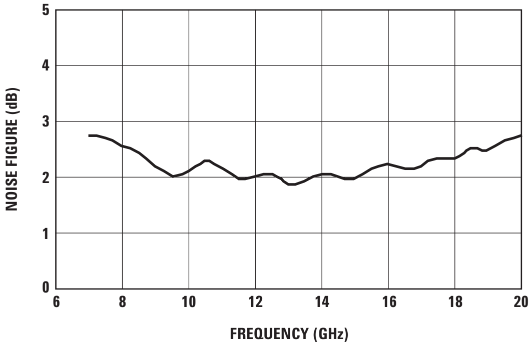


Figure 2. Typical noise figure

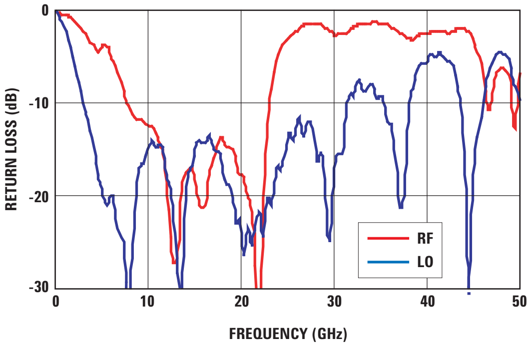


Figure 3. Return loss at RF & LO ports

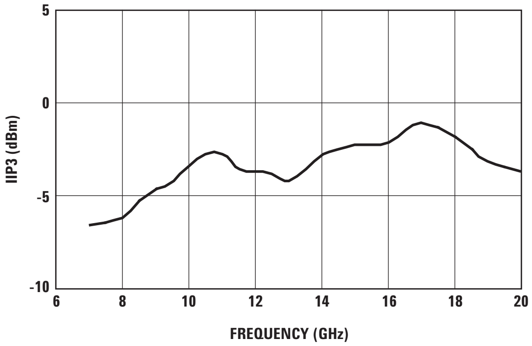


Figure 4. Typical input IP3

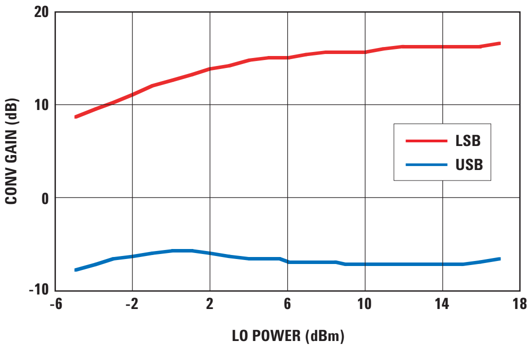


Figure 5. Conv gain vs. LO power (RF = 15 GHz)

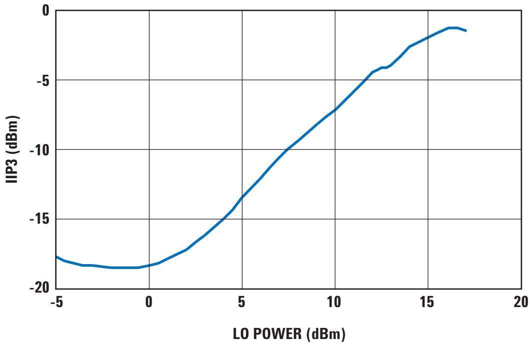


Figure 6. Input IP3 vs. LO power (RF = 15 GHz)

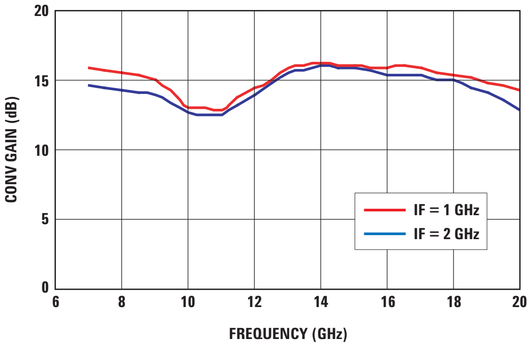


Figure 7. LSB conversion gain at two IF frequencies

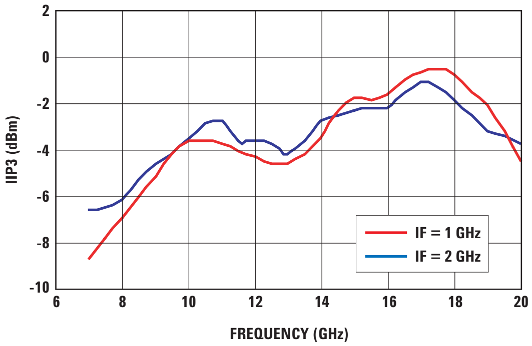


Figure 8. Input IP3 at two IF frequencies

AMMP-6522 Typical Performance (cont.)[1,2]

(T_A = 25°C, Vdd = 4 V, Idd = 75 mA, V_g = -1 V, I_g = 0 mA, Z_{in} = Z_{out} = 50 Ω), IF Freq = 2 GHz, LO Power = +15 dBm unless noted)

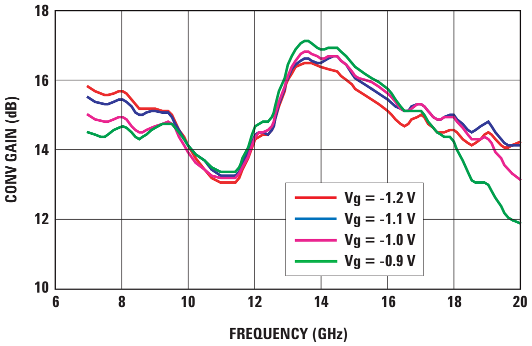


Figure 9. Conversion gain over Vg

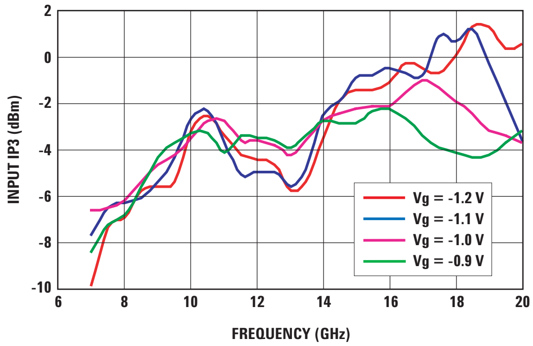


Figure 10. Input IP3 over Vga

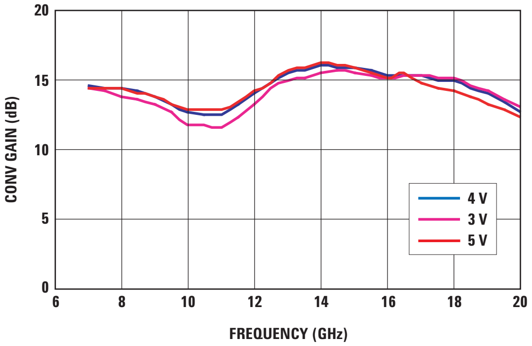


Figure 11. Receiver conversion gain over Vdd

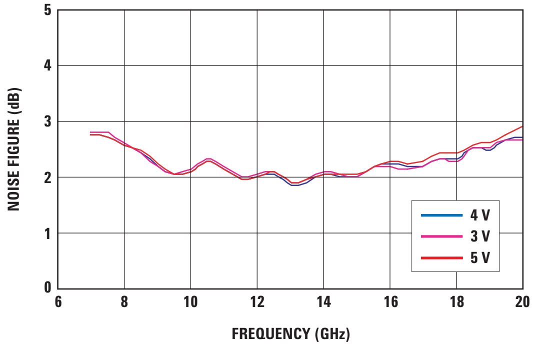


Figure 12. Noise figure over Vdd

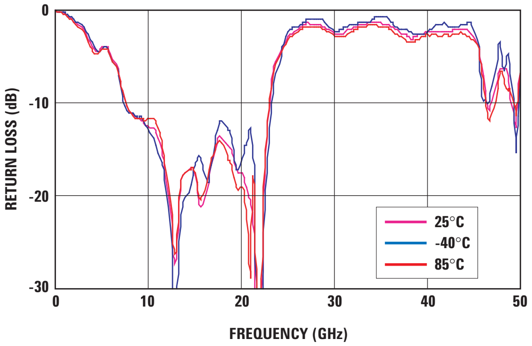


Figure 13. Return loss at RF over temperature

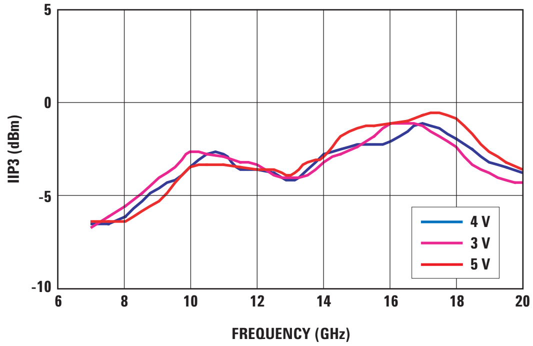


Figure 14. Input IP3 over Vdd

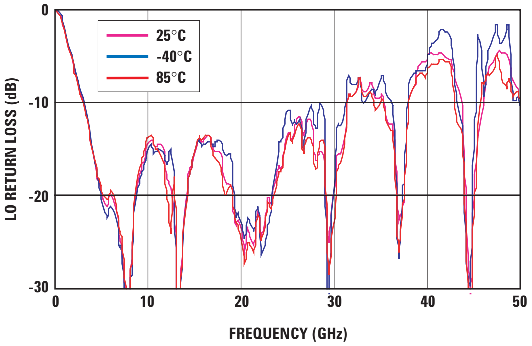


Figure 15. Return loss at LO over temperature

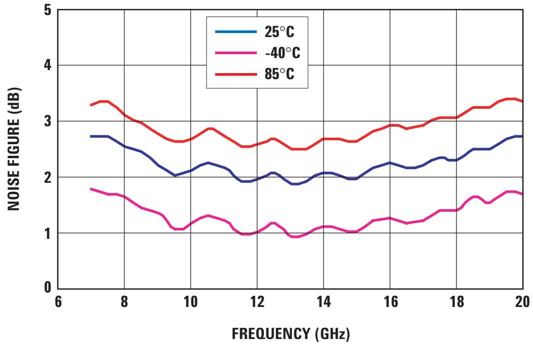


Figure 16. Noise figure over temperature

Notes:

1. S-parameters are measured with R&D Eval Board as shown in Figure 19. Board and connector effects are included in the data.
2. Noise Figure is measured with R&D Eval Board as shown in Figure 19, and with a 3-dB pad at input. Board and connector losses are already de-embeded from the data.

AMMP-6522 Application and Usage

Biasing and Operation

The AMMP-6522 is normally biased with a positive drain supply connected to the VDD pin and a negative gate voltage connected to the Vg pin through bypass capacitors as shown in Figure 17. The recommended drain supply voltage is 4 V and gate bias voltage is -1 V. The corresponding currents are 75 mA and 0.1 mA respectively. The typical required LO level is +15 dBm and it should come from a low noise driver to ensure that overall Front End NF is low.

The image rejection performance is dependent on the selection of the IF quadrature hybrid. The performance of the IF hybrid as well as the phase balance and VSWR of the interface to the AMMP-6522 will affect the overall front end performance.

There is minimal performance degradation if Vdd is lowered to 3 V or raised to 5 V. If lower current is required, then Vdd = 3 V will provide considerably similar RF performance.

The recommended Vg is -1 V. However, depending on the operating frequency, Vg can be changed to achieve better performance for that particular frequency. Please refer to Figures 9 and 10 for how to best select the appropriate Vg for the intended frequency of operation.

Theoretically IF frequencies can be as low as DC. However, when direct conversion is used (IF = DC), a so-called phenomenon DC-offset could occur at the two IF outputs. In most practical applications, IF should be more than a few hundreds kHz to avoid DC-offset correction.

Refer the Absolute Maximum Ratings table for allowed DC and thermal condition.

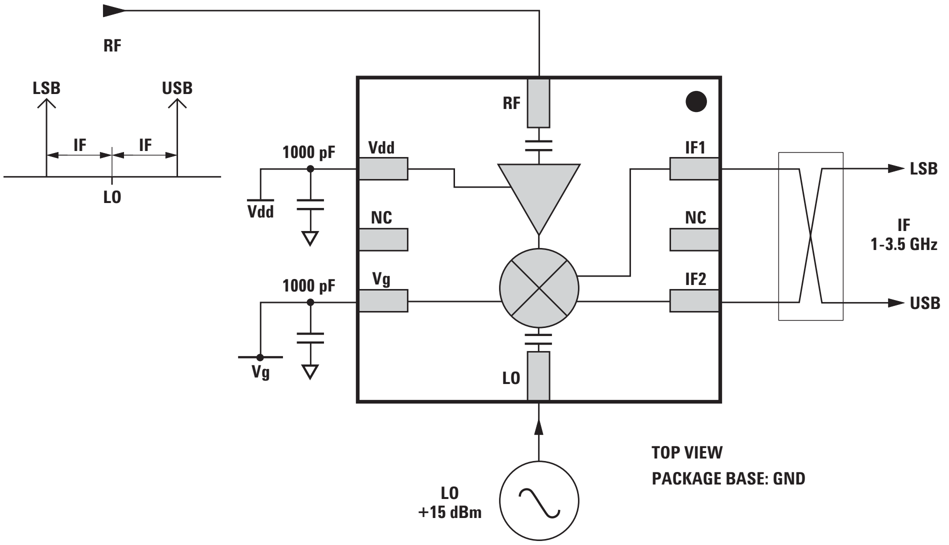


Figure 17. Application of receiver with IF Balun

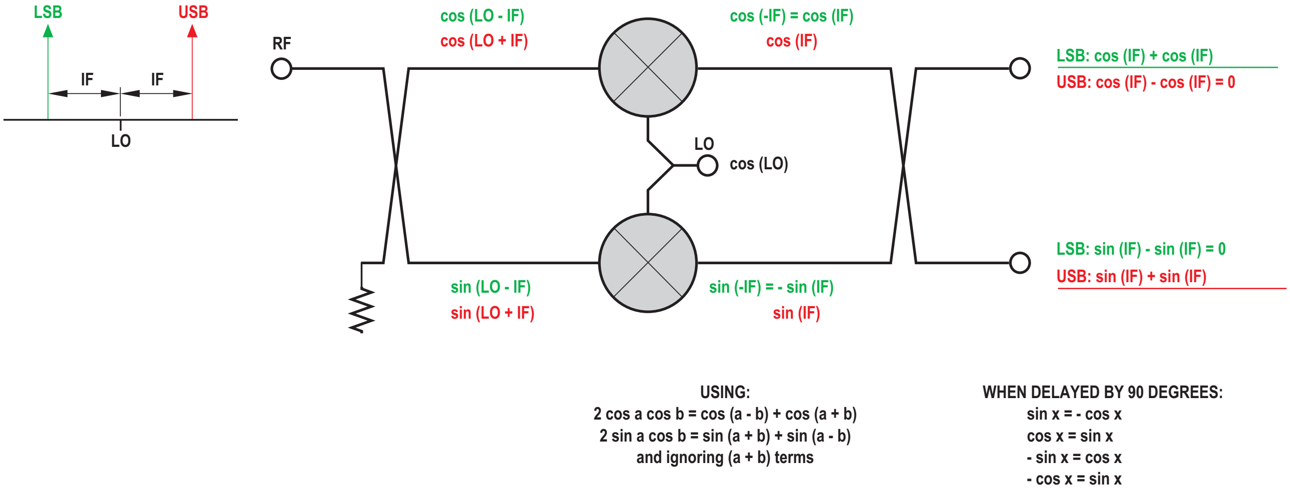


Figure 18. Theory of harmonic rejection

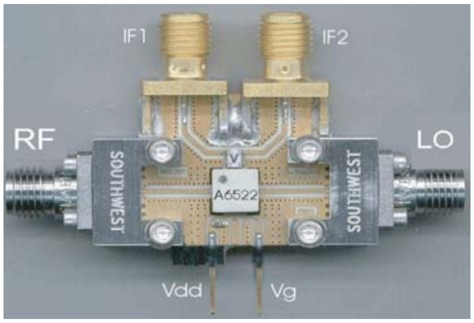


Figure 19. Evaluation/test board

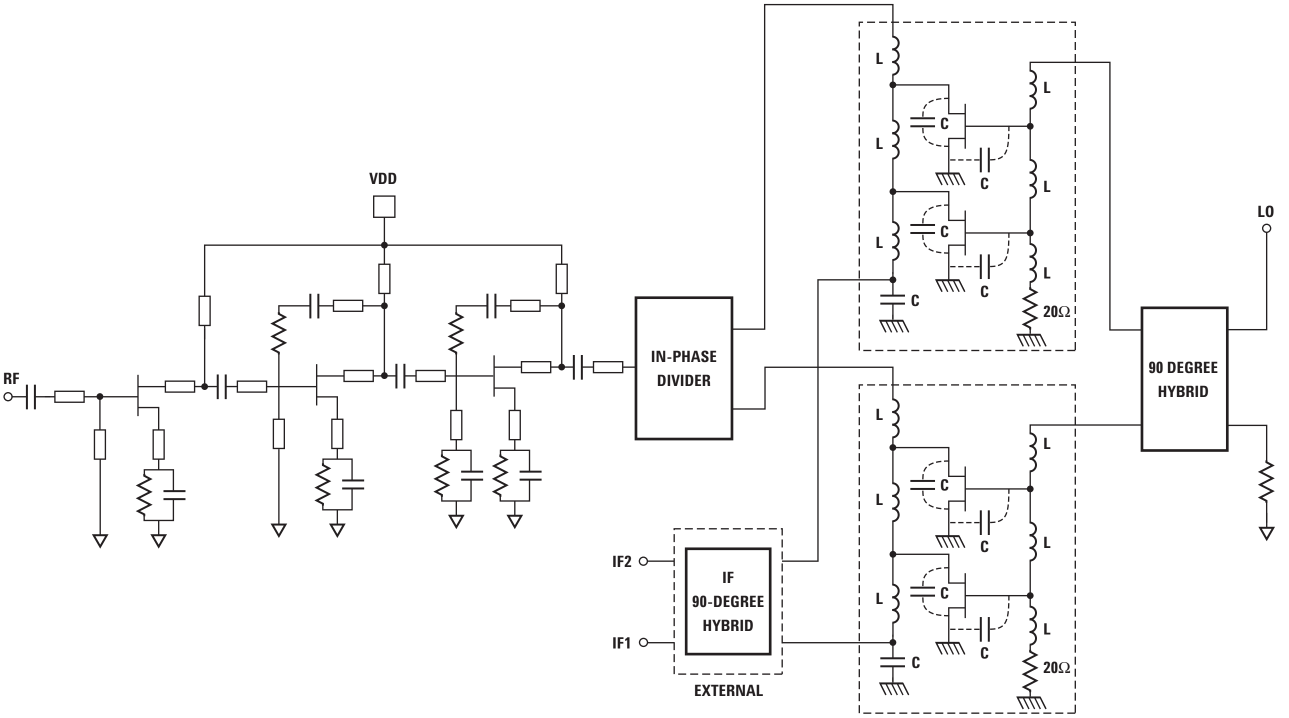


Figure 20. Simplified LNA with IRM Receiver Schematic
(the IF quadrature hybrid is external to the circuit)

Recommended SMT Attachment for 5x5 Package

The AMMP Packaged Devices are compatible with high volume surface mount PCB assembly processes.

The PCB material and mounting pattern, as defined in the data sheet, optimizes RF performance and is strongly recommended. An electronic drawing of the land pattern is available upon request from Agilent Sales & Application Engineering.

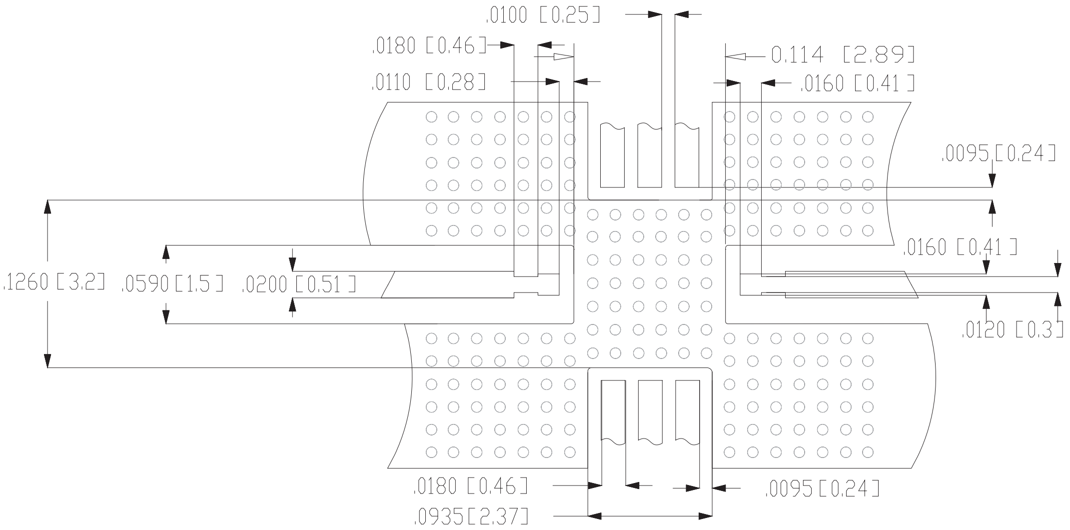


Figure 21. Suggested PCB Land Pattern and Stencil Layout

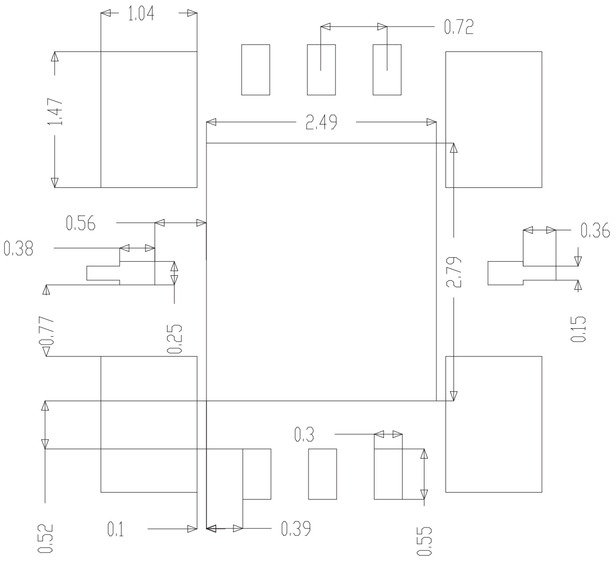


Figure 22. Stencil Outline Drawing (mm)

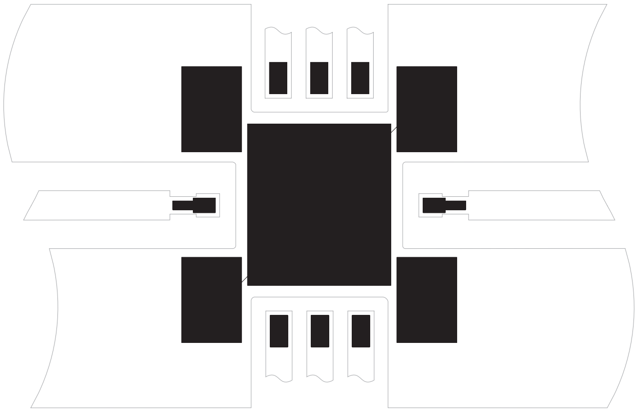


Figure 23. Combined PCB and Stencil Layouts

Manual Assembly

- Follow ESD precautions while handling packages.
- Handling should be along the edges with tweezers.
- Recommended attachment is conductive solder paste. Please see recommended solder reflow profile. Neither Conductive epoxy or hand soldering is recommended.
- Apply solder paste using a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance.
- Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temp. to avoid damage due to thermal shock.
- Packages have been qualified to withstand a peak temperature of 260°C for 20 seconds. Verify that the profile will not expose device beyond these limits.

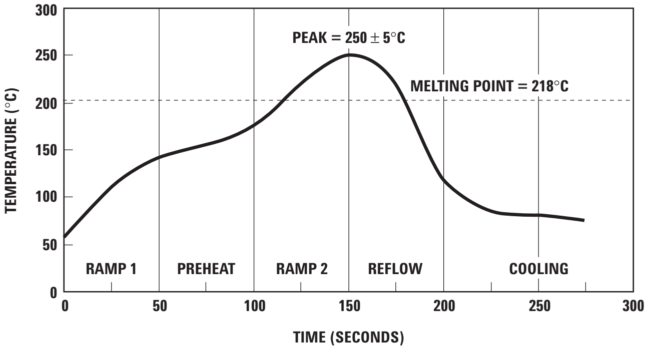


Figure 22. Suggested lead-free Reflow Profile for SnAgCu solder paste

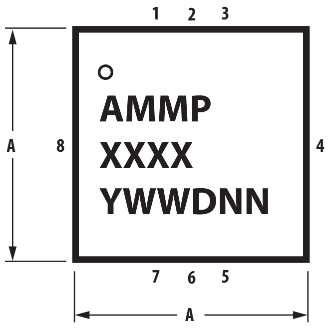
A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads. The recommended stencil layout is shown in Figure 21. The stencil has a solder paste deposition opening approximately 70% to 90% of the PCB pad. Reducing stencil opening can potentially generate more voids underneath. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use a laser cut stencil composed of 0.127mm (5 mils) thick stainless steel which is capable of producing the required fine stencil outline.

The most commonly used solder reflow method is accomplished in a belt furnace using convection heat transfer. The suggested reflow profile for automated reflow processes is shown in Figure 22. This profile is designed to ensure reliable finished joints. However, the profile indicated in Figure 1 will vary among different solder pastes from different manufacturers and is shown here for reference only.

AMMP-6522 Part Number Ordering Information

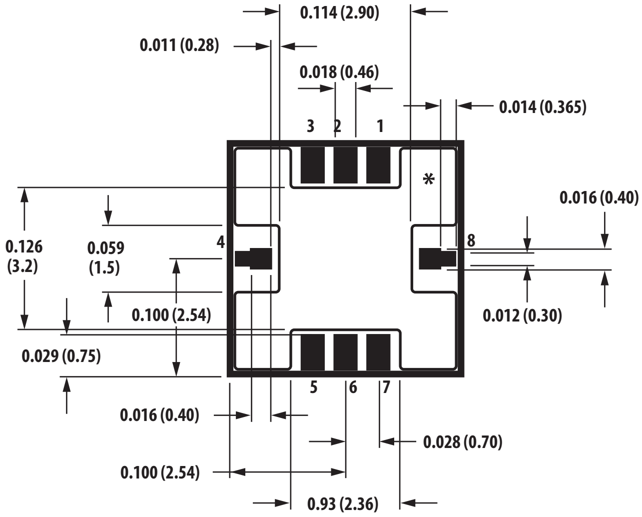
Part Number	Devices per Container	Container
AMMP-6522-BLKG	10	Antistatic bag
AMMP-6522-TR1G	100	7" Reel
AMMP-6522-TR2G	500	7" Reel

Package Dimensions



FRONT VIEW

SIDE VIEW



BACK VIEW

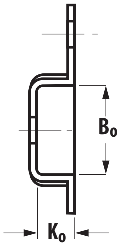
DIMENSIONAL TOLERANCE FOR BACK VIEW: 0.002" (0.05 mm)

SYMBOL	MIN.	MAX.
A	0.198 (5.03)	0.213 (5.4)
B	0.0685 (1.74)	0.088 (2.25)

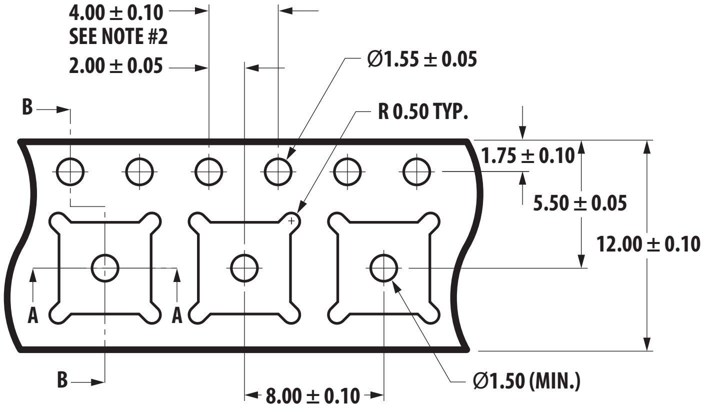
DIMENSIONS ARE IN INCHES (MM)

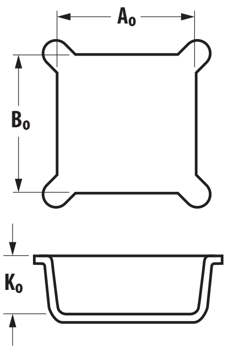
NOTES:
1. * INDICATES PIN 1
2. DIMENSIONS ARE IN INCHES (MILLIMETERS)
3. ALL GROUNDS MUST BE SOLDERED TO PCB RF GROUND

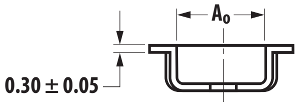
Carrier Tape and Pocket Dimensions



SECTION B-B



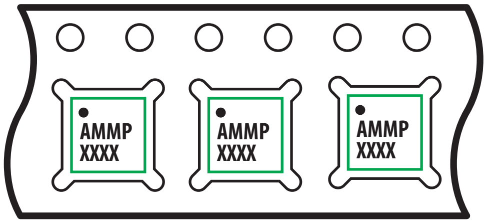




SECTION A-A

A_0: 5.30
B_0: 5.30
K_0: 2.20
PITCH: 8.00
WIDTH: 12.00

	A_0	B_0	K_0
MIN.	5.20	5.20	2.10
NOM.	5.30	5.30	2.20
MAX.	5.40	5.40	2.30



Notes:
1. A_0 and B_0 measured at 0.3 Mm above base of pocket.
2. 10 Pitches cumulative tolerance is ± 0.2 Mm.
3. Dimensions are in millimeters (mm).

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

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