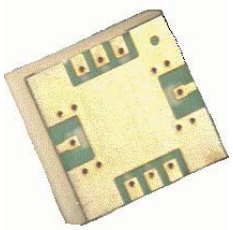
AMMP-6425
18-28 GHz 1W Power Amplifier
in SMT Package

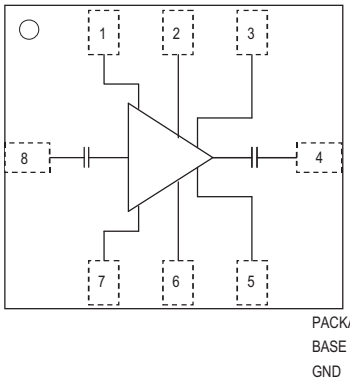
Data Sheet



Description

The AMMP-6425 MMIC is a broadband 1W power amplifier in a surface mount package designed for use in transmitters that operate in various frequency bands between 18GHz and 28GHz. At 25GHz, it provides 31dBm of output power (P-1dB) and 25dB of small-signal gain from a small easy-to-use device. The device has input and output matching circuitry for use in 50Ω environments. The AMMP-6425 also integrates a temperature compensated RF power detection circuit that enables power detection of 0.25V/W. DC bias is simple and the device operates on widely available 5V for current supply (negative voltage only needed for Vg). It is fabricated in a PHEMT process for exceptional power and gain performance.

Pin Connections (Top View)



Pin	Function
1	Vgg
2	Vdd
3	DET_O
4	RF_out
5	DET_R
6	Vdd
7	Vgg
8	RF_in

Features

- 5x5 mm Surface Mount Package
- Wide Frequency Range 18-28GHz
- One watt output power
- 50 Ω match on input and output
- ESD protection (60V MM, and 200V HBM)

Specifications (Vdd=5V, Idsq=650mA)

- Frequency range 18 to 28 GHz
- Small signal Gain of 22dB
- Output power @P-1 of 28dBm (Typ.)
- Input/Output return-loss of -12dB

Applications

- Microwave Radio systems
- Satellite VSAT, DBS Up/Down Link
- LMDS & Pt-Pt mmW Long Haul
- Broadband Wireless Access (including 802.16 and 802.20 WiMax)
- WLL and MMDS loops
- Commercial grade military

Note:
1. This MMIC uses depletion mode pHEMT devices. Negative supply is used for DC gate biasing.

Attention: Observe Precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A): 60V
ESD Human Body Model (Class 0): 200V
The Detector pin ESD voltage level :
MM < 20v and HBM < 60v.
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

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Absolute Maximum Ratings

Symbols	Parameters	Units	Minimum	Maximum	Notes
Vd-Vg	Drain to Gate Voltage	V		8	
Vd	Positive Supply Voltage	V		5.5	
Vg	Gate Supply Voltage	V	-2.5	0.5	
Id	Drain Current	mA		TBD	2
PD	Power Dissipation	W		4	2 and 3
Pin	CW Input Power	dBm		20	2
Tch	Operating Channel Temp	°C		+150	4
Tstg	Storage Case Temp.	°C		-65 to +155	
Tmax	Maximum Assembly Temp (30 sec max)	°C		+320	

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to this device. Functional operation at or near these limitations will significantly reduce the lifetime of the device.
2. Dissipated power PD is in any combination of DC voltage, Drain Current, input power and power delivered to the load.
3. When operated at maximum PD with a base plate temperature of 85 °C, the median time to failure (MTTF) is significantly reduced.
4. These ratings apply to each individual FET. The operating channel temperature will directly affect the device MTTF. For maximum life, it is recommended that junction temperatures (Tj) be maintained at the lowest possible levels. See MTTF vs. Tchannel Temperature Table.

DC Specifications/ Physical Properties [6]

Symbol	Parameters and Test Conditions	Units	Value
I_{dq}	Drain Supply Current (Vdd=5 V, Vg set for Idq Typical)	mA	650
V_g	Gate Supply Operating Voltage (Id(Q) = 650 (mA))	V	-1.1
$R_{\theta JC}$	Thermal Resistance[6] (Channel-to-Base Plate)	°C/W	17.8
T_{ch}	Channel Temperature	°C	142.8

Notes:
6. Assume SnPb soldering to an evaluation RF board at 85°C base plate temperatures. Worst case is at saturated output power when DC power consumption rises to 5.5W with 1.58W RF power delivered to load. Power dissipation is 3.92W and the temperature rise in the channel is 69.8 °C. In this condition, the channel temperature reached at the maximum operational channel temperature of 155°C. To maintain the maximum operational temperature below 155°C, the base plate temperature must be maintained below 85°C

Thermal Properties

Parameter	Test Conditions	Value
Maximum Power Dissipation	Tbaseplate = 85°C	PD = 4W Tchannel = 150°C
Thermal Resistance (θjc)	Vd = 5V Id = 650mA PD = 3.25W Tbaseplate = 85°C	θjc = 17.8°C/W Tchannel = 143°C
Thermal Resistance (θjc) Under RF Drive	Vd = 5V Id = 900mA Pout = 30dBm Pd = 3.5W Tbaseplate = 85°C	θjc = 17.8°C/W Tchannel = 147°C

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MTTF vs. Tchannel Temperature

Operation	60% Confidence Level		90% Confidence Level		Point Data R=	
Tj	λ (ΦIT)	MTTF (hrs)	λ (ΦIT)	MTTF (hrs)	λ (ΦIT)	MTTF (Yrs)
150	3511	2.8E+05	8822	1.1E+05	3831	2.6E+05
140	1298	7.7E+05	3260	3.1E+05	1416	7.1E+05
130	456	2.2E+06	1147	8.7E+05	498	2.0E+05
120	152	6.6E+06	382	2.6E+06	166	6.0E+06
110	48	2.1E+07	120	8.3E+06	52	1.9E+06
100	14	7.0E+07	36	2.8E+07	15	6.5E+07
90	4	2.5E+08	10	1.0E+08	4	2.3E+08
80	1	9.9E+08	3	3.9E+08	1	9.1E+08
70	0	4.2E+09	1	1.7E+09	0	3.8E+09
60	0	1.9E+10	0	7.6E+09	0	1.7E+10
50	0	9.6E+10	0	3.8E+10	0	8.8E+10

AMMP-6425 RF Specifications [1, 2, 3, 4]

(Data obtained from 2.4-mm connector based test fixture, and this data is including connecter loss, and board loss.)
T_A= 25°C, V_{dd} = 5.0 V, I_{dq} =650 mA, V_g = -1.1V, Z_o=50Ω

Symbol	Parameters and Test Conditions		Units	Minimum	Typical	Maximum
Freq	Operational Frequency		GHz	18		28
Gain	Small-signal Gain[3, 4]	Freq (GHz) = 18, 23	dB	21	23	
		Freq (GHz) = 28	dB	20	22	
P_{-1dB}	Output Power at 1dB[3]	Freq (GHz) = 18	dBm	26	28	
	Gain Compression	Freq (GHz) = 23, 28	dBm	27	28	
OIP3	Output Third Order Intercept Point		dBm		35	
RL_{in}	Input Return Loss		dB		10	
RL_{out}	Output Return Loss		dB		10	
Isolation	Reverse Isolation		dB		43	

Notes:
1. Small/Large -signal data measured in packaged form on a 2.4mm connecter based evaluation board at TA = 25°C.
2. This final package part performance is verified by a functional test correlated to actual performance at one or more frequencies
3. Specifications are derived from measurements in a 50Ω test environment. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity, or power matching.
4. Pre-assembly into package performance verified 100% on-wafer published specifications at Frequencies=18, 23, and 28GHz.
5. The Gain and P1dB tested at 18, 23 and 28 GHz guaranteed with measurement accuracy ±1.5dB for Gain and P1dB, except Gain at 18 GHz with measurement accuracy ±1.8dB.

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AMMP-6425 Typical Performance

(Data obtained from 2.4-mm connector based test fixture, and this data is including connecter loss, and board loss.)
(T_A = 25°C, Vdd=5V, Idq=650mA, V_g=-1.1 V, Z_{in} = Z_{out} = 50Ω)

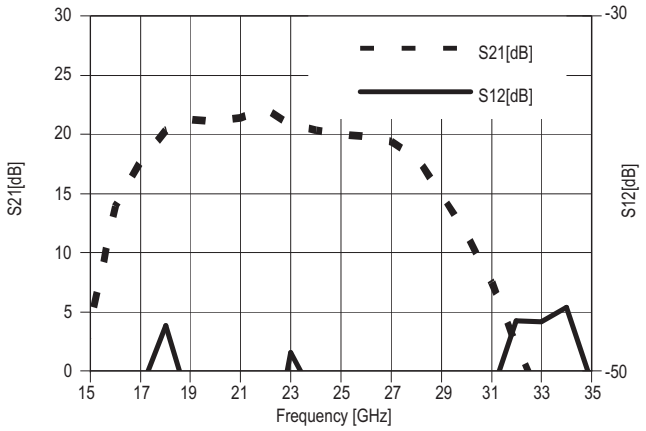

Figure 1. Typical Gain and Reverse Isolation

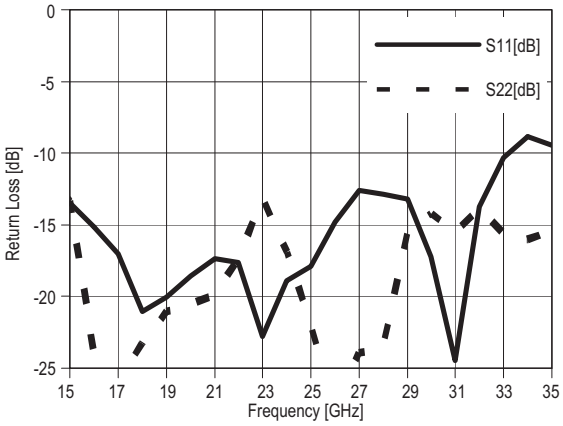

Figure 2. Typical Input & Output Return Loss

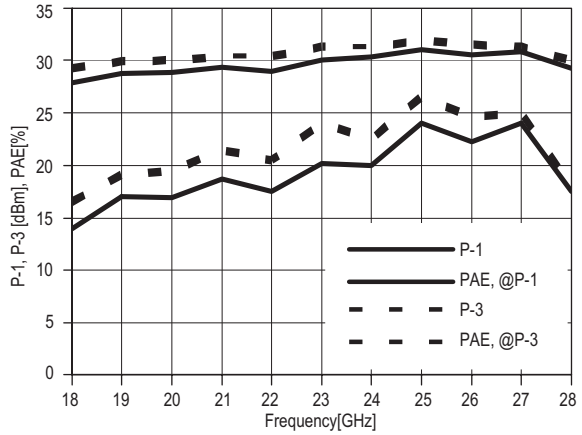

Figure 3. Typical P-1 and PAE

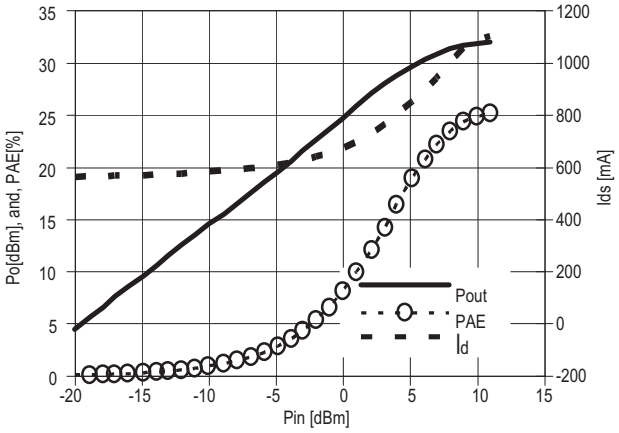

Figure 4. Typical Pout, Ids, and PAE vs. Pin at Freq=25GHz

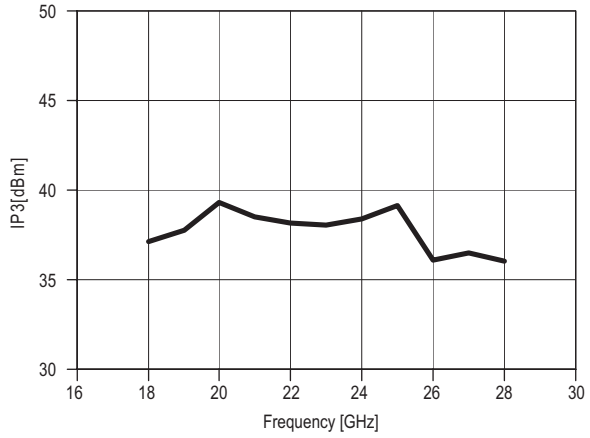

Figure 5. Typical IP3 (Third Order Intercept) @Pin=-20dBm

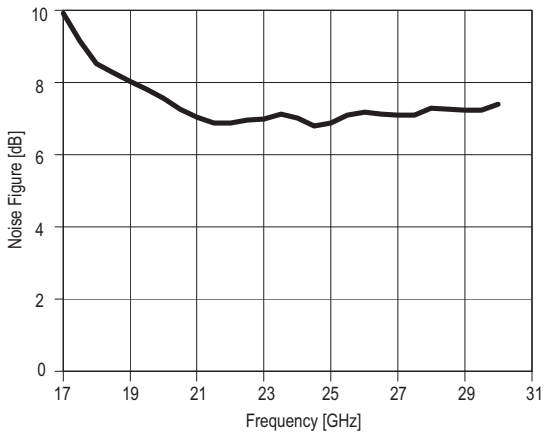

Figure 6. Typical Noise Figure

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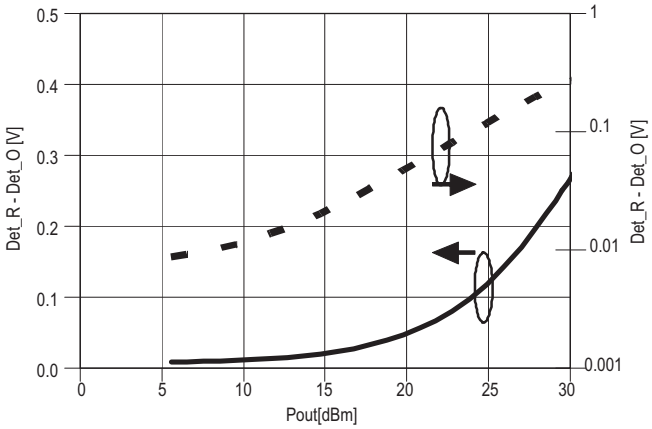

Figure 7. Typical Detector voltage vs. Output Power

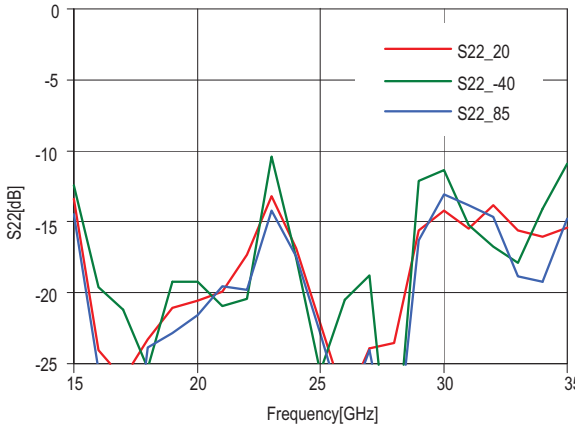

Figure 8. Typical S22 over temperature

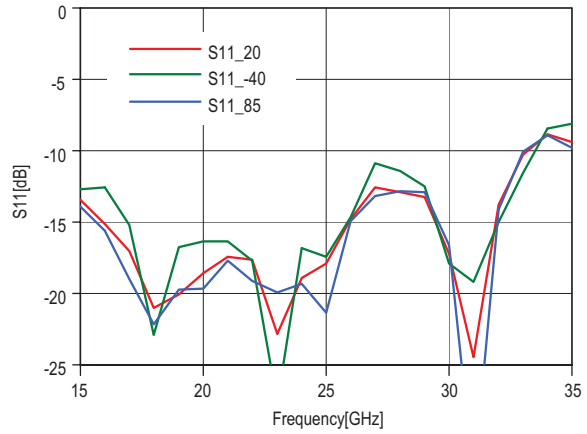

Figure 9. Typical S11 over temperature

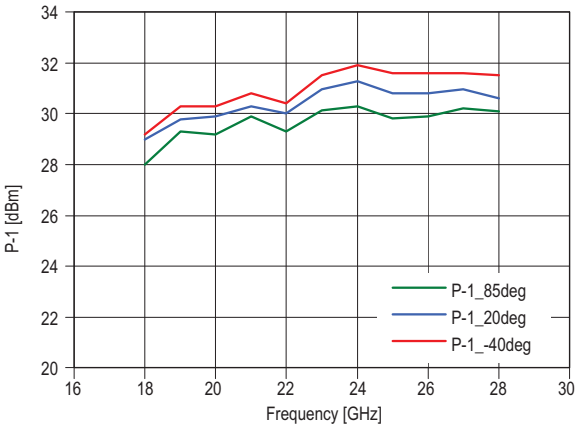

Figure 10. Typical P-1 over temperature

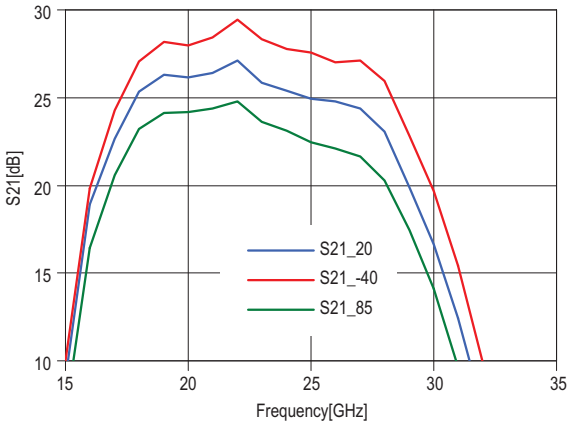

Figure 11. Typical Gain over temperature

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Typical Scattering Parameters [1]

(T_A = 25°C, V_{dd} =5 V, I_{dq} = 650 mA, Z_{in} = Z_{out} = 50Ω)

Freq	S11			S21			S12			S22		
[GHz]	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase
1	-0.178	0.980	-37.820	-47.292	0.004	-74.488	-80.369	9.58E-05	103.780	-0.085	0.990	-34.276
2	-0.523	0.942	-74.503	-44.008	0.006	149.890	-70.925	2.84E-04	15.146	-0.279	0.968	-68.410
3	-0.978	0.893	-110.430	-46.417	0.005	67.301	-65.116	5.55E-04	-50.709	-0.630	0.930	-102.400
4	-1.451	0.846	-145.650	-46.503	0.005	13.513	-62.769	7.27E-04	-62.503	-1.318	0.859	-134.930
5	-2.031	0.792	178.840	-45.038	0.006	-58.861	-58.964	1.13E-03	-135.670	-1.389	0.852	-167.440
6	-2.704	0.732	143.950	-47.901	0.004	-154.120	-54.809	1.82E-03	178.760	-1.958	0.798	158.670
7	-3.392	0.677	109.310	-49.517	0.003	169.350	-53.665	2.07E-03	141.890	-2.558	0.745	125.480
8	-4.109	0.623	75.156	-50.018	0.003	105.240	-51.070	2.80E-03	104.940	-3.104	0.700	92.207
9	-4.791	0.576	41.436	-53.613	0.002	44.075	-51.693	2.60E-03	53.998	-3.633	0.658	58.406
10	-5.516	0.530	8.579	-56.475	0.002	-12.575	-51.331	2.71E-03	32.567	-4.100	0.624	24.394
11	-6.364	0.481	-23.142	-46.029	0.005	-103.650	-51.167	2.76E-03	11.953	-4.608	0.588	-10.323
12	-7.445	0.424	-52.655	-29.971	0.032	-152.130	-51.615	2.63E-03	3.625	-5.224	0.548	-45.888
13	-8.819	0.362	-78.361	-16.053	0.158	149.700	-50.249	3.07E-03	-15.675	-6.438	0.477	-82.797
14	-10.363	0.303	-98.427	-3.496	0.669	81.099	-50.263	3.07E-03	-28.191	-9.045	0.353	-120.890
15	-11.090	0.279	-112.740	8.685	2.718	-4.135	-46.066	4.97E-03	-65.232	-14.588	0.186	-150.360
16	-12.282	0.243	-131.170	18.694	8.604	-119.950	-46.237	4.88E-03	-110.450	-24.953	0.057	-82.936
17	-12.416	0.239	-151.110	22.143	12.798	128.380	-60.278	9.68E-04	-136.210	-14.586	0.187	-124.060
18	-18.133	0.124	-159.160	25.421	18.666	25.746	-58.209	1.23E-03	-69.871	-17.548	0.133	-113.800
19	-11.405	0.269	-143.530	24.729	17.236	-77.696	-47.566	4.18E-03	-85.440	-9.908	0.320	-139.560
20	-12.614	0.234	172.380	25.037	17.859	-153.820	-45.013	5.61E-03	-114.600	-12.434	0.239	164.360
21	-15.765	0.163	172.820	25.244	18.289	120.010	-46.939	4.50E-03	-153.480	-19.545	0.105	177.540
22	-18.729	0.116	169.430	25.205	18.208	41.393	-46.250	4.87E-03	-155.050	-19.073	0.111	-162.420
23	-19.222	0.109	155.900	24.889	17.557	-34.617	-49.429	3.38E-03	165.260	-19.220	0.109	176.780
24	-16.511	0.149	168.470	23.841	15.562	-111.460	-47.594	4.17E-03	177.280	-17.045	0.141	-178.550
25	-18.712	0.116	146.270	23.888	15.647	-179.450	-46.045	4.99E-03	168.010	-18.114	0.124	171.490
26	-17.947	0.127	175.590	24.682	17.143	103.360	-45.724	5.17E-03	158.550	-16.455	0.150	-178.830
27	-11.711	0.260	168.100	24.823	17.423	13.068	-42.460	7.53E-03	135.940	-11.479	0.267	172.720
28	-10.060	0.314	125.410	22.405	13.191	-74.382	-41.090	8.82E-03	113.320	-11.025	0.281	129.980
29	-13.299	0.216	95.693	19.705	9.666	-157.160	-42.711	7.32E-03	83.227	-15.117	0.175	123.360
30	-17.064	0.140	102.470	16.154	6.422	122.330	-38.921	1.13E-02	55.944	-13.896	0.202	133.650
31	-13.487	0.212	101.410	12.154	4.052	48.186	-44.057	6.27E-03	18.061	-11.050	0.280	111.830
32	-11.785	0.257	84.008	8.383	2.625	-23.332	-46.564	4.70E-03	2.928	-10.645	0.294	91.607
33	-11.532	0.265	62.490	4.076	1.599	-91.933	-53.813	2.04E-03	17.837	-10.575	0.296	76.604
34	-10.906	0.285	45.088	0.130	1.015	-158.780	-55.014	1.78E-03	112.070	-10.010	0.316	61.871
35	-10.536	0.297	23.915	-4.190	0.617	136.430	-48.002	3.98E-03	132.840	-9.589	0.332	45.962
36	-10.699	0.292	-1.693	-8.418	0.379	74.411	-40.193	9.78E-03	80.387	-9.107	0.350	29.444
37	-12.367	0.241	-29.330	-12.489	0.237	15.586	-38.833	1.14E-02	35.254	-8.758	0.365	12.764
38	-17.928	0.127	-55.180	-16.801	0.145	-41.207	-37.437	1.34E-02	6.758	-8.550	0.374	-1.575
39	-23.162	0.069	34.718	-21.962	0.080	-95.210	-34.527	1.88E-02	-16.672	-8.096	0.394	-17.493
40	-11.353	0.271	26.590	-27.653	0.041	-155.570	-36.493	1.50E-02	-57.641	-7.734	0.410	-32.201
41	-7.080	0.443	-9.207	-40.696	0.009	131.530	-36.464	1.50E-02	-63.002	-7.456	0.424	-46.161
42	-5.965	0.503	-39.140	-36.215	0.015	-26.815	-36.100	1.57E-02	-66.924	-6.986	0.447	-60.000
43	-6.061	0.498	-62.125	-33.829	0.020	-89.274	-34.607	1.86E-02	-102.970	-6.790	0.458	-74.546
44	-6.152	0.492	-76.987	-32.808	0.023	-126.740	-33.593	2.09E-02	-126.260	-6.710	0.462	-87.216
45	-5.936	0.505	-89.697	-36.302	0.015	-161.820	-37.542	1.33E-02	-154.850	-6.733	0.461	-98.984

Note:
1. Data obtained from a 2.4-mm connecter based module, and this data is including connecter loss, and board loss.

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AMMP-6425 Application and Usage

Recommended quiescent DC bias condition for optimum power and linearity performances is Vdd=5 volts with Vg (-1.1V) set for Idq=650 mA. Minor improvements in performance are possible depending on the application. The drain bias voltage range is 3 to 5V. A single DC gate supply connected to Vgg will bias all gain stages. Muting can be accomplished by setting Vgg to the pinch-off voltage Vp.

A simplified schematic for the AMMP6425 MMIC die is shown in Figure 12. The MMIC die contains ESD and over voltage protection diodes for Vg, and Vdd terminals. The package diagram for the recommended assembly is shown in Figure 13. In finalized package form, ESD diodes protect all possible ESD or over voltage damages between Vgg and ground, Vgg and Vdd, Vdd and ground. Typical ESD diode current versus diode voltage for 11-connected diodes in series is shown in Figure 14. Under the recommended DC quiescent biasing condition at Vds=5V, Ids=650mA, Vgg=-1V, typical gate terminal current is approximately 0.3mA. If an active biasing technique is selected for the AMMP6425 MMIC PA DC biasing, the active biasing circuit must have more than 10-times higher internal current that the gate terminal current.

An optional output power detector network is also provided. The differential voltage between the Det-Ref and Det-Out pads can be correlated with the RF power emerging from the RF output port. The detected voltage is given by :

$$V = (V_{ref} - V_{det}) - V_{ofs}$$

where V_{ref} is the voltage at the DET_R port, V_{det} is a voltage at the DET_0 port, V_{ofs} and is the zero-input-power offset voltage.

There are three methods to calculate V_{ofs} :

1. V_{ofs} can be measured before each detector measurement (by removing or switching off the power source and measuring V_{ref} - V_{det}). This method gives an error due to temperature drift of less than 0.01dB/50°C.
2. V_{ofs} can be measured at a single reference temperature. The drift error will be less than 0.25dB.
3. V_{ofs} can either be characterized over temperature and stored in a lookup table, or it can be measured at two temperatures and a linear fit used to calculate V_{ofs} at any temperature. This method gives an error close to the method #1.

The RF ports are AC coupled at the RF input to the first stage and the RF output of the final stage. No ground wired are needed since ground connections are made with plated through-holes to the backside of the device.

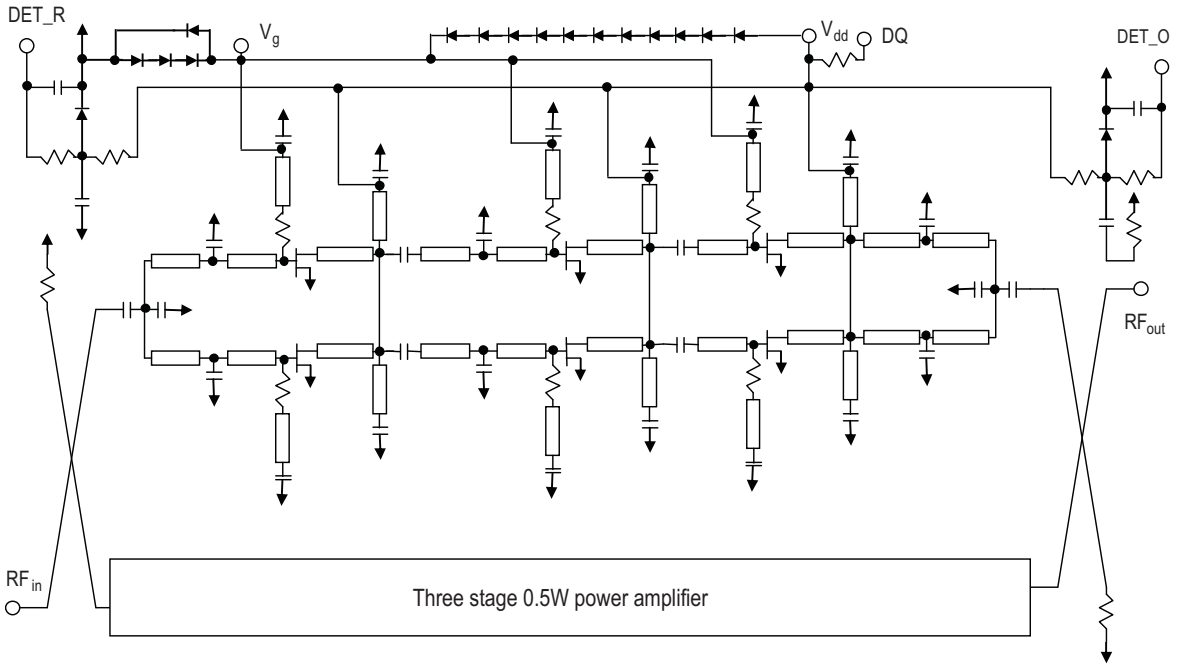

Figure 12. Simplified schematic for the MMIC die

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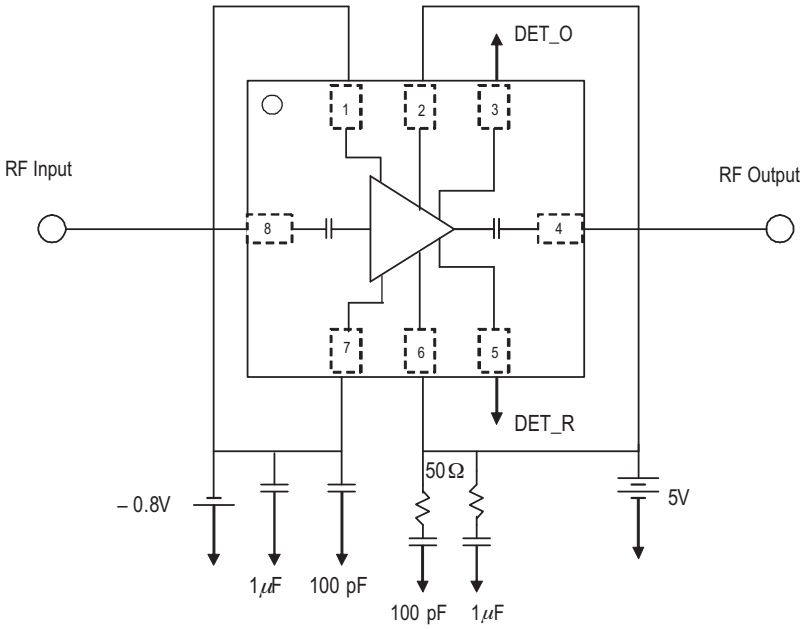

Pin	Function
1	Vgg
2	Vdd
3	DET_O
4	RF_out
5	DET_R
6	Vdd
7	Vgg
8	RF_in

Figure 13. Typical DC connection

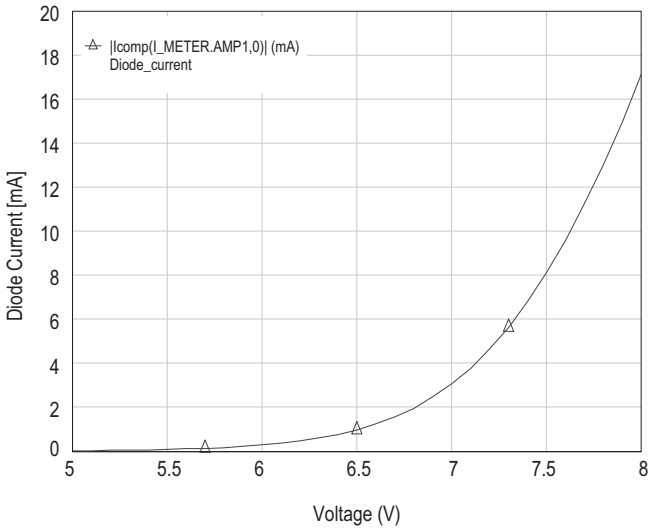

Figure 14. Typical ESD diode current versus diode voltage for 11-connected diodes in series

Note:

No RF performance degradation is seen due to ESD up to 200V HBM and 60V MM. The DC characteristics in general show increased leakage at lower ESD discharge voltages. The user is reminded that this device is ESD sensitive and needs to be handled with all necessary ESD protocols.

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Recommended SMT Attachment for 5x5 Package

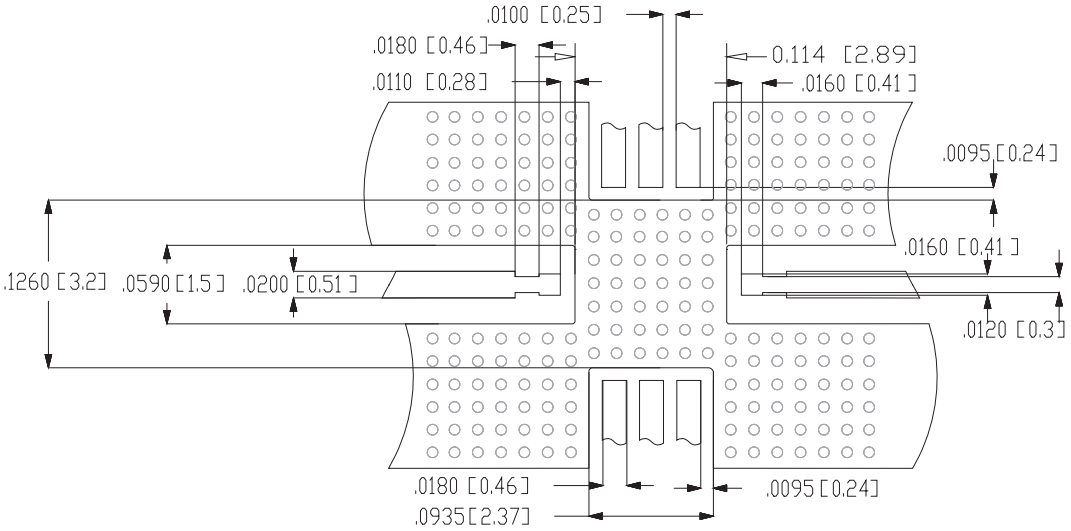

Figure 15a. Suggested PCB Land Pattern and Stencil Layout

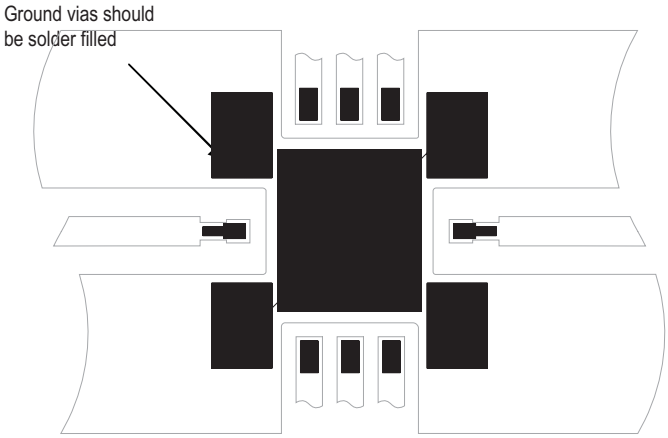

Figure 15b. PCB Land Pattern and Stencil Layouts

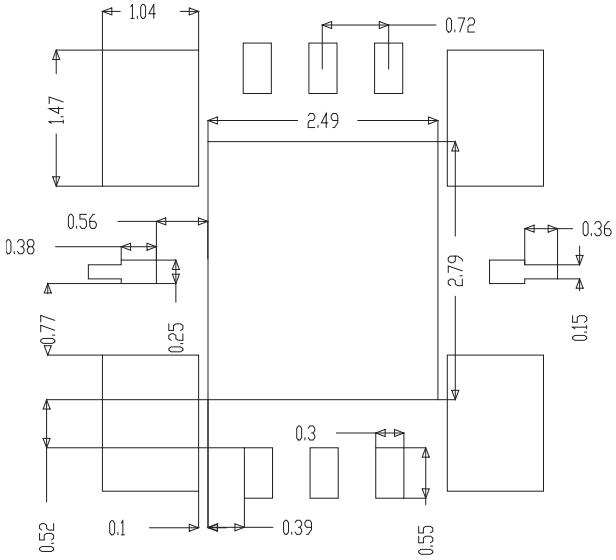

Figure 15c. Stencil Outline Drawing(mm)

The AMMP Packaged Devices are compatible with high volume surface mount PCB assembly processes.

The PCB material and mounting pattern, as defined in the data sheet, optimizes RF performance and is strongly recommended. An electronic drawing of the land pattern is available upon request from Avago Sales & Application Engineering.

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Manual Assembly

- Follow ESD precautions while handling packages.
- Handling should be along the edges with tweezers.
- Recommended attachment is conductive solder paste. Please see recommended solder reflow profile. Neither Conductive epoxy or hand soldering is recommended.
- Apply solder paste using a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance.
- Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temp. to avoid damage due to thermal shock.
- Packages have been qualified to withstand a peak temperature of 260°C for 20 seconds. Verify that the profile will not expose device beyond these limits.

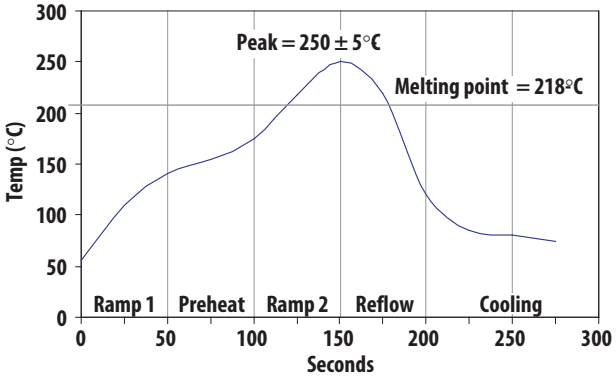

Figure 16. Suggested Lead-Free Reflow Profile for SnAgCu Solder Paste

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads. The recommended stencil layout is shown in Figure 15b. The stencil has a solder paste deposition opening approximately 70% to 90% of the PCB pad. Reducing stencil opening can potentially generate more voids underneath. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use a laser cut stencil composed of 0.127mm (5 mils) thick stainless steel which is capable of producing the required fine stencil outline.

The most commonly used solder reflow method is accomplished in a belt furnace using convection heat transfer. The suggested reflow profile for automated reflow processes is shown in Figure 16. This profile is designed to ensure reliable finished joints. However, the profile indicated in Figure 1 will vary among different solder pastes from different manufacturers and is shown here for reference only.

AMMP-6425 Part Number Ordering Information

Part Number	Devices Per Container	Container
AMMP-6425-BLKG	10	Antistatic bag
AMMP-6425-TR1G	100	7″ Reel
AMMP-6425-TR2G	500	7″ Reel

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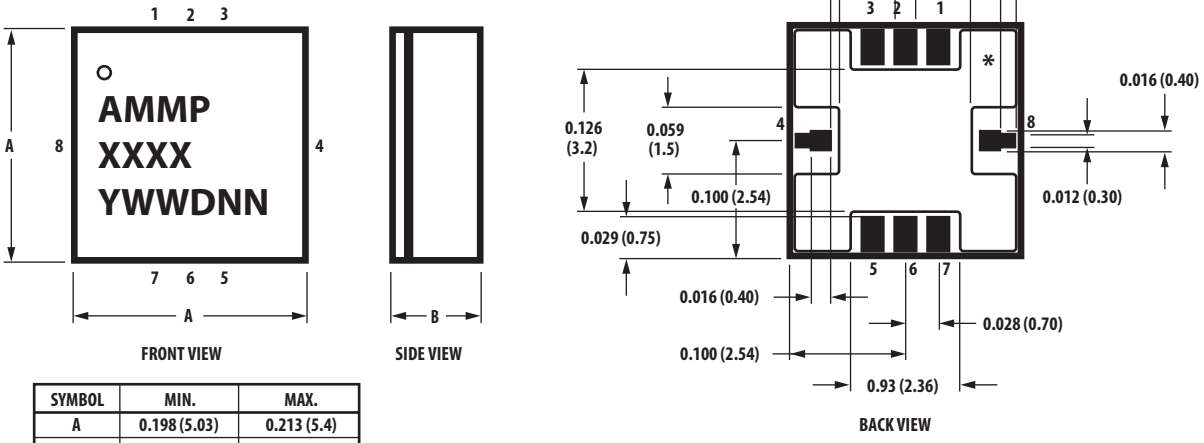
Package Dimensions



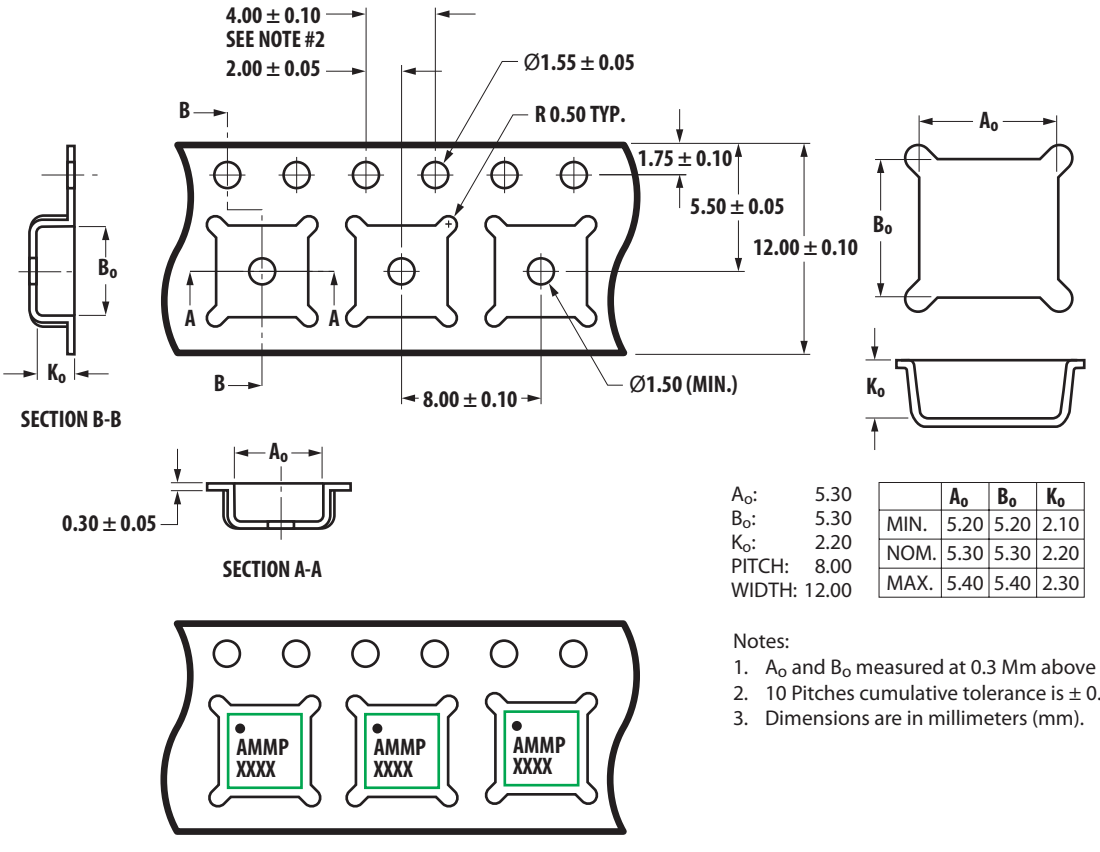
SYMBOL	MIN.	MAX.
A	0.198 (5.03)	0.213 (5.4)
B	0.0685 (1.74)	0.088 (2.25)

DIMENSIONS ARE IN INCHES (MM)

DIMENSIONAL TOLERANCE FOR BACK VIEW: 0.002" (0.05 mm)

NOTES:
1. * INDICATES PIN 1
2. DIMENSIONS ARE IN INCHES (MILLIMETERS)
3. ALL GROUNDS MUST BE SOLDERED TO PCB RF GROUND

Tape Dimensions



A_o:	5.30
B_o:	5.30
K_o:	2.20
PITCH:	8.00
WIDTH:	12.00

	A_o	B_o	K_o
MIN.	5.20	5.20	2.10
NOM.	5.30	5.30	2.20
MAX.	5.40	5.40	2.30

Notes:
1. A_o and B_o measured at 0.3 Mm above base of pocket.
2. 10 Pitches cumulative tolerance is ± 0.2 Mm.
3. Dimensions are in millimeters (mm).

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AV02-0034EN - February 25, 2010

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