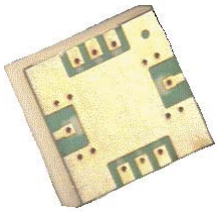
AMMP-6222
7 to 21 GHz GaAs High Linearity LNA in SMT Package

AVAGO TECHNOLOGIES

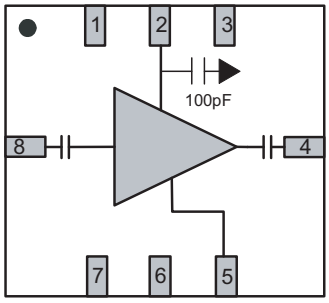
Data Sheet



Description

Avago Technologies' AMMP-6222 is an easy-to-use broadband, high gain, high linearity Low Noise Amplifier in a surface mount package. The wide band and unconditionally stable performance makes this MMIC ideal as a primary or sub-sequential low noise block or a transmitter or LO driver. The MMIC has 3 gain stages and a selectable pin to switch between low and high current, corresponding with low and high output power and linearity. In the high current, high output power state, it requires a 4V, 120mA supply. In the low current, low output power state, the supply is reduced to 4V, 95mA. Since this MMIC covers several bands, it can reduce part inventory and increase volume purchase options The MMIC is fabricated using PHEMT technology. The surface mount package eliminates the need of "chip & wire" assembly for lower cost. This MMIC is fully SMT compatible with backside grounding and I/Os.

Pin Connections (Top View)



Top view
Package base: GND

Pin	Function
1	
2	Vdd
3	
4	RFout
5	Current Sel
6	
7	
8	RFin

Features

- Surface Mount Package, 5.0 x 5.0 x 1.25 mm
- Single Positive Bias Pin
- Selectable Output Power / Linearity
- No Negative Gate Bias

Specifications (Vdd = 4.0V, Idd = 120mA)

- RF Frequencies: 7 - 21 GHz
- High Output IP3: 29dBm
- High Small-Signal Gain: 24dB
- Typical Noise Figure: 2.3dB
- Input, Output Match: -10dB

Applications

- Microwave Radio systems
- Satellite VSAT, DBS Up/Down Link
- LMDS & Pt-Pt mmW Long Haul
- Broadband Wireless Access (including 802.16 and 802.20 WiMax)
- WLL and MMDS loops

Note:
1. This MMIC uses depletion mode pHEMT devices.

Attention:
Observe precautions for handling electrostatic sensitive devices.

ESD Machine Model (60V)
ESD Human Body Model (150V)
Refer to Avago Application Note A004R:
Electrostatic Discharge Damage and Control

Absolute Maximum Ratings [1]

Parameters/Condition	Symbol	Unit	Maximum
Drain to Ground Voltage	Vdd	V	5.5
Drain Current	Idd	mA	170
RF CW Input Power Max	Pin	dBm	10
Max channel temperature	Tch	C	+150
Storage temperature	Tstg	C	-65 +150
Maximum Assembly Temp	Tmax	C	260 for 20s

1. Operation in excess of any of these conditions may result in permanent damage to this device. The absolute maximum ratings for Vdd, Idd and Pin were determined at an ambient temperature of 25°C unless noted otherwise.

DC Specifications/ Physical Properties [2]

Parameter and Test Condition	Symbol	Unit	Minimum	Typical	Maximum
Drain Supply Current under any RF power drive and temp. (Vd=4.0 V)	Idd	mA	80	120	160
Drain Supply Voltage	Vd	V	3	4	5
Thermal Resistance[3]	θjc	°C/W		31.4	

2. Ambient operational temperature TA=25°C unless noted
3. Channel-to-backside Thermal Resistance (Tchannel = 34°C) as measured using infrared microscopy. Thermal Resistance at backside temp. (Tb) = 25°C calculated from measured data.

AMMP-6222 RF Specifications [4]

TA= 25°C, Idd=120mA, Vdd = 4.0 V, Zo=50 Ω

				High Output Power Configuration			Low Output Power Configuration		
Parameters and Test Conditions	Symbol	Units	Freq. (GHz)	Minimum	Typical	Maximum	Minimum	Typical	Maximum
Drain Current	Idd	mA			120			95	
Small-Signal Gain [5]	Gain	dB	9, 12, 17	19	24			23	
Noise Figure into 50Ω [5]	NF	dB	9, 12, 17		2.3	3.5		2.3	
Output Power at 1dB Gain Compression	P-1dB	dBm			15.5			14	
Output Power at 3dB Gain Compression	P-3dB	dBm			17.5			16	
Output Third Order Intercept Point	OIP3	dBm			29			27	
Isolation	Iso	dB			-45			-45	
Input Return Loss	RLin	dB			-10			-10	
Output Return Loss	RLout	dB			-10			-10	

4. Refer to characteristic plots for detailed individual frequency performance.
5. All tested parameters guaranteed with measurement accuracy ± 0.5dB for gain and ±0.3dB for NF in the high output power configuration.

AMMP-6222 Typical Performance for High Current, High Output Power Configuration [1], [2]

(T_A = 25°C, Vdd=4V, Idd=120mA, Zin = Zout = 50 Ω unless noted)

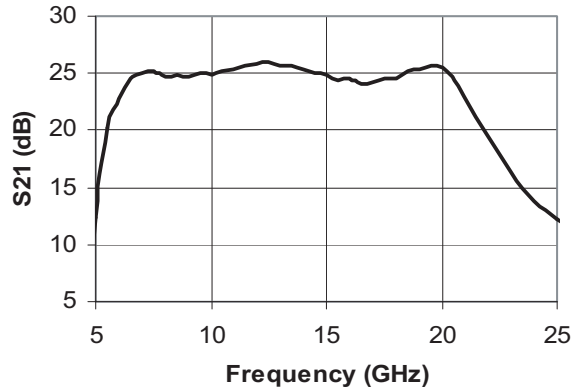


Figure 1a. Small-signal Gain

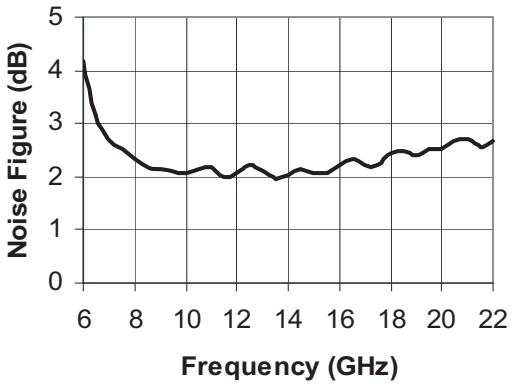


Figure 2a. Noise Figure

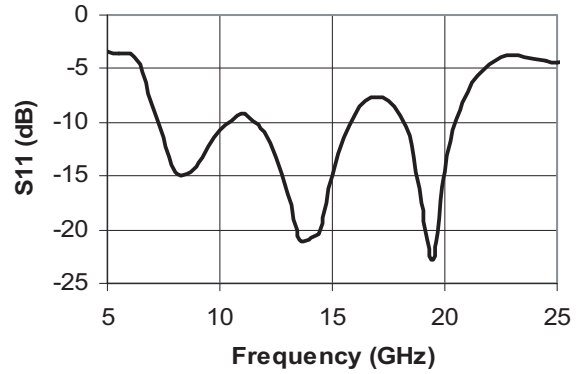


Figure 3a. Input Return Loss

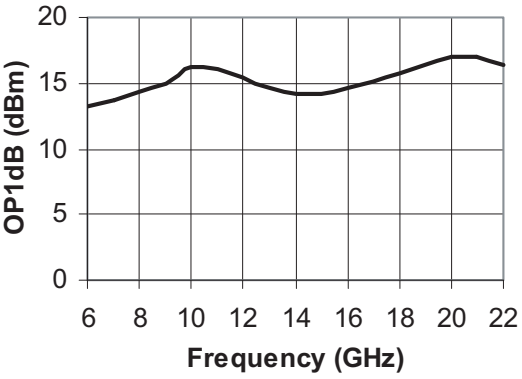


Figure 4a. Output P-1dB

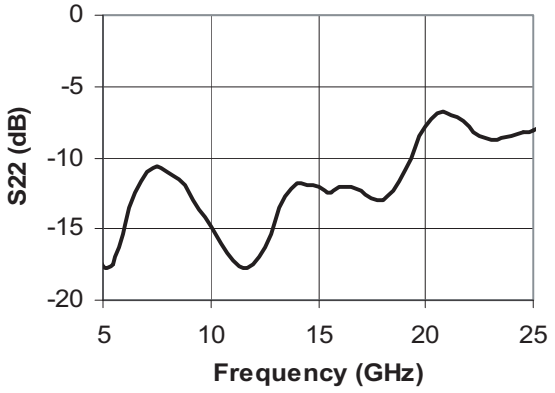


Figure 5a. Output Return Loss

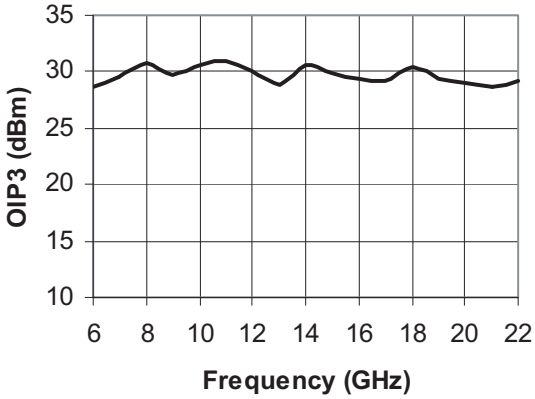


Figure 6a. Output IP3

Note:
1. S-parameters are measured with R&D Eval Board as shown in Figure 21. Board and connector effects are included in the data.
2. Noise Figure is measured with R&D Eval board as shown in Figure 21, and with a 3-dB pad at input. Board and connector losses are already de-embeded from the data.

AMMP-6222 Typical Performance for High Current, High Output Power Configuration (Cont)

(T_A = 25°C, Vdd=4V, Idd=120mA, Zin = Zout = 50 Ω unless noted)

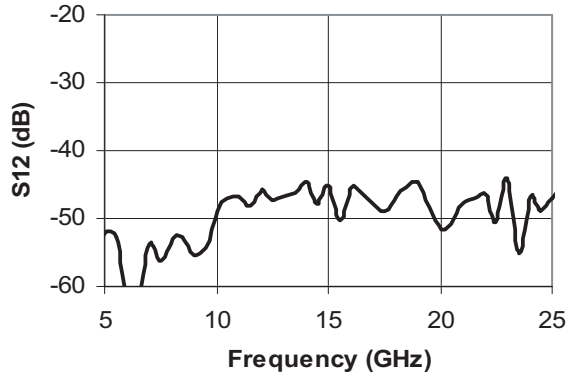


Figure 7a. Isolation

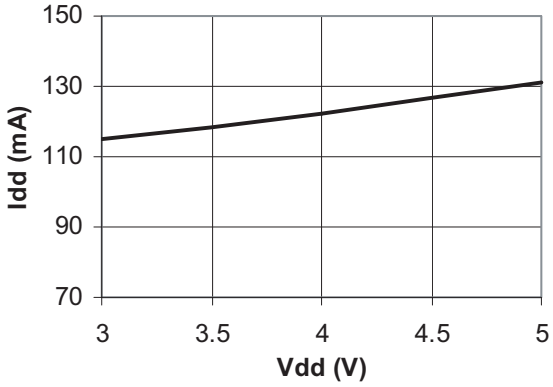


Figure 8a. Idd over Vdd

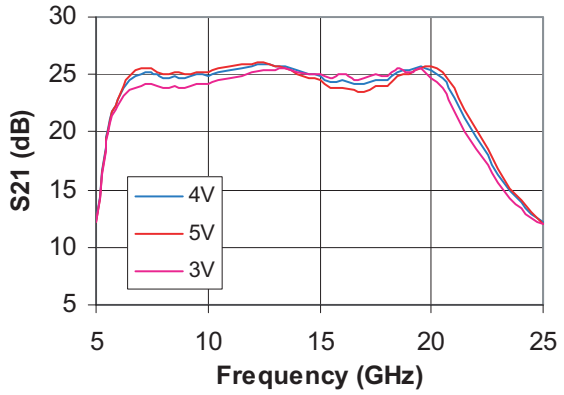


Figure 9a. Small-signal Gain Over Vdd

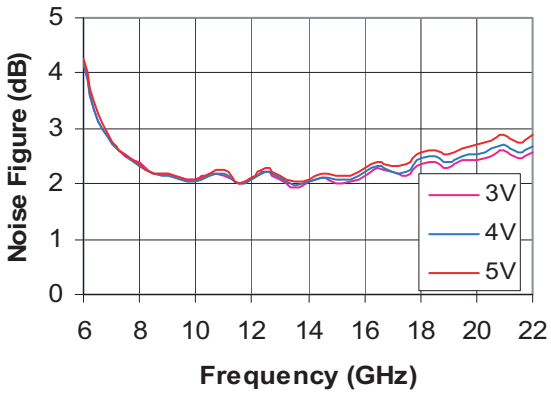


Figure 10a. Noise Figure Over Vdd

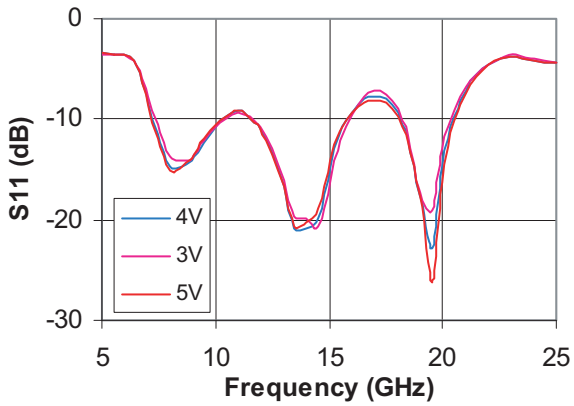


Figure 11a. Input Return Loss Over Vdd

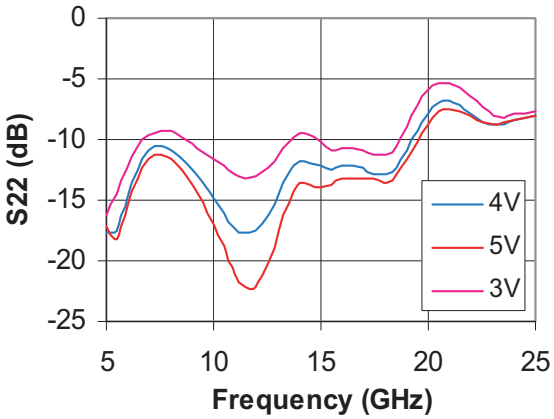


Figure 12a. Output Return Loss Over Vdd

AMMP-6222 Typical Performance for High Current, High Output Power Configuration (Cont)

(TA = 25°C, Vdd=4V, Idd=120mA, Zin = Zout = 50 Ω unless noted)

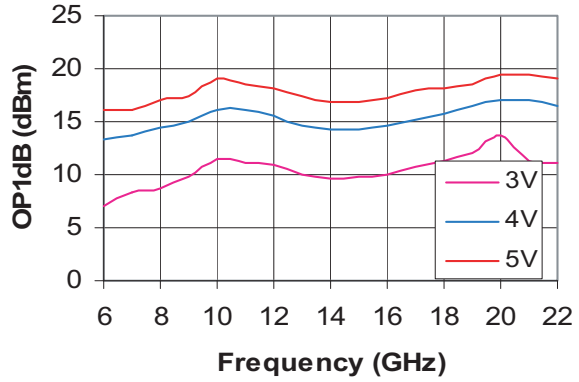


Figure 13a. Output P1dB over Vdd

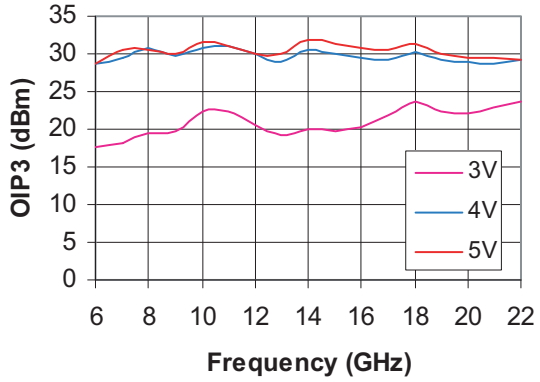


Figure 14a. Output IP3 over Vdd

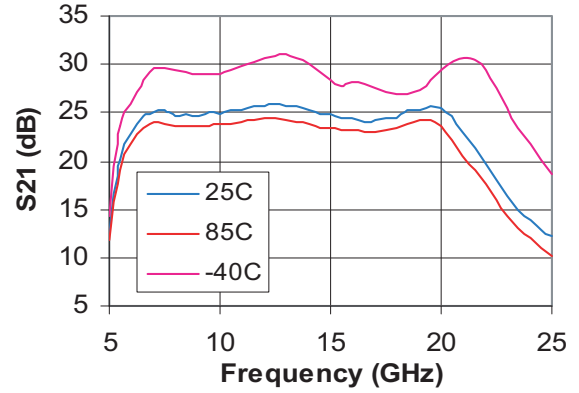


Figure 15a. Small-signal Gain Over Temp

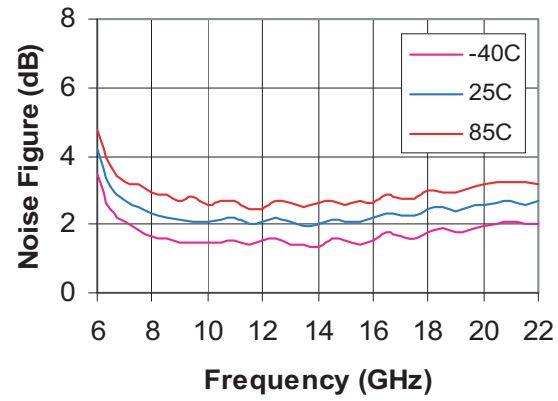


Figure 16a. Noise Figure Over Temp

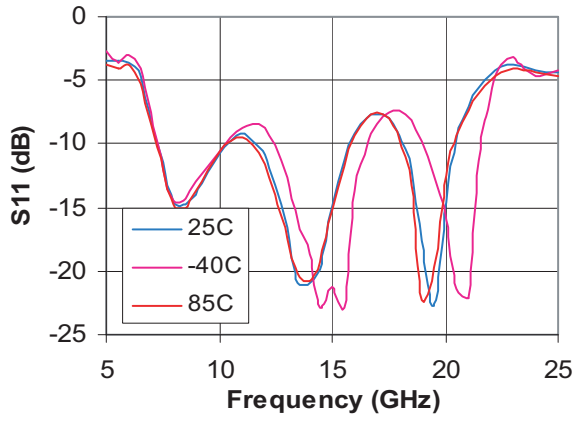


Figure 17a. Input Return Loss Over Temp

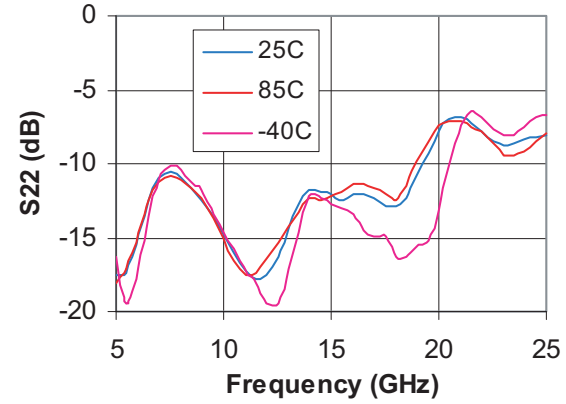


Figure 18a. Output Return Loss Over Temp

AMMP-6222 Typical Performance for Low Current, Low Output Power Configuration [1], [2]

(T_A = 25°C, Vdd=4V, Idd=95mA, Zin = Zout = 50 Ω unless noted)

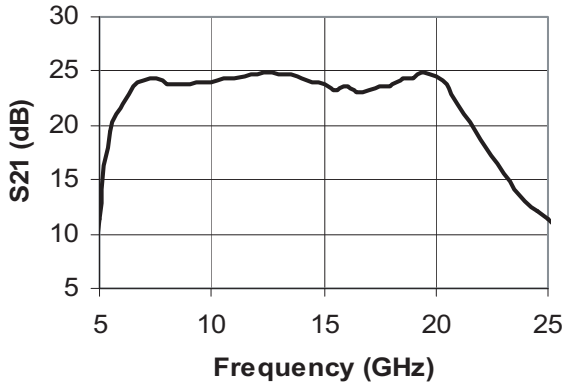


Figure 1b. Small-signal Gain

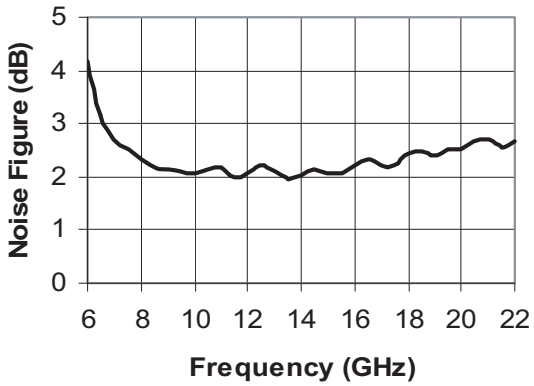


Figure 2b. Noise Figure

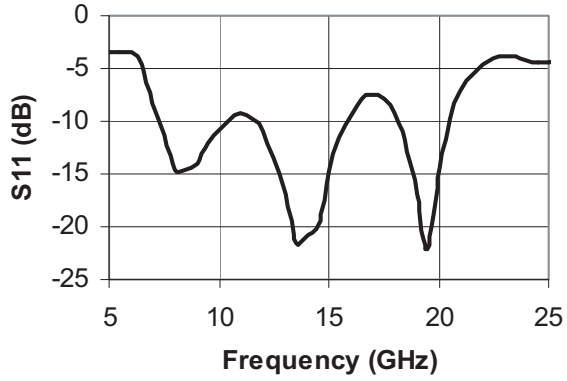


Figure 3b. Input Return Loss

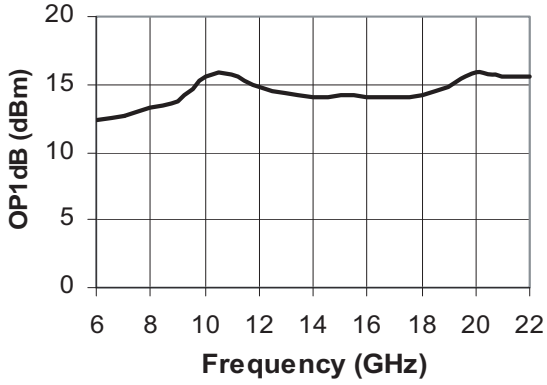


Figure 4b. Output P-1dB

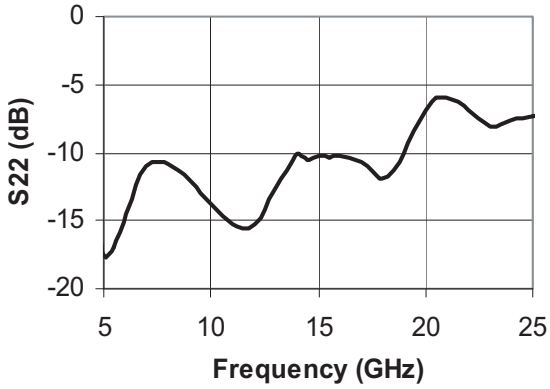


Figure 5b. Output Return Loss

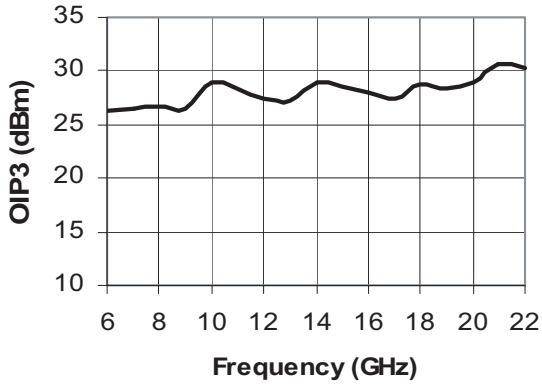


Figure 6b. Output IP3

Note:
1. S-parameters are measured with R&D Eval Board as shown in Figure 21. Board and connector effects are included in the data.
2. Noise Figure is measured with R&D Eval board as shown in Figure 21, and with a 3-dB pad at input. Board and connector losses are already de-embeded from the data

AMMP-6222 Typical Performance for Low Current, Low Output Power Configuration (Cont)

(T_A = 25°C, Vdd=4V, Idd=95mA, Zin = Zout = 50 Ω unless noted)

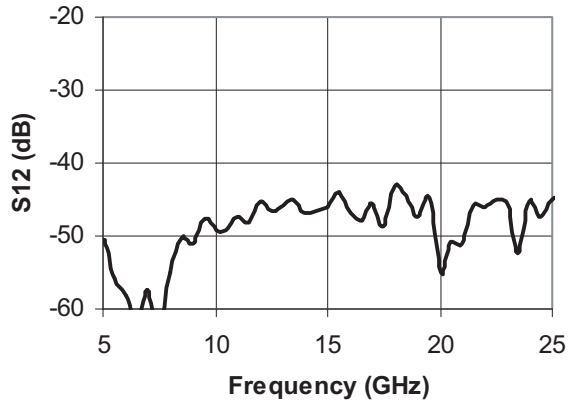


Figure 7b. Isolation

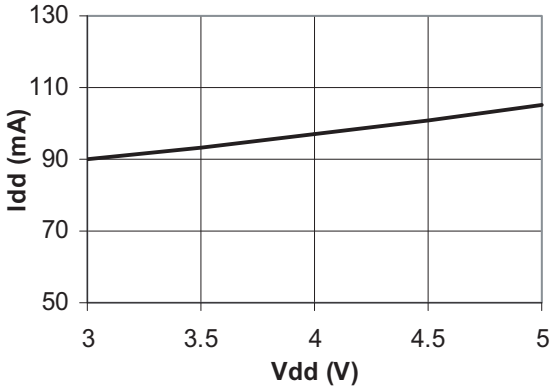


Figure 8b. Idd over Vdd

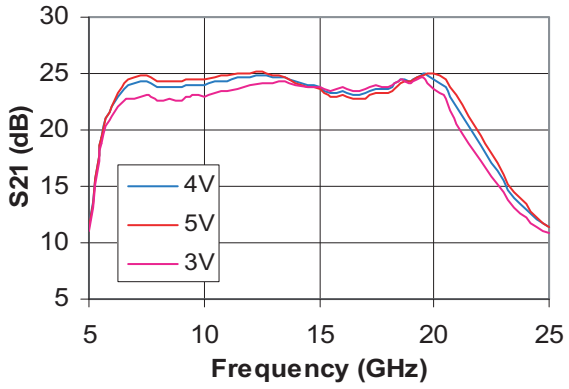


Figure 9b. Small-signal Gain Over Vdd

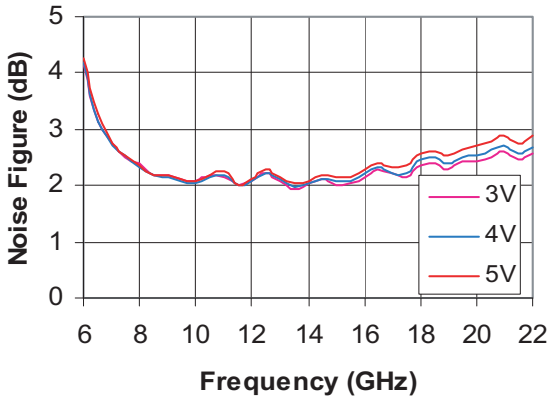


Figure 10b. Noise Figure Over Vdd

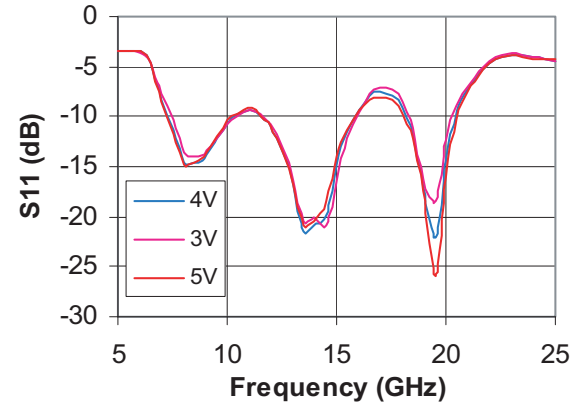


Figure 11b. Input Return Loss Over Vdd

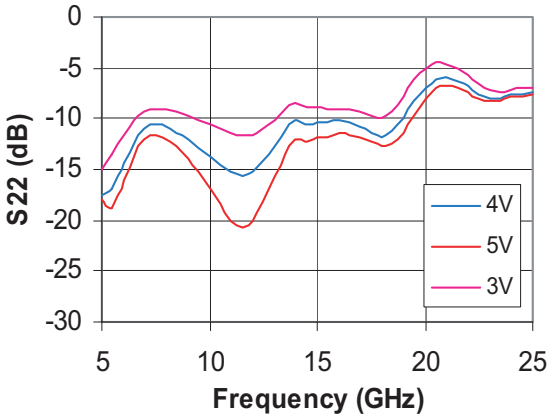


Figure 12b. Output Return Loss Over Vdd

AMMP-6222 Typical Performance for Low Current, Low Output Power Configuration (Cont)

(T_A = 25°C, Vdd=4V, Idd=95mA, Zin = Zout = 50 Ω unless noted)

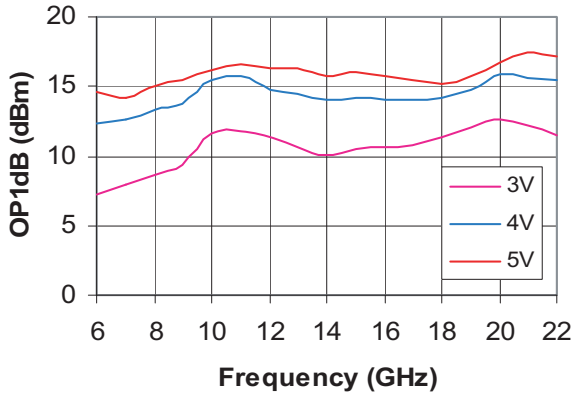


Figure 13b. Output P1dB over Vdd

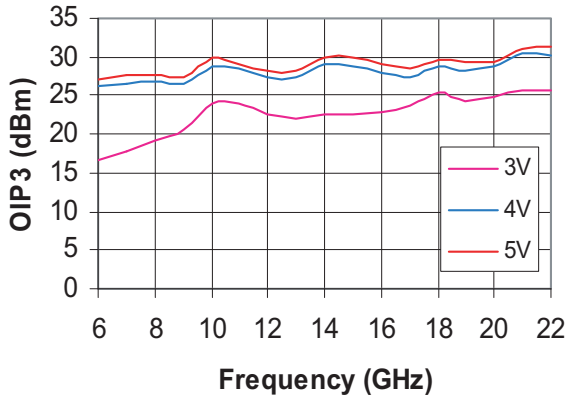


Figure 14b. Output IP3 over Vdd

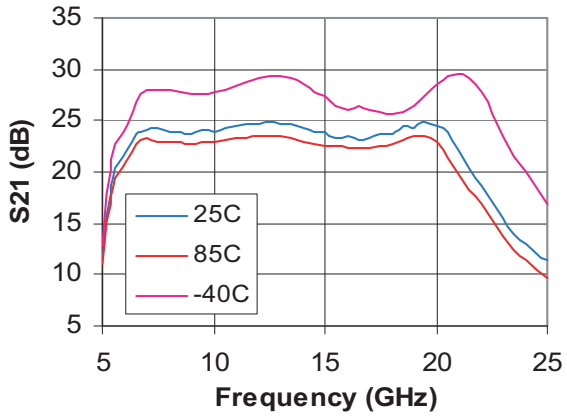


Figure 15b. Small-signal Gain Over Temp

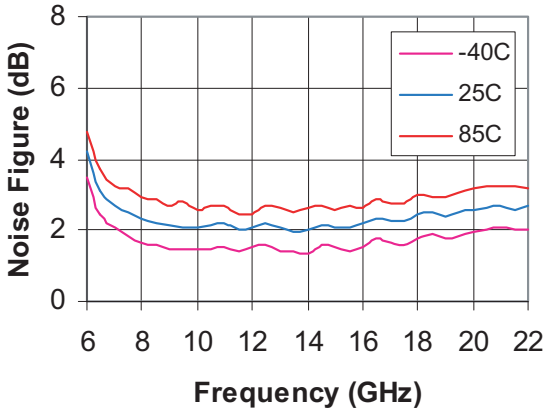


Figure 16b. Noise Figure Over Temp

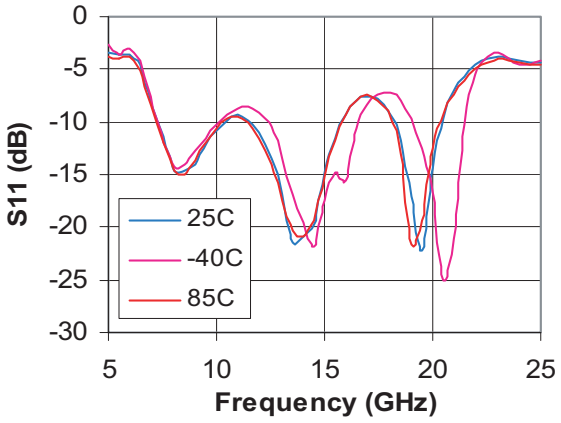


Figure 17b. Input Return Loss Over Temp

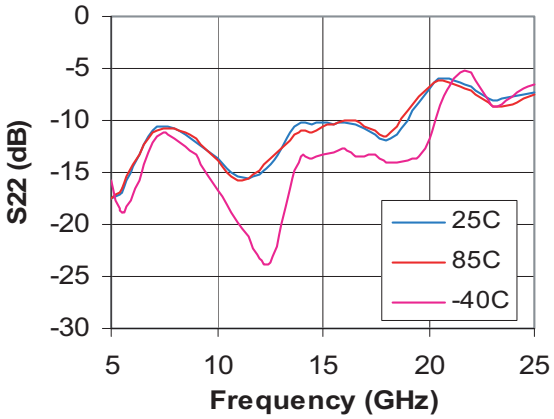


Figure 18b. Output Return Loss Over Temp

AMMP-6222 Application and Usage

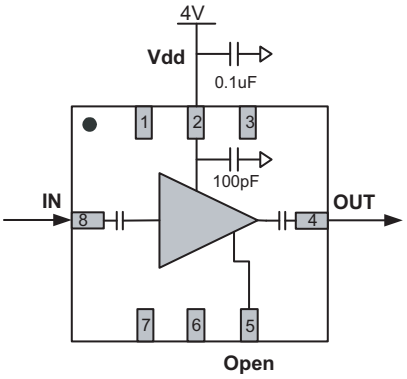


Figure 19. Low Current, Low Output Power State

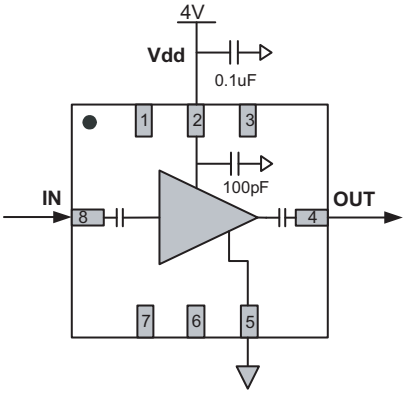


Figure 20. High Current, High Output Power State

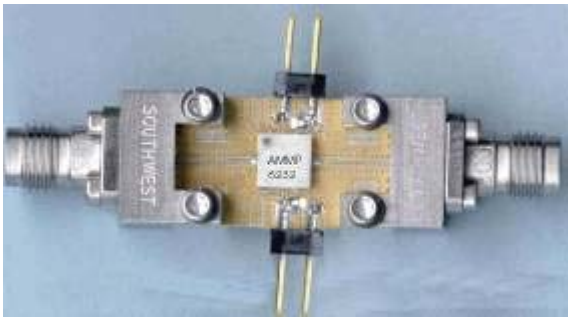


Figure 21. Evaluation/Test Board (available to qualified customer request)

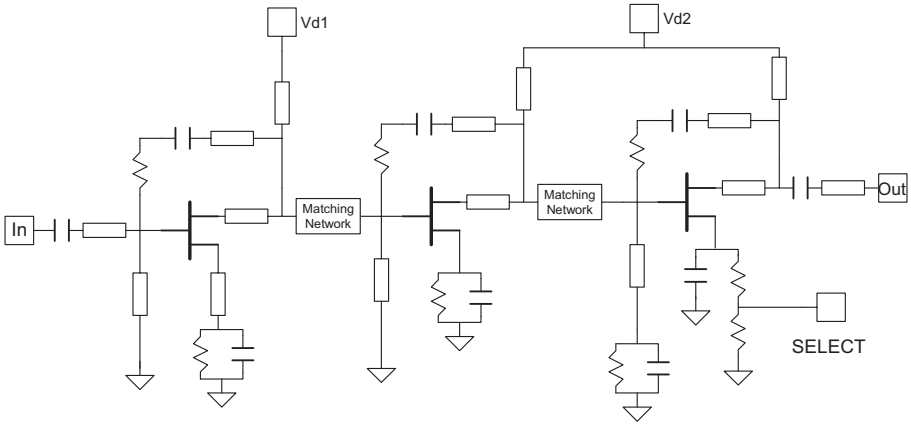


Figure 22. Simplified High Linearity LNA Schematic

Biasing and Operation

The AMMP-6222 is normally biased with a positive drain supply connected to the VDD pin through bypass capacitor as shown in Figures 19 and 20. The recommended drain supply voltage for general usage is 4V and the corresponding drain current is approximately 120mA. It is important to have 0.1uF bypass capacitor and the capacitor should be placed as close to the component as possible. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity, or low noise (Topt) matching.

For receiver front end low noise applications where high power and linearity are not often required, the AMMP-6222 can be set in low current state when pin # 5 is open as shown in Figure 19. In this configuration, the bias current is approximately 90mA, 95mA and 100mA for 3V, 4V and 5V respectively.

In applications where high output power and linearity are often required such as LO or transmitter drivers, the AMMP-6222 can be selected to operate at its highest output power by grounding pin # 5 as shown in Figure 20. At 5V, the amplifier can provide Psat of ~ 20dBm. The bias current in this configuration is 115mA, 120mA and 125mA for 3V, 4V and 5V respectively.

Refer the Absolute Maximum Ratings table for allowed DC and thermal conditions.

Recommended SMT Attachment for 5x5 Package

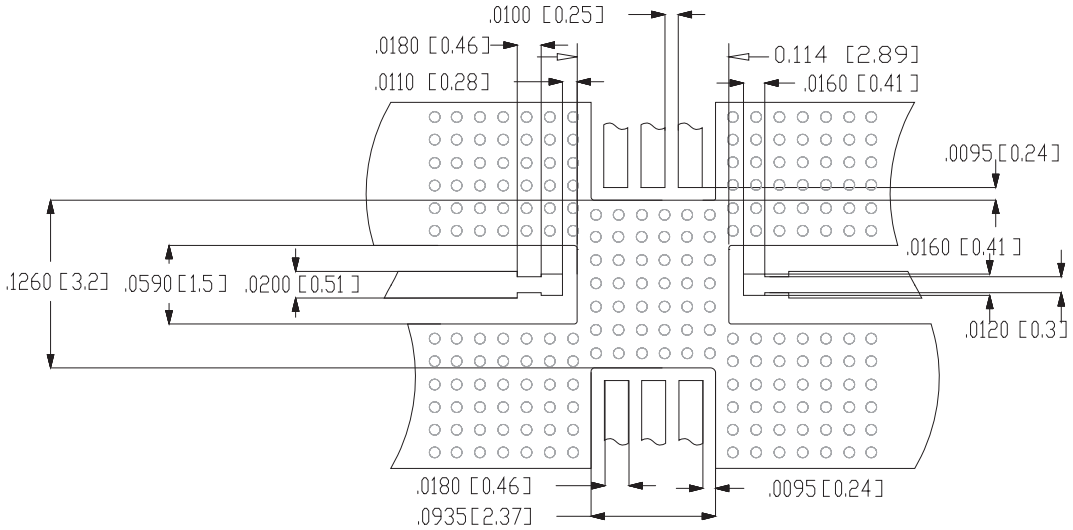


Figure 23a. Suggested PCB Land Pattern and Stencil Layout

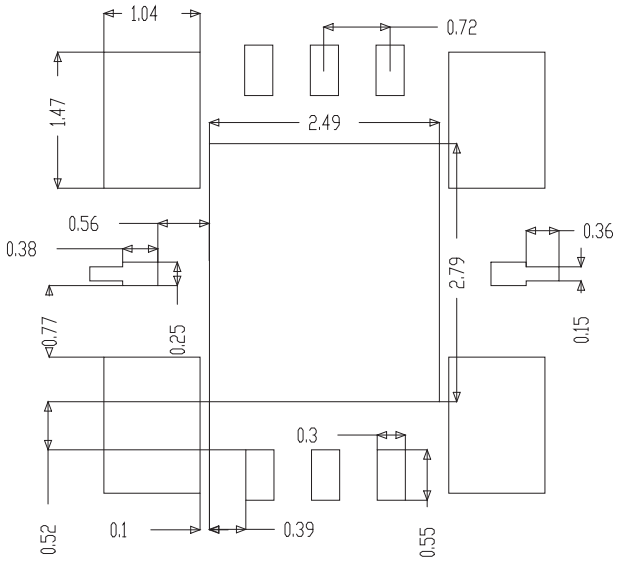


Figure 23b. Stencil Outline Drawing (mm)

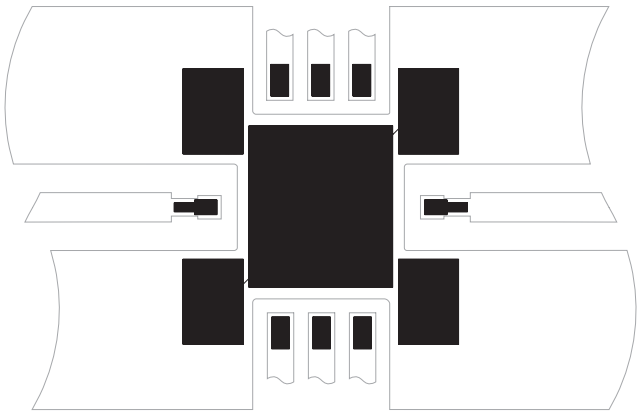


Figure 23c. Combined PCB and Stencil Layouts

The AMMP Packaged Devices are compatible with high volume surface mount PCB assembly processes.

The PCB material and mounting pattern, as defined in the data sheet, optimizes RF performance and is strongly recommended. An electronic drawing of the land pattern is available upon request from Avago Sales & Application Engineering.

Manual Assembly

- Follow ESD precautions while handling packages.
- Handling should be along the edges with tweezers.
- Recommended attachment is conductive solder paste. Please see recommended solder reflow profile. Neither Conductive epoxy or hand soldering is recommended.
- Apply solder paste using a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance.
- Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temp. to avoid damage due to thermal shock.
- Packages have been qualified to withstand a peak temperature of 260°C for 20 seconds. Verify that the profile will not expose device beyond these limits.

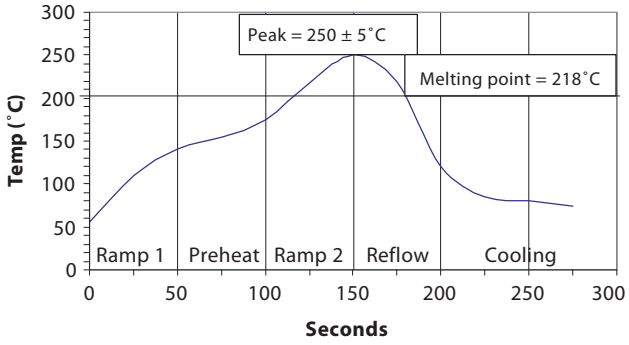


Figure 24. Suggested Lead-Free Reflow Profile for SnAgCu Solder Paste

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads. The recommended stencil layout is shown in Figure 23. The stencil has a solder paste deposition opening approximately 70% to 90% of the PCB pad. Reducing stencil opening can potentially generate more voids underneath. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use a laser cut stencil composed of 0.127mm (5 mils) thick stainless steel which is capable of producing the required fine stencil outline.

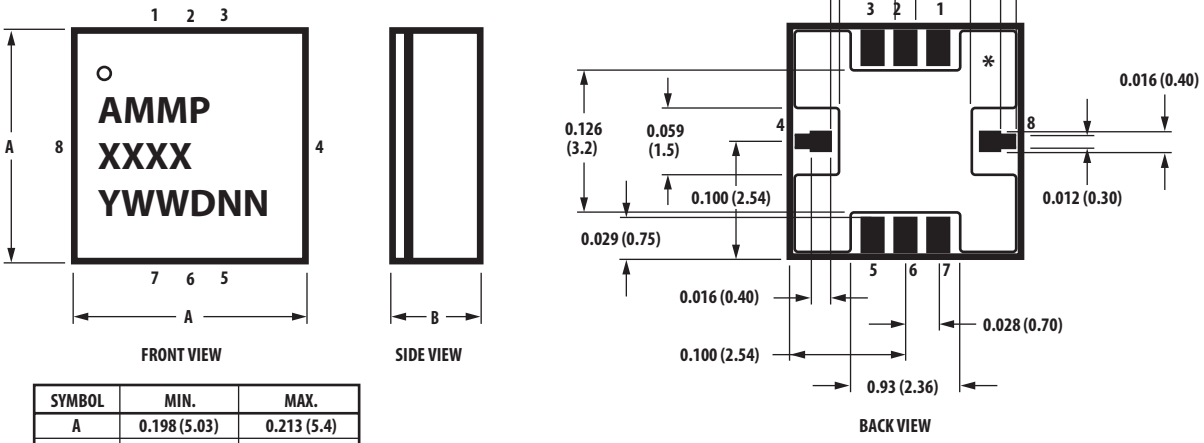
The most commonly used solder reflow method is accomplished in a belt furnace using convection heat transfer. The suggested reflow profile for automated reflow processes is shown in Figure 24. This profile is designed to ensure reliable finished joints. However, the profile indicated in Figure 14 will vary among different solder pastes from different manufacturers and is shown here for reference only.

Package, Tape & Reel, and Ordering Information

AMMP-6222 Part Number Ordering Information

Part Number	Devices Per Container	Container
AMMP-6222-BLKG	10	Antistatic bag
AMMP-6222-TR1G	100	7" Reel
AMMP-6222-TR2G	500	7" Reel

Package Dimensions



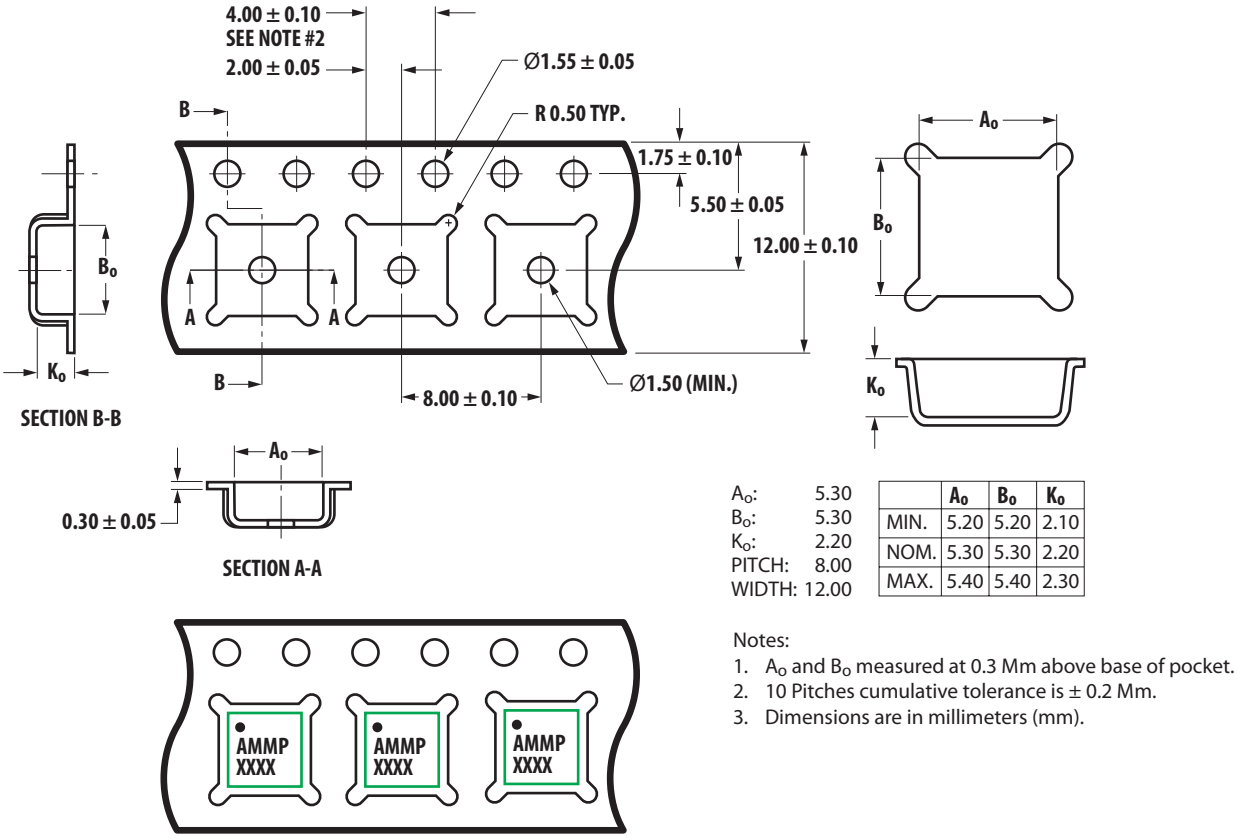
SYMBOL	MIN.	MAX.
A	0.198 (5.03)	0.213 (5.4)
B	0.0685 (1.74)	0.088 (2.25)

DIMENSIONS ARE IN INCHES (MM)

DIMENSIONAL TOLERANCE FOR BACK VIEW: 0.002" (0.05 mm)

NOTES:
1. * INDICATES PIN 1
2. DIMENSIONS ARE IN INCHES (MILLIMETERS)
3. ALL GROUNDS MUST BE SOLDERED TO PCB RF GROUND

Tape Dimensions



Ao: 5.30
Bo: 5.30
Ko: 2.20
PITCH: 8.00
WIDTH: 12.00

	Ao	Bo	Ko
MIN.	5.20	5.20	2.10
NOM.	5.30	5.30	2.20
MAX.	5.40	5.40	2.30

Notes:
1. A_o and B_o measured at 0.3 Mm above base of pocket.
2. 10 Pitches cumulative tolerance is ± 0.2 Mm.
3. Dimensions are in millimeters (mm).

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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