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RF3800

GaAs HBT PRE-DRIVER AMPLIFIER

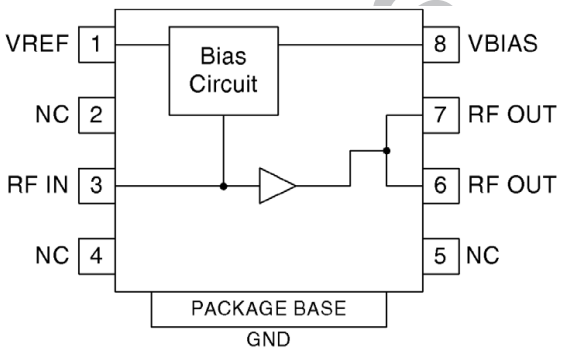
RoHS Compliant & Pb-Free Product
Package Style: AIN

Features

- 6W Output Power
- High Linearity
- >50% Efficiency
- Thermally-Enhanced AlN Packaging
- 150MHz to 960MHz Operation
- 5V to 8V Supply with Adjustable Bias

Applications

- Linear Driver
- Final Stage in Repeater Applications
- Final Stage in High Efficiency High Power Applications



Functional Block Diagram

Product Description

The RF3800 is specifically designed for use as a linear driver amplifier, as well as a high power, high efficiency output stage. Using a highly reliable GaAs HBT process, external matching allows for use in sub-bands ranging from 150MHz to 960MHz. Low thermal resistance is achieved with surface mount AlN package. Various schematics are available to address a broad range of wireless applications, as well as a standard evaluation board configured for 450MHz operation.

Ordering Information

RF3800	GaAs HBT Pre-Driver Amplifier
RF3800PCBA-416	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{CC})	9.0	V
DC Supply Current	2300	mA
Input RF Power	29	dBm
Output Load VSWR (see note)	7:1	
Maximum Operating Junction Temperature	150	°C
Maximum Current at I_{REF}	50	mA
Operating Ambient Temperature	85	°C
Storage Temperature	+125	°C

Note: For survival at OP1dB on standard 450MHz evaluation board (V_{CC}=8.0V).

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall - 450MHz					I_{REF}=16mA, V_{CC}=V_{BIAS}=V_{REF}=8V, Temp=+25°C
Frequency	450		470	MHz	
Output P1dB	37.0	38.0	39.1	dBm	
Power Added Efficiency		45		%	@ P1dB
		52		%	@ P_{SAT}
Small Signal Gain	14.0	14.7		dB	
Input Return Loss	15	20		dB	
Output Return Loss	8	12		dB	
OIP3		41		dBm	23dBm/tone
		44		dBm	26dBm/tone
		45		dBm	28dBm/tone
	46	51		dBm	30dBm/tone
		51		dBm	31dBm/tone
		50		dBm	32dBm/tone
Noise Figure		6.5		dB	
Second Harmonic		-35		dBc	@ P1dB
Third Harmonic		-50		dBc	@ P1dB
Power Control					
V_{REF}		8.0		V	To set I_{REF} at 16mA
Power Control “OFF”	0	0	0.5	V	
Power Supply					
Power Supply Voltage		8		V	
Supply Current	300	400	500	mA	V_{REF}=8V, I_{REF}=16mA
Power Down Current			10	µA	V_{REF}=0V, V_{CC}=8V

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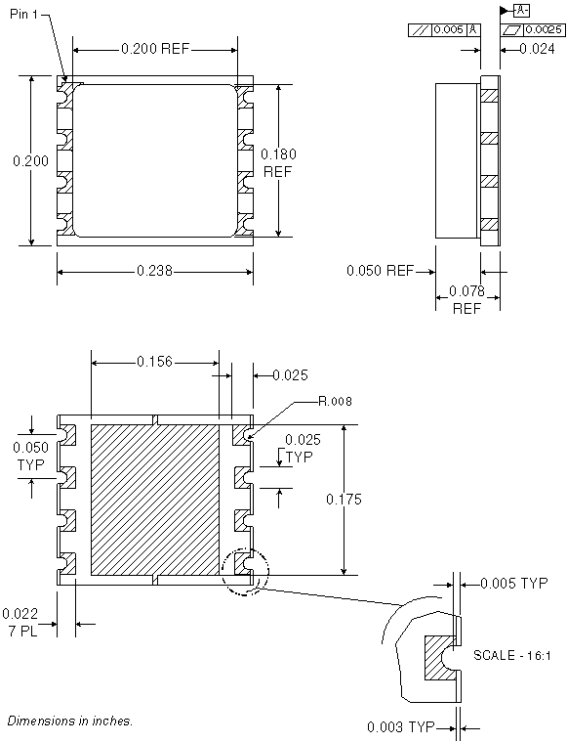
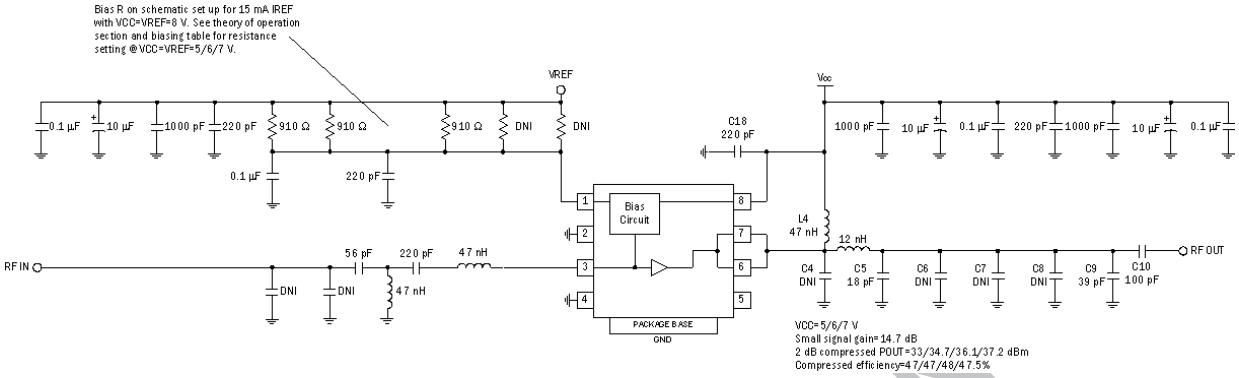
Pin	Function	Description
1	VREF	Control for active bias. See theory of operation section and biasing table for details.
2	NC	Not connected.
3	RF IN	RF input. Requires RF match and DC block.
4	NC	Not connected.
5	NC	Not connected.
6	RF OUT	RF output. Requires RF match, bias feed and DC block.
7	RF OUT	See pin 6.
8	VBIAS	Supply for active bias. Set to same voltage as V_{CC}. Tied to V_{CC} on evaluation board.
Pkg Base	GND	Backside of package should be connected to a short path to ground.

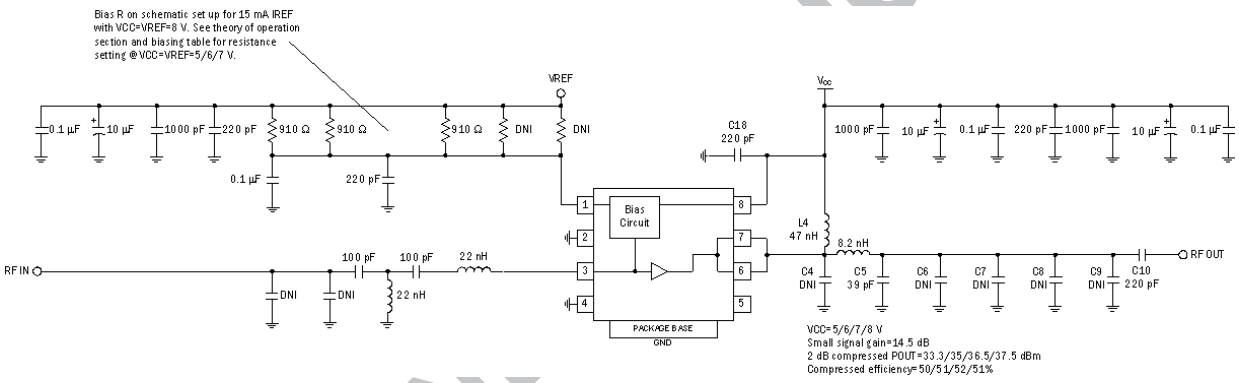
Package Drawing



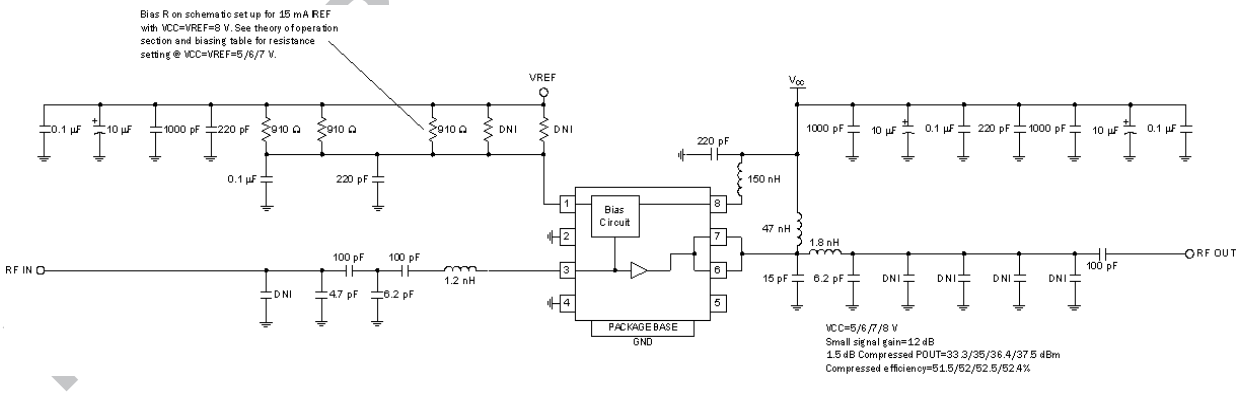
Application Schematic - 150MHz



Application Schematic - 220MHz



Application Schematic - 836MHz



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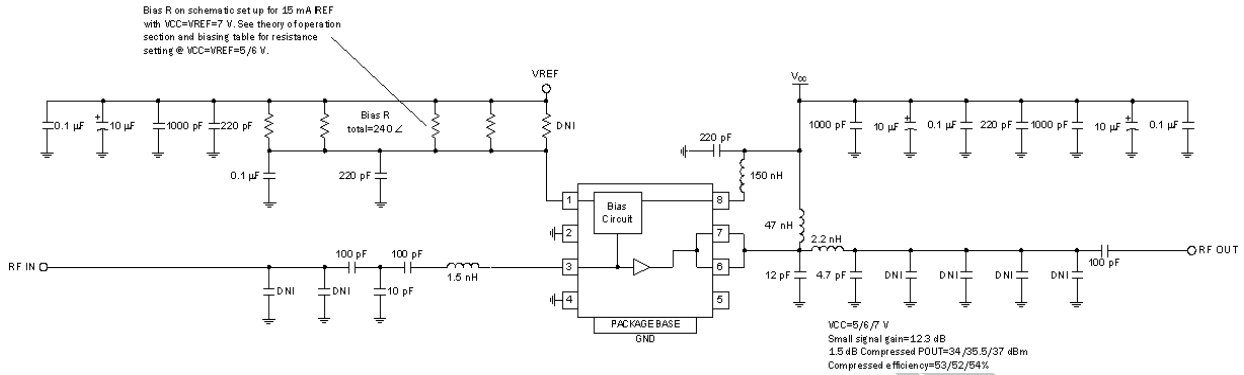
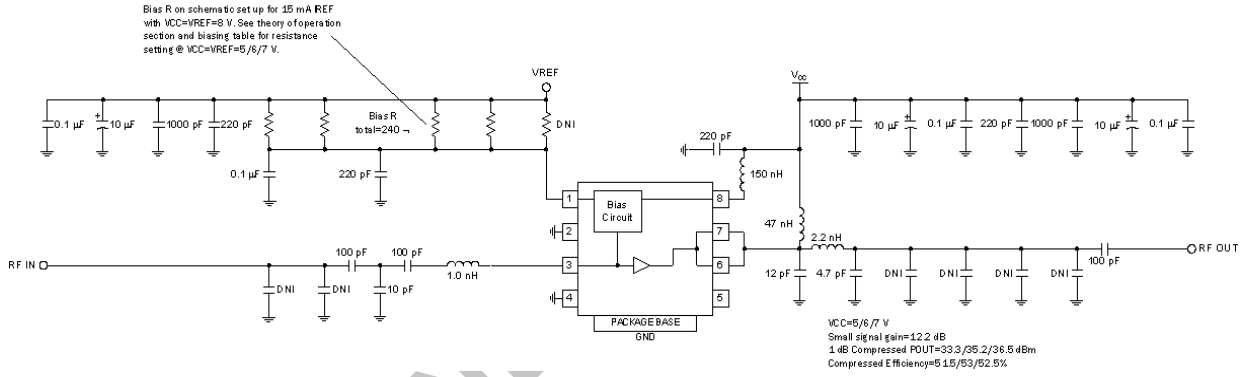
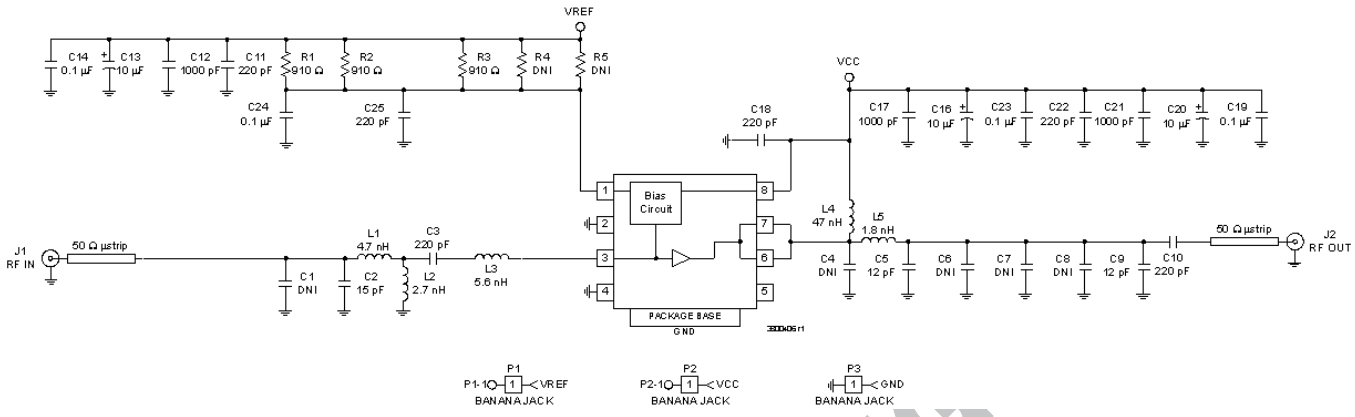
Application Schematic - 900 MHz



Application Schematic - 940 MHz



Evaluation Board Schematic - 450MHz



RF3800 Biasing Table

V_{CC}	V_{REF} Applied	V_{REF} @ Pin 1	Bias R	I_{REF}	I_{CQ}	Projected T_J @ 85°C Ambient (DC Condition)	Application
8	8	3.292	303	0.016	332	125.504	High Power
8	8	3.92	120	0.034	530	149.66	Low Power Linear
7	7	3.48	220	0.016	335	120.76125	High Power
7	7	4.582	62	0.039	556	144.353	Low Power Linear
6	6	3.53	130	0.019	365	118.3975	High Power
6	6	5.02	20	0.049	593	139.2595	Low Power Linear
5	5	3.575	75	0.019	355	112.06875	High Power
5	5	5	0	0.047	565	128.08125	Low Power Linear

Values shown for setting bias resistance on V_{REF} line, V_{CC} range 5V to 8V. Bias R set for low power linear and high power applications. In both cases, R_{TH} curves should be used to calculate/verify junction temperature is at or below 150°C. In the high power case, it is recommended that output load matching be set to achieve high efficiency, as seen within application schematic section of data sheet.

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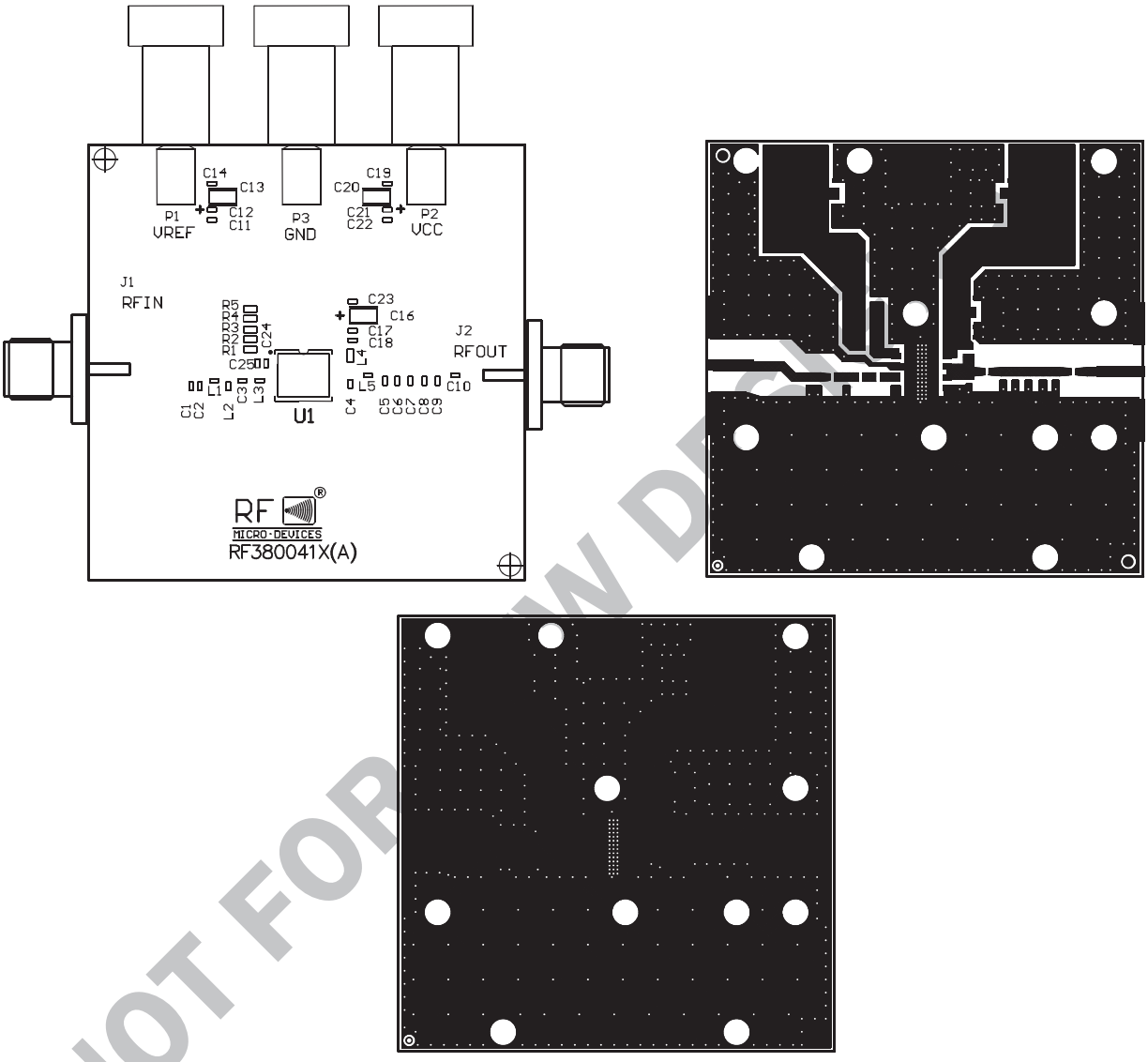
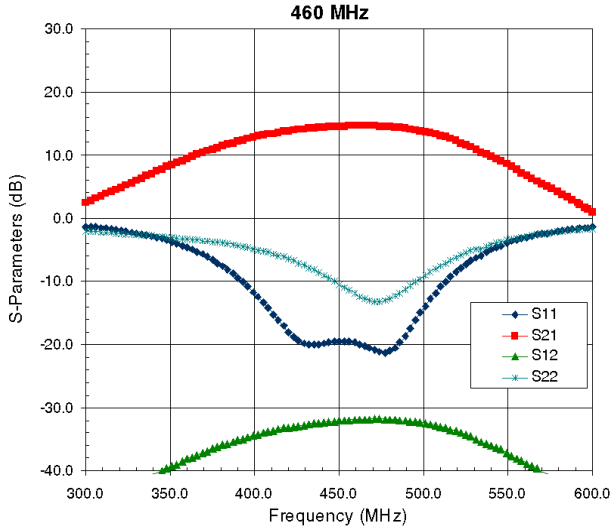
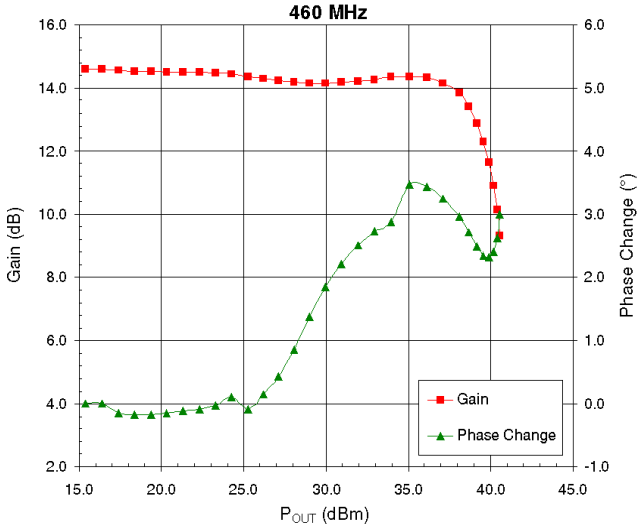
Evaluation Board Layout
Board Size 2.0” x 2.0”
Board Thickness 0.02”, Board Material Rogers 4350



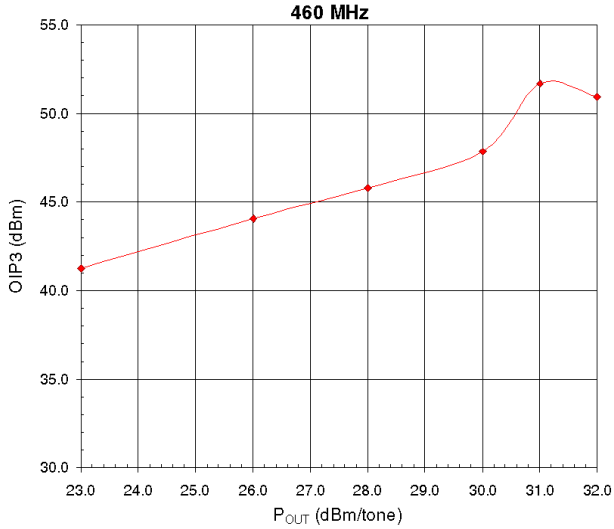
S-Parameters
460 MHz



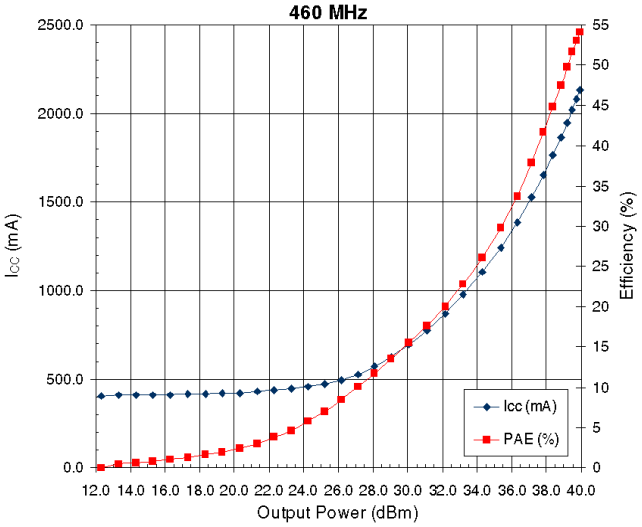
Gain and Phase versus P_{OUT}
460 MHz



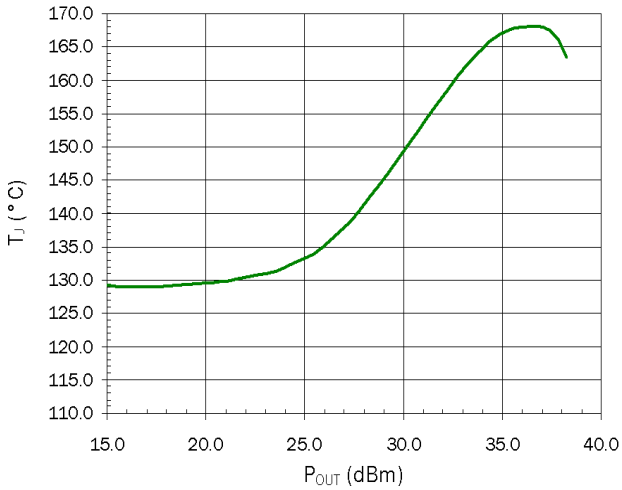
OIP3 versus P_{OUT}
460 MHz



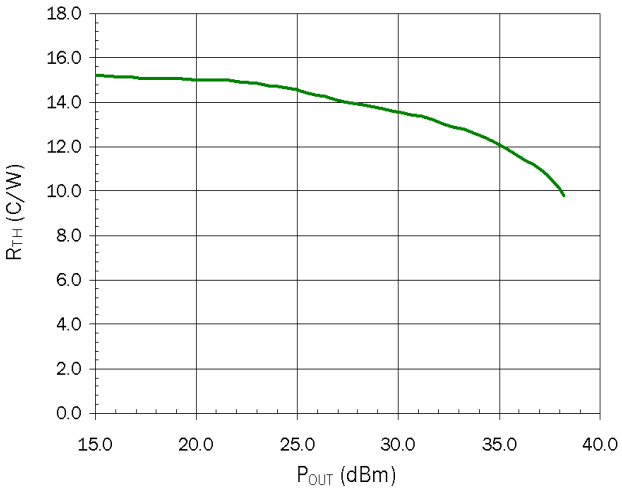
I_{CC} and Efficiency versus Output Power
460 MHz



Junction Temperature @ 85 °C Ambient
450MHz Evaluation Board



Thermal Resistance
450MHz Evaluation Board



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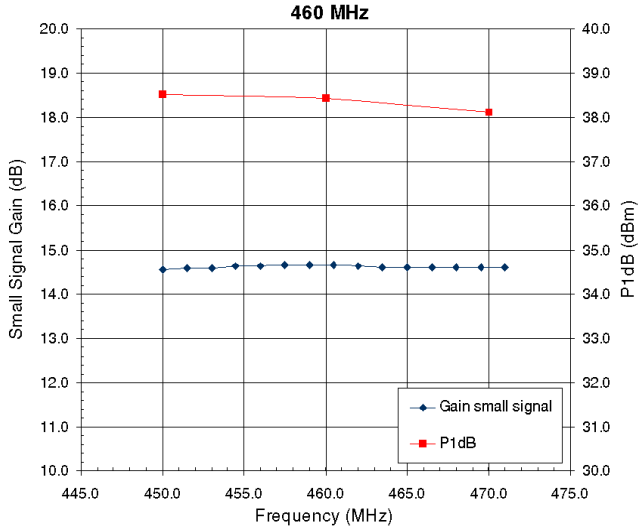
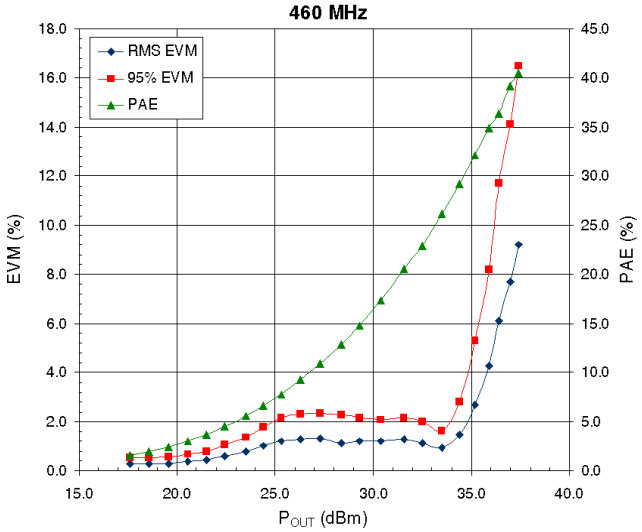
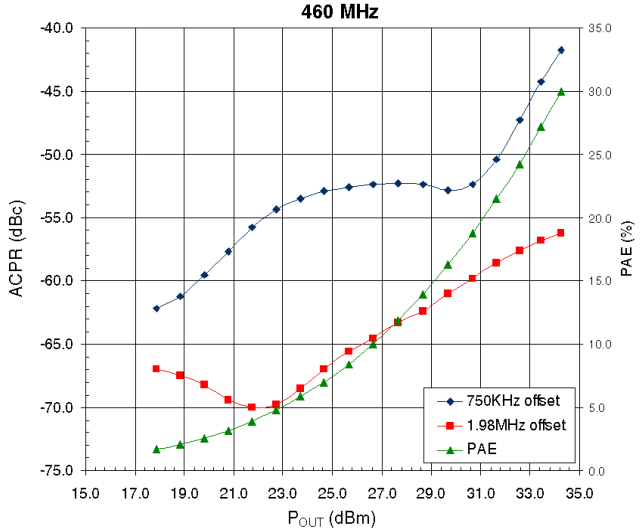
P1dB and Gain versus Frequency
460 MHz



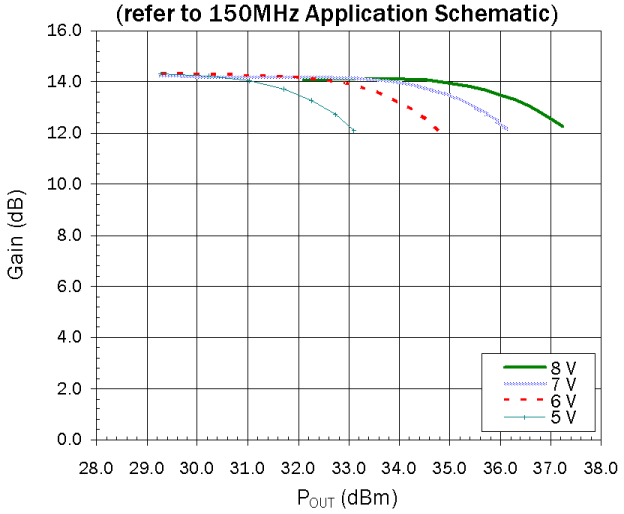
EDGE EVM
460 MHz



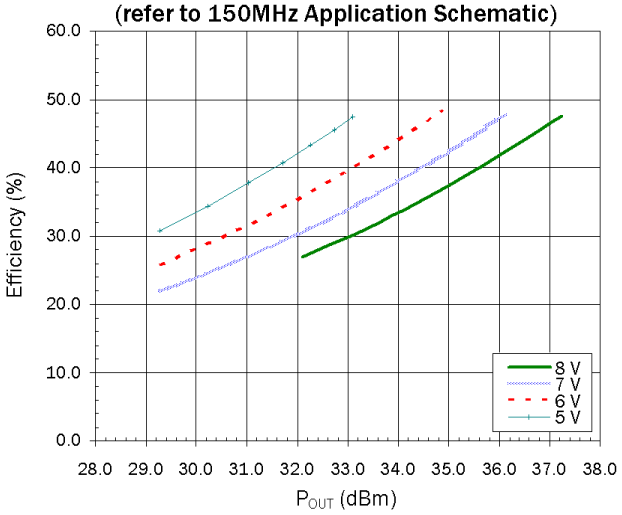
CDMA2000 Performance
460 MHz



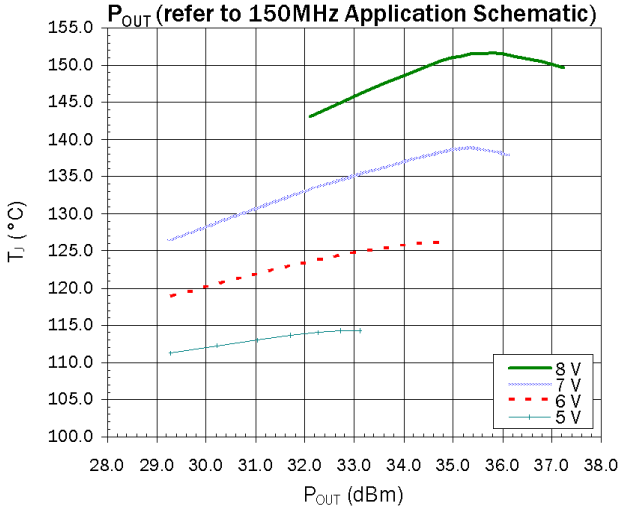
150MHz Gain versus P_{OUT}
(refer to 150MHz Application Schematic)



150MHz Efficiency versus P_{OUT}
(refer to 150MHz Application Schematic)



150MHz Projected T_J @ 85 °C Ambient versus P_{OUT} (refer to 150MHz Application Schematic)



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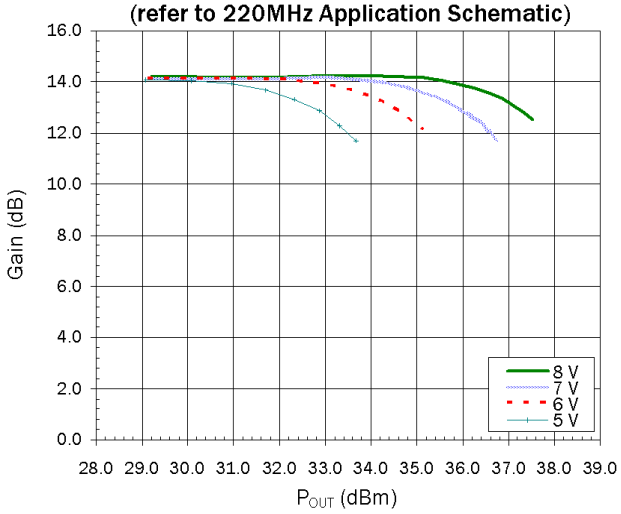
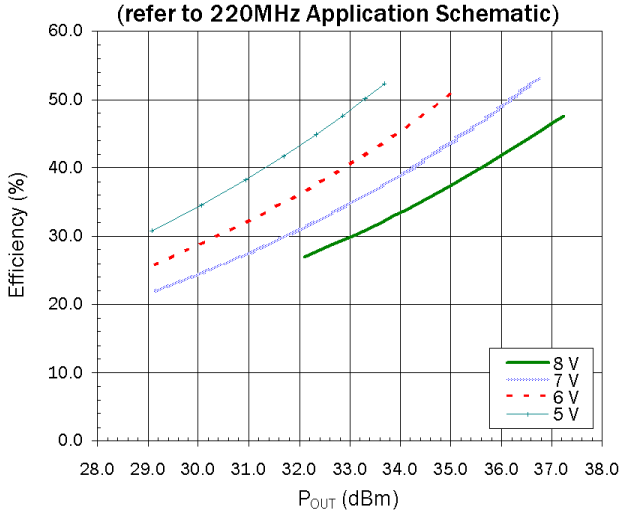
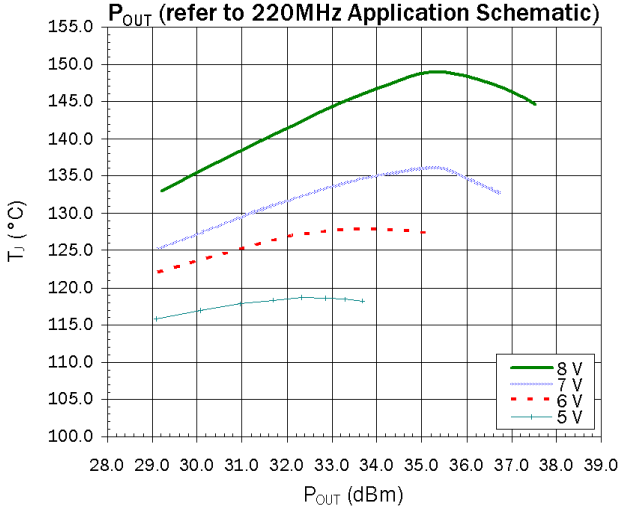
220MHz Gain versus P_{OUT}
(refer to 220MHz Application Schematic)



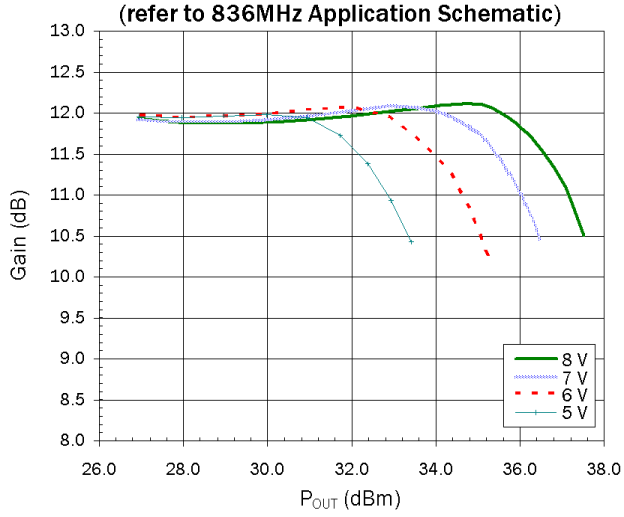
220MHz Efficiency versus P_{OUT}
(refer to 220MHz Application Schematic)



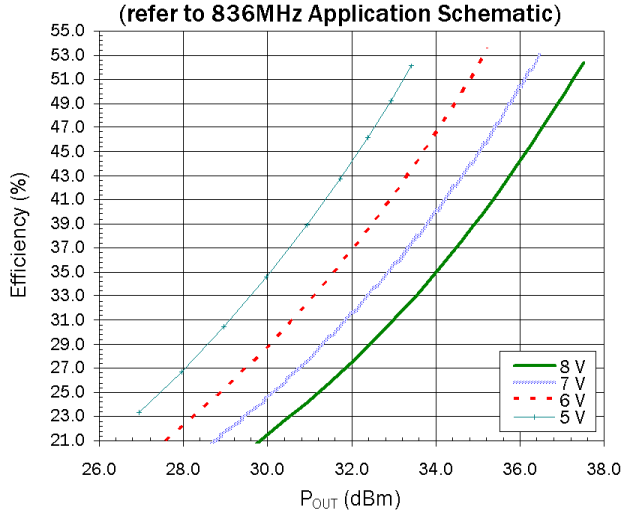
220MHz Projected T_J @ 85 °C Ambient versus
P_{OUT} (refer to 220MHz Application Schematic)



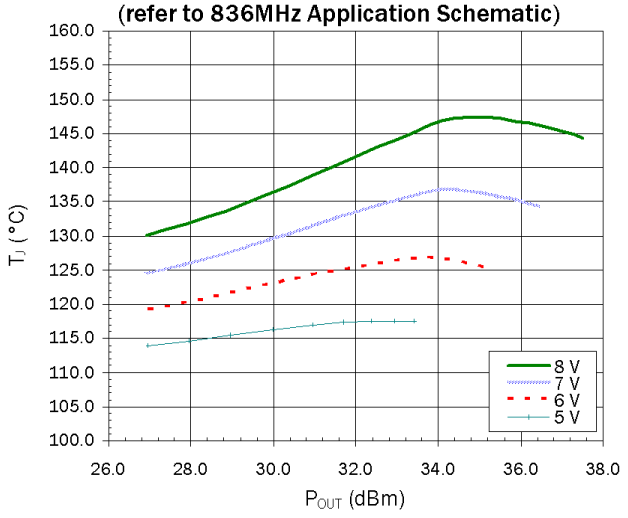
836MHz Gain versus P_{OUT}
(refer to 836MHz Application Schematic)



836MHz Efficiency versus P_{OUT}
(refer to 836MHz Application Schematic)



836 MHz Projected T_J@85 °C Ambient versus P_{OUT}
(refer to 836MHz Application Schematic)



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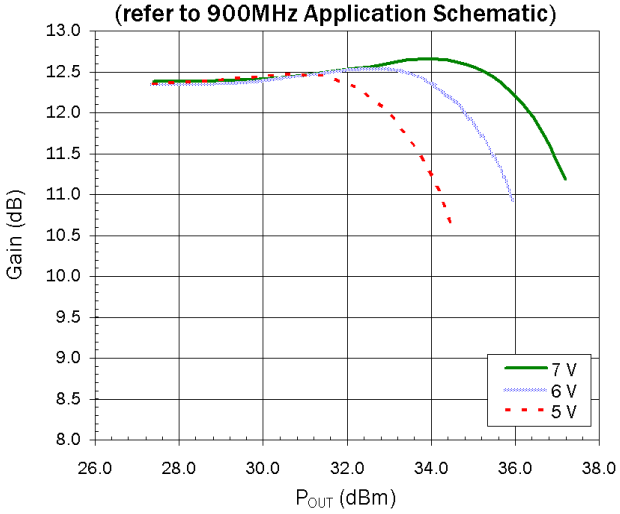
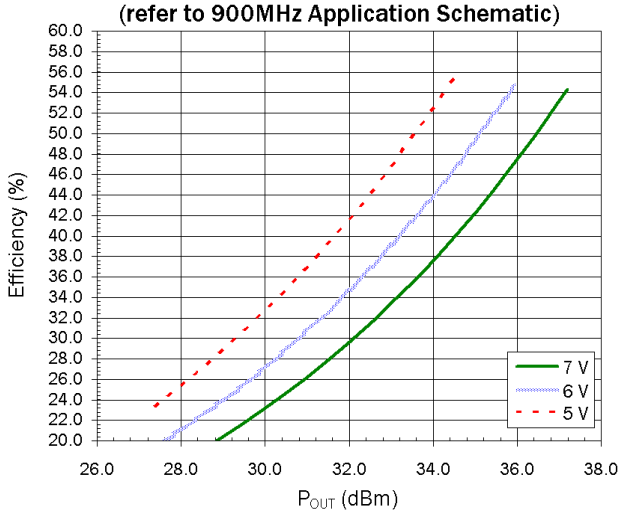
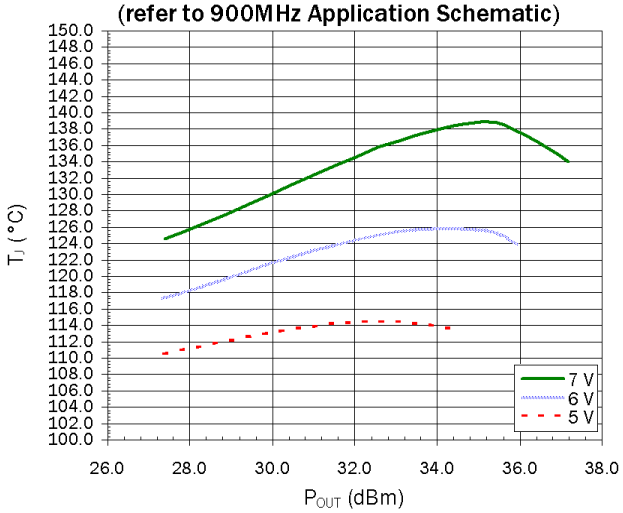
900MHz Gain versus P_{OUT}
(refer to 900MHz Application Schematic)



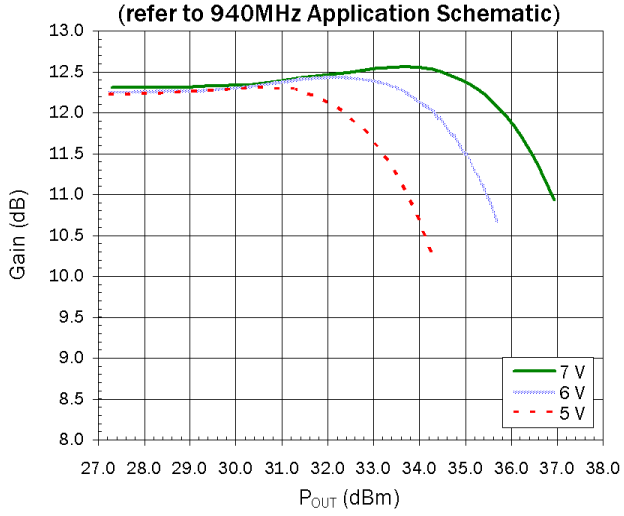
900MHz Efficiency versus P_{OUT}
(refer to 900MHz Application Schematic)



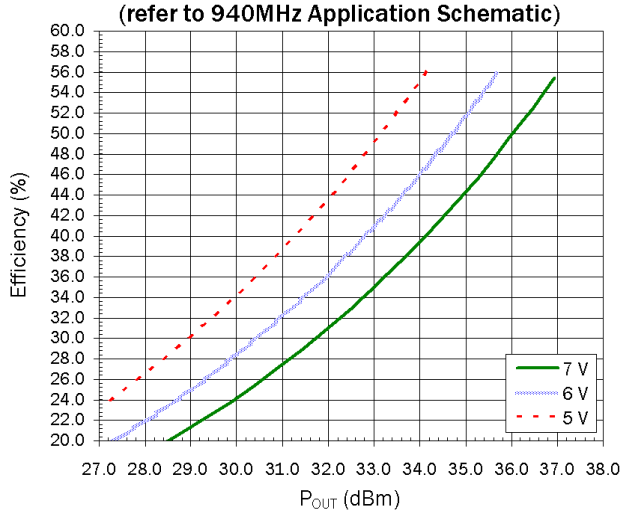
900MHz Projected T_J@85 °C Ambient versus P_{OUT}
(refer to 900MHz Application Schematic)



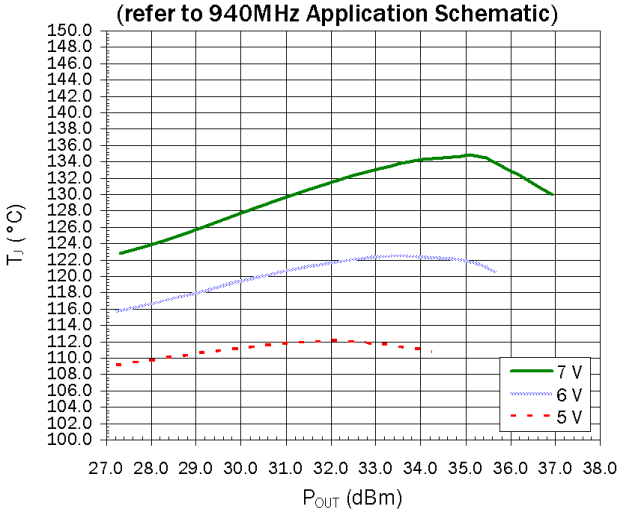
940MHz Gain versus P_{OUT}
(refer to 940MHz Application Schematic)



940MHz Efficiency versus P_{OUT}
(refer to 940MHz Application Schematic)



940MHz Projected T_J@85 °C Ambient versus P_{OUT}
(refer to 940MHz Application Schematic)



Theory of Operation

This section contains guidelines for using RF3800 in a variety of applications. Throughout this section, discussion will refer and point to supporting information elsewhere in the data sheet. Note on page 1 useable frequency range calls out 150MHz to 960MHz. Refer to information in the application schematic section for details corresponding to matches for 150MHz, 220MHz, 836MHz, 900MHz, and 940MHz. The RF3800 standard evaluation board comes matched for 450MHz. That board can be easily converted by adjustment as per application schematic of choice, where RF3800 has been impedance matched with the following approach:

1. Output load matched for efficiency, to allow for reliable operation at high Vcc/Pout.

2. Bias R shown on schematic is set for Vcc = Vref = 7/8 V, Iref = 16 mA ("7/8 V": 2 schematics show 5/6/7 V data, 3 schematics show 5/6/7/8 V data). Bias R adjust is required to obtain same Iref when lower Vcc = Vref is used (detailed discussion found later in this section). In graph section of data sheet, find curves corresponding to each application schematic, for 5/6/7 (5/6/7/8) V operation.

I_{REF}=16mA is the nominal setting for case where power amplifier is intended for use at P_{OUT}>27dBm. In this scenario, self biasing of RF3800 will provide linearity for operation below OP1dB. In backed off applications requiring maximum linearity, bias R can be adjusted for higher I_{REF}/I_{CQ}. In these, as with all cases, attention should be paid to maintaining junction temperature (T_J)<150°C, taking into account the worse case ambient for the application. In graph sections contained herein, curves for projected T_J versus P_{OUT} are included. Thermal resistance (R_{TH}) curve is also provided, which shows R_{TH} versus P_{OUT} (data taken on 450MHz evaluation board). This curve defines R_{TH}_total=RF3800 R_{TH}_jc + R_{TH}_eval board. R_{TH}_eval board=1°C/W. As such, R_{TH}_total from curve can be used as a conservative value for RF3800 R_{TH}_jc, with case defined at GND slug of package.

When adjusting bias R at V_{REF} to obtain desired I_{REF}/I_{CQ} for a given $V_{CC}=V_{REF}$, refer to data sheet biasing table. Given bias points provided, those not found in the table can be obtained as per this example. Assume a low power, linear application at the following conditions:

V_{CC}=6V
Frequency=940MHz
P_{OUT}=20dBm
I_{CQ}=580mA

Nominal data sheet biasing condition=$V_{CC}=V_{REF}$=8V, with bias R=300Ω. The evaluation board in this discussion shows I_{REF}=16mA, I_{CQ}=332mA. The task is to change bias R such that I_{CQ}=580mA with $V_{CC}=V_{REF}$=6V. To obtain a starting point bias R value, do the following:

1. With board as is (bias R set for 8 V), adjust V_{CC} to 6V, and V_{REF} such that I_{CQ}=580mA. At this condition: V_{CC}=6V, V_{REF}=18.8V, I_{REF}=46mA, I_{CQ}=577mA.

2. Now, calculate voltage at V_{REF} pin given the above condition:

a. $V_{REF\_PIN}=V_{REF}-I_{REF}$*bias R=18.8-(0.046)*(300)=5.0V

3. Calculate bias R which will yield same I_{REF} and V_{REF_PIN} with V_{REF}=6V:

a. bias R=$(V_{REF}-V_{REF\_PIN})/I_{REF}$=(6-5.0)/0.046=21.7Ω.

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4. As mentioned above, initial calculation was to determine starting point bias R. Refining by trial and error and using standard R values yielded the following:

a. bias R=20Ω

b. $V_{CC}=V_{REF}=6V$

c. $I_{REF}=49mA$

d. $I_{CQ}=593mA$

e. $V_{REF\_PIN}=5.02V$

Note that I_{REF} is just within limit of 50mA called out in max ratings table on page 2. Measured data for this example, 940MHz evaluation board set up for 6V linear operation at 20dBm output power:

P_{OUT}=20dBm
OIP3=47.5dBm
Gain=12dB
OP1dB=33.8dBm

In comparison to 940MHz data in application schematics section, we see lower gain and OP1dB. The reason for this delta is a slightly different output match was used: 4.7pF shunt output capacitor was changed to 5.6pF for enhanced OIP3. This shows the importance of output load impedance in each application. The application schematic match was intentionally set for high OP1dB and efficiency, while the above case was geared for backed off linearity.

As mentioned above, one factor to keep in mind when increasing bias for low power linearity would be consideration of junction temperature, T_J. This becomes more critical as V_{CC} is increased. As an exercise to demonstrate, use data sheet curves to approximate T_J at 85°C ambient for above 940MHz, 20dBm example:

Dissipated power at 20dBm=$P_{DISS}=V_{CC}*I_{CC}-P_{OUT}=6*0.593-0.1=3.458W$. From data sheet R_{TH} versus P_{OUT} curve, we see $R_{TH}=14.7°C/W$. Thus, at 85 deg C ambient, $T_J=85+3.458*14.7=135.8°C$.

When matching RF3800 for a unique frequency not addressed in the data sheet, the following methodology has been proven effective:

1. Small signal s-parameters can be obtained from RFMD applications/sales. Using s2p data, matching topology/values at input/output can be determined. This via simple Smith Chart matching, or simulation software.

2. Once acceptable small signal response is obtained, the match is evaluated for target specs:

a. Gain

b. Compression point

c. Linearity requirement

d. Efficiency and projected junction temperature at corresponding output power.

3. Output match optimization can now take place, such that specification compliance is achieved.

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PCB Design Requirements

PCB Surface Finish

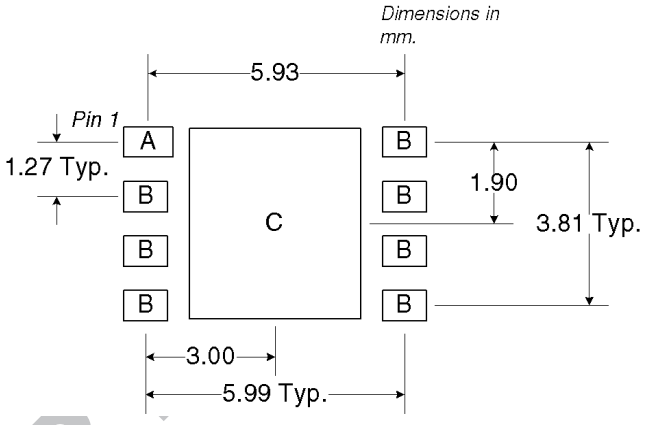
The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for PFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land Pattern

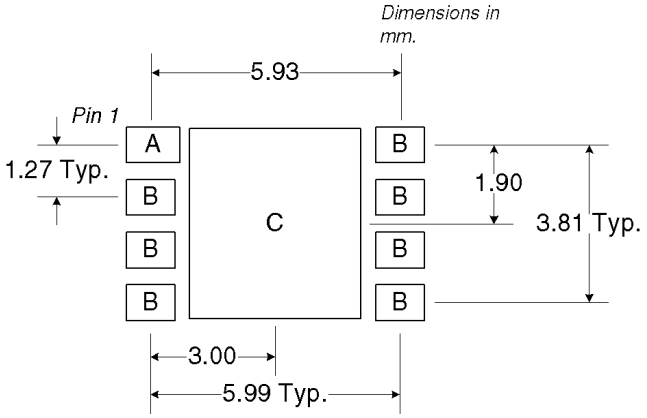
A = 1.14 x 0.71
B = 1.02 x 0.71 Typ.
C = 3.96 x 4.44



PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

A = 1.30 x 0.86
B = 1.17 x 0.86 Typ.
C = 4.11 x 4.60



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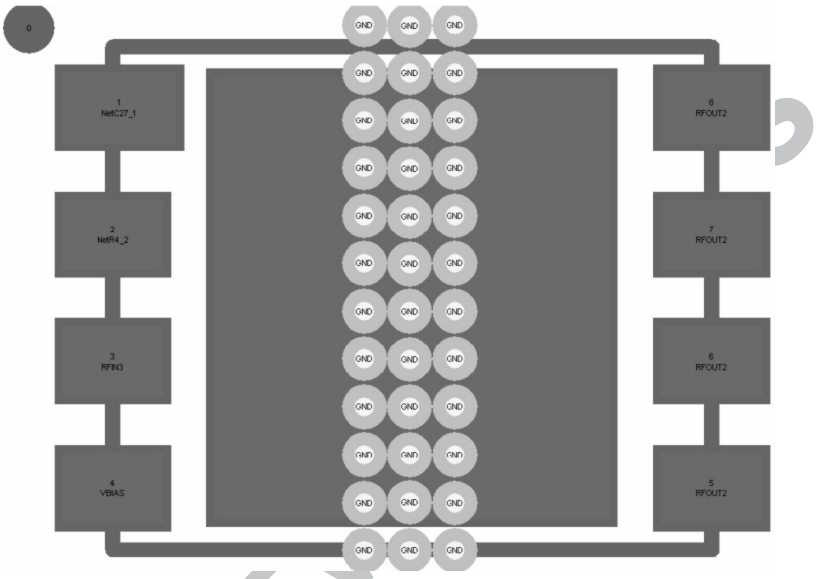
Thermal Pad and Via Design

The DUT must be connected to the PCB backside ground through a low inductance, low thermal resistance path. The required interface is achieved with the via pattern shown below for both low inductance as well as low thermal resistance. The footprint provided below worked well on the RFMD 20mil thick Rogers 4350 PCB and also standard FR4. The vias are 8mil vias that are partially plated through and are finished to 8mils±2mils with a minimum plating of 1.5mil. Failure to place these vias within the DUT mounting area on the PCB in this prescribed manner may result in electrical performance and/or reliability degradation.



Tape and Reel Information

Carrier tape basic dimensions are based on EIA481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the boyd and the solder terminals from damaging stresses. The individual pocket design can vary from vendor to vendor, but wide and pitch will be consistent.

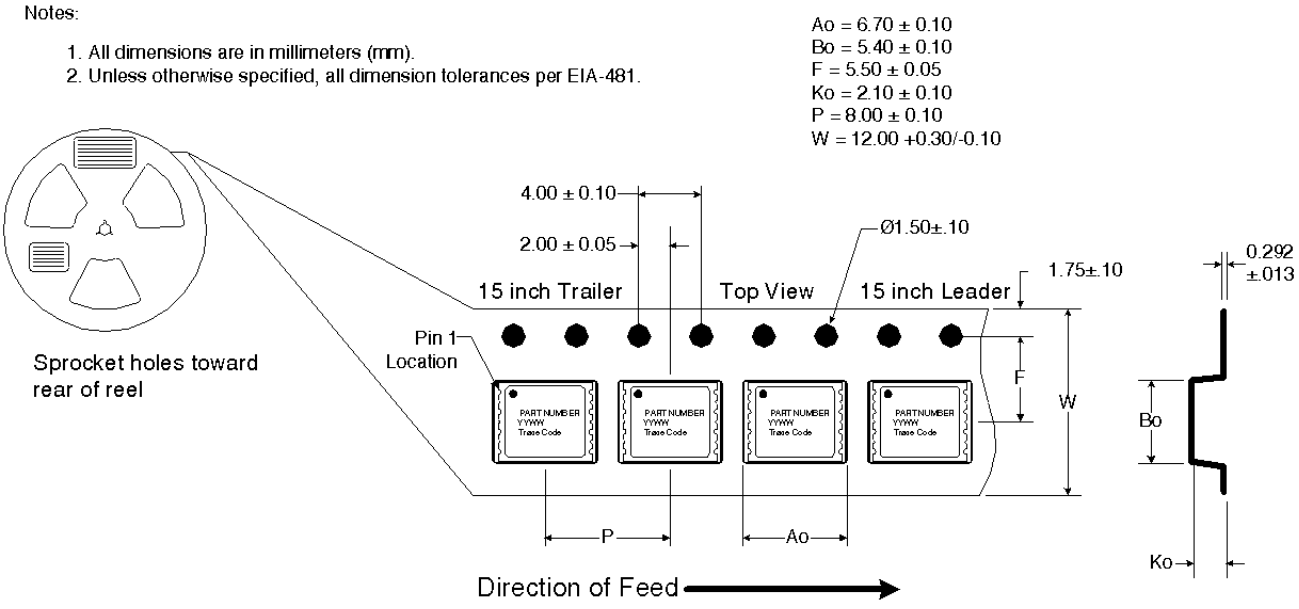
Carrier tape is wound or placed on a shipping reel with a diameter of either 330mm (13inches) or 178mm (7inches). The center hub design is large enough to ensure the radius formed by the carrier tape around it does not put unnecessary stress on the parts.

Prior to shipping, moisture sensitive parts (MSL level 2a to 5a) are baked and placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier, ESD bag, which is placed in a cardboard shipping box. It is important to note that unused moisture sensitive parts need to be resealed in the moisture barrier bag. If the reels exceed the exposure limit and need to be rebaked, most carrier tape and shipping reels are not rate as bakeable at 125°C. If baking is required, devices may be baked according to section 4, table 4-1, column 8 of Joint Industry Standard IPC/JEDECJ-STD-033A.

The following table provides useful information for carrier tape and reels used for shipping the devices described in this document.

RFMD Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units per Reel
RF3800TR13	13 (330)	4 (102)	12	8	Single	2500
RF3800TR7	7 (178)	2.4 (61)	12	8	Single	750

Carrier Tape Drawing with Part Orientation



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RoHS* Banned Material Content

RoHS Compliant:	yes
Package total weight in grams (	0.137
Compliance Date Code:	N/A
Bill of Materials Revision:	Rev B
Pb Free Category:	e4

Bill of Materials	Parts Per Million (PPM)					
	Pb	Cd	Hg	Cr VI	PBB	PBDE
Die	0	0	0	0	0	0
Molding Compound	0	0	0	0	0	0
Lead Frame	0	0	0	0	0	0
Die Attach Epoxy	0	0	0	0	0	0
Wire	0	0	0	0	0	0
Solder Plating	0	0	0	0	0	0

This RoHS banned material content declaration was prepared solely on information, including analytical data, provided to RFMD by its suppliers, and applies to the Bill of Materials (BOM) revision noted above.

* DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment

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