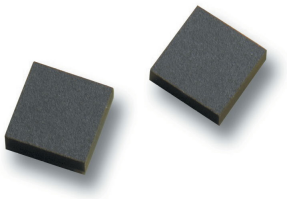
ACPM-7833

CDMA1900 (PCS) Power Amplifier Module

Data Sheet



Description

The ACPM-7833 is a fully matched CDMA Power amplifier module. Designed around Avago Technologies' new Enhancement Mode pHEMT process, the ACPM-7833 offers premium performance in a very small form factor. Fully matched to 50 Ohms on the input and output.

The amplifier has excellent ACPR and efficiency performance at max Pout and low quiescent current with a single bias control voltage. For even lower quiescent current, a dynamic bias control circuit can be used by varying the voltage on the Vcntl pin between 1.2V to 2.5V.

Designed in a surface mount RF package, the ACPM-7833 is cost and size competitive.

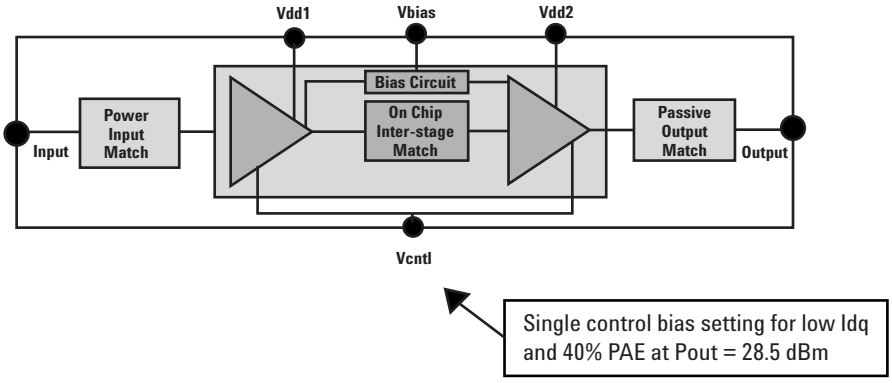
The ACPM-7833 is another key component of the Avago Technologies CDMAdvantage RF chipset.

Features

- Operating frequency: 1850– 1910 MHz
- 28.5 dBm linear output power @ 3.4V
- High efficiency: 40% PAE
- Dynamic bias control for low midpower Idd
- Very low quiescent current with single control voltage
- Internal 50 ohm matching networks for both RF IN/OUT
- 3.2– 4.2V linear operation
- cdma2000 1xRTT capable
- Only 3 SMT parts needed
- 4.0 x 4.0 x 1.1 mm SMT package

Applications

- CDMA handsets
- Datacards
- PDAs



Maximum Ratings[1]

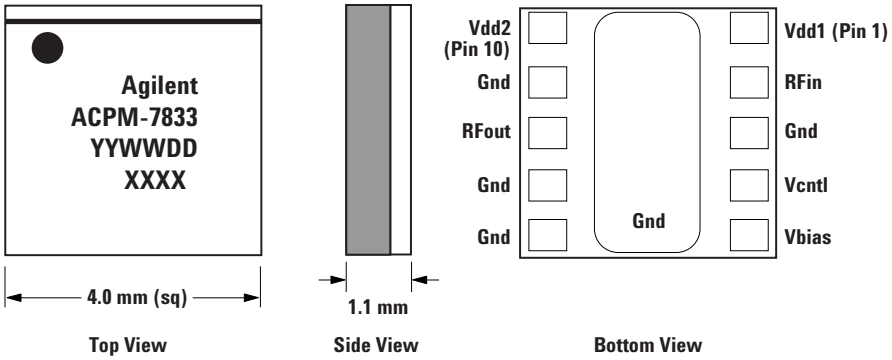
Parameter	Min.	Max.
Vdd Supply Voltage		6.0 V
Power Dissipation [2]		2.5 W
Bias Current		1.5 A
Control Voltage (Vcntl)		3.0 V
Amplifier Input RF Power		10 dBm
Junction Temperature		+150°C
Storage Temperature (case temperature)	-40°C	+100°C

Notes:
1. Operation of this device in excess of any of these limits may cause permanent damage.
2. Tcase = 25°C

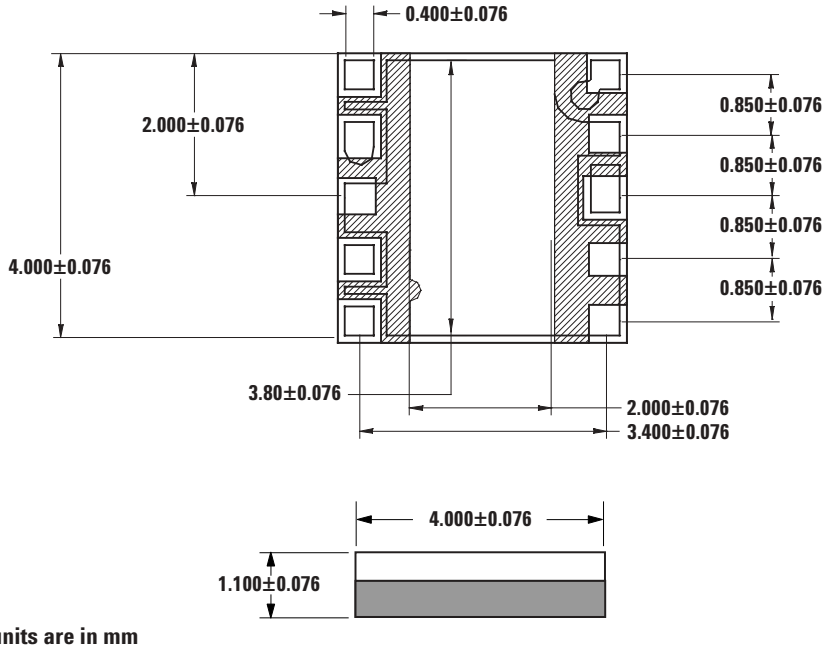
Thermal Resistance[2] θ_{jc} = 22.3°C/W

Recommended operating range of Vdd = 3.2 to 4.2 V, Ta = -30 to +85°C

Package Marking and Dimensions



Note:
YYWWDD: year – work week – day
XXXX: lot code



All units are in mm

Electrical Characterization Information

All tests are done in 50Ω system at Vdd1=Vdd2=Vbias = 3.4V, 25°C, unless noted otherwise.

Parameter	Units	Min	Typ	Max	Comments
PCS CDMA					
Frequency Range	MHz	1850		1910	
Gain (Fixed Cntl Voltage)					
P_{out} = 28.5 dBm	dB	25.5	27.5	29.5	Vcntl= 2.5V
P_{out} = 16 dBm		24	26	28	Vcntl= 1.8V
Power Added Efficiency					
P_{out} = 28.5 dBm	%	38	40		Vcntl= 2.5V
P_{out} = 16 dBm	%	7.5	8.5		Vcntl= 1.8V
Total Supply Current	mA mA mA		520 135 31	550 156	P_{out} = 28.5 dBm, Vcntl= 2.5V P_{out} =16 dBm, Vcntl= 1.8V P_{out} = -5 dBm, Vcntl = 1.2V
ACPR @ ± 1.25 MHz offset	dBc/30 kHz	-45	-48		P_{out} - 28.5 dBm
ACPR @ ± 1.98 MHz offset	dBc/30 kHz	-53	-55		P_{out} - 28.5 dBm
Quiescent Current	mA mA mA		62 47 25	80 60	P_{out} - 28.5 dBm, Vcntl= 2.5V Vcntl = 1.8V Vcntl = 1.2V
Vcntl Current	mA		2.0	2.7	Vcntl = 2.5V
Input VSWR (P_{out} = 28.5 dBm)			2.0:1		
Noise Figure	dB		4.5		
Noise Power @ 80 MHz offset in 1930–1990 MHz	dBm/Hz		-141	-138	
Stability (Spurious): Load VSWR 5:1	dBc	-50			All phases
Harmonic Suppression: 2Fo	dBc	-30	-38		

Typical Performance, data measured in 50Ω system, Vdd1=Vdd2=Vbias = 3.4V, Vcntl = 2.5V, T = 25°C and Freq = 1880 MHz unless noted otherwise.

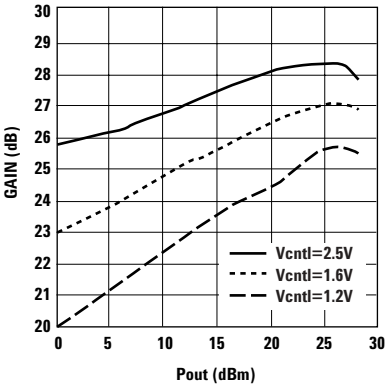


Figure 1. Gain vs. Pout.

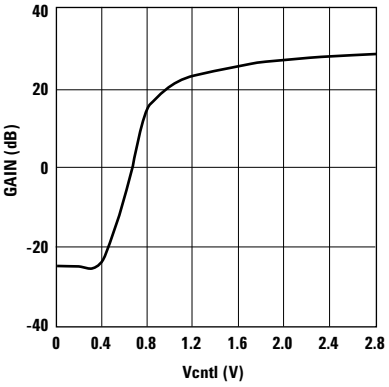


Figure 2. Gain vs. Vcntl.

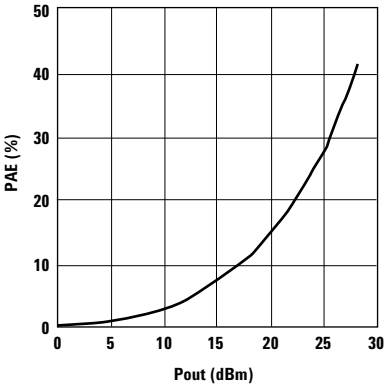


Figure 3. PAE vs. Pout.

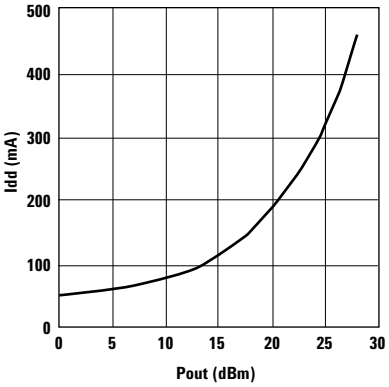


Figure 4. Idd vs. Output Power.

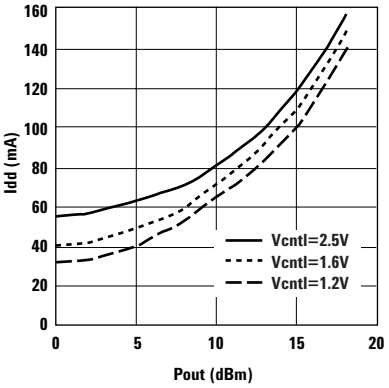


Figure 5. Idd vs. Output Power.

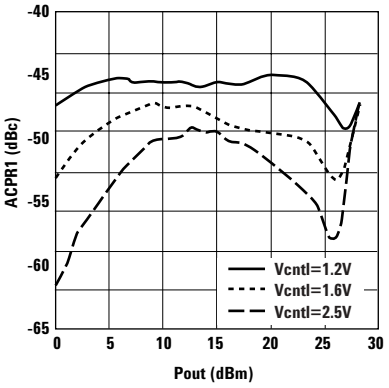


Figure 6. ACPR (1.25 MHz offset) vs. Pout.

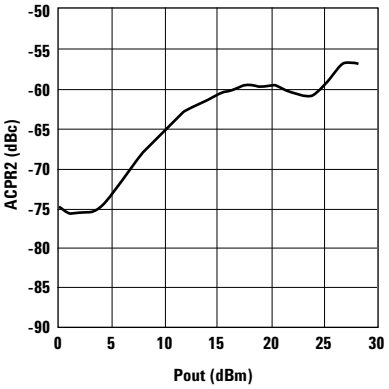


Figure 7. ACPR (1.98 MHz offset) vs. Pout.

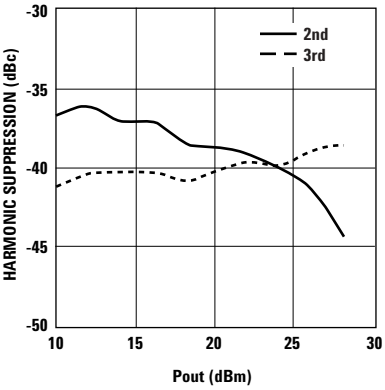
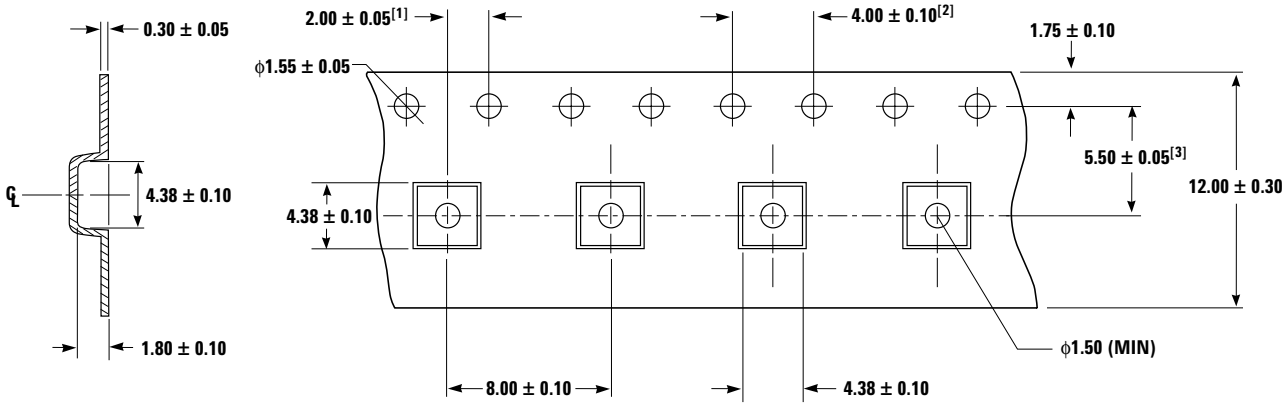


Figure 8. 2nd/3rd Harmonics vs. Pout.

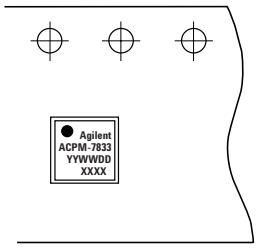
Ordering Information

Part Number	No. of Devices	Container
ACPM-7833-BLK	10	Bulk
ACPM-7833-TR1	1000	7″ Tape and Reel

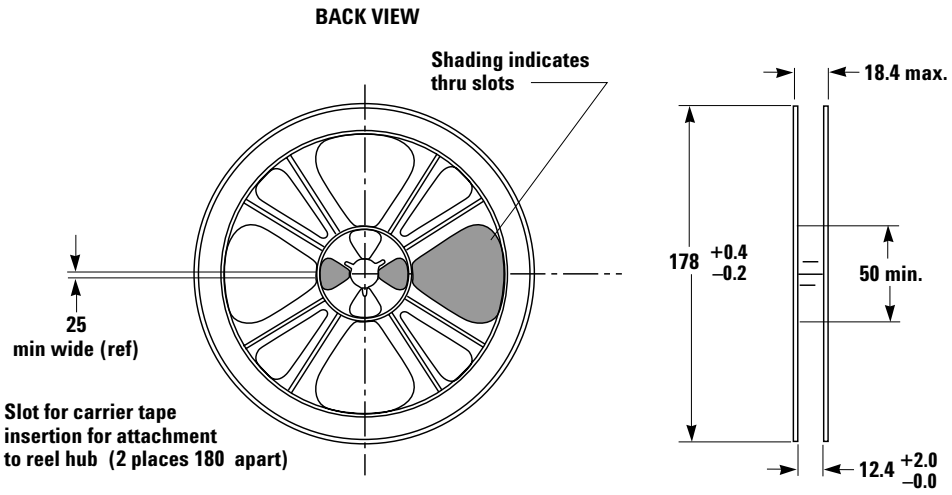
Tape Dimensions and Orientation

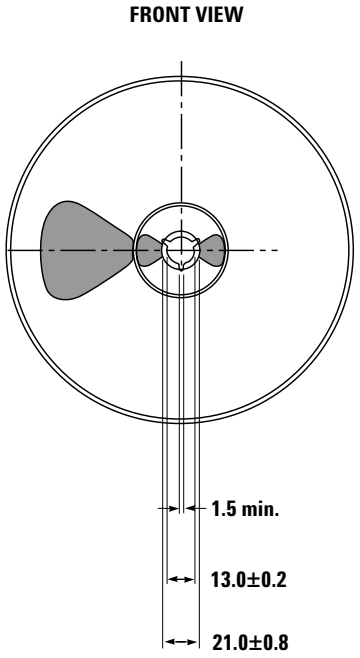


Notes:
1. Measured from centerline of sprocket hole to centerline of pocket
2. Cumulative tolerance of 10 sprocket holes is ±0.2 mm
3. All dimensions in millimeters unless otherwise stated.



Reel Drawing





NOTES:

1. Reel shall be labeled with the following information (as a minimum).
   a. manufacturers name or symbol
   b. Avago Technologies part number
   c. purchase order number
   d. date code
   e. quantity of units
2. A certificate of compliance (c of c) shall be issued and accompany each shipment of product.
3. Reel must not be made with or contain ozone depleting materials.
4. All dimensions in millimeters (mm)

Application Information

The following material is presented to assist in general design and use of the APCM-7833.

- 3.0V Characterization, for use in Data Card Applications
- cdma2000 1XRTT Description and Characterization data
- Design tips on various methods to control the bias on Vcntl pin
- Description of ACPR measurement methods
- Description of Avago Technologies evaluation demoboard for ACPM-7833
- IR Reflow Profile (applicable for all Avago Technologies E-pHEMT PAs)

3.0V Characterization, Data Card Applications

Electrical Data

All tests are done in 50Ω system at Vdd1=Vdd2=Vbias = 3.0V, 25°C, unless noted otherwise.

Parameter	Units	Min	Typ	Max	Comments
1900 MHz CDMA					
Frequency Range	MHz	1850		1910	
Gain (Fixed Cntl Voltage)					
(P_{out} = 28.5 dBm)	dB		26		Vcntl = 2.5V
(P_{out} = 13 dBm)	dB		28		Vcntl = 2.5V
(P_{out} = -5 dBm)	dB		28		Vcntl = 2.5V
Power Added Efficiency					
P_{out} = 28.0 dBm	%		42		Vcntl = 2.5V
P_{out} = 16 dBm	%		8.5		Vcntl = 2.5V
Total Supply Current	mA		500		P_{out} = 28.0 dBm, Vcntl= 2.5V
			100		P_{out} = 13 dBm, Vcntl= 1.6V
			30		P_{out} = -5 dBm, Vcntl= 1.2V
ACPR @ ± 1.25 MHz offset	dBc/30 kHz		-43		P_{out} - 28.5 dBm
ACPR @ ± 1.98 MHz offset	dBc/30 kHz		-56		P_{out} - 28.5 dBm
Quiescent Current	mA		60		P_{out} - 28.5 dBm, Vcntl = 2.5V
Input VSWR					
(P_{out} = 28.5 dBm)			2.0:1		
(P_{out} = 16 dBm)			2.5:1		
Noise Figure	dB		4.5		
Noise Power @ 80 MHz offset in 1930 - 1990 MHz	dBm/Hz		-141		
Stability (Spurious): Load VSWR 5:1	dBc		-50		All phases
Harmonic Suppression					
2Fo	dBc		-40		
3Fo	dBc		-40		

Typical Performance, data measured in 50Ω system, Vdd1=Vdd2=Vbias = 3.0V, Vcntl = 2.5V, T = 25°C and Freq =1880 MHz.

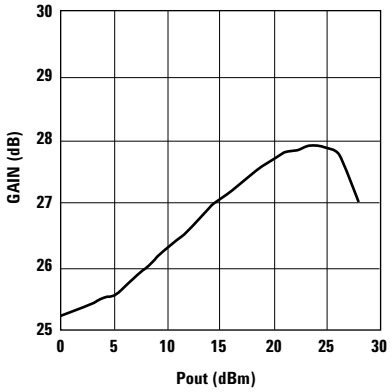


Figure 9. Gain vs. Pout.

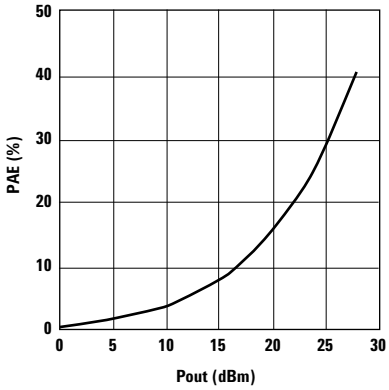


Figure 10. PAE vs. Pout.

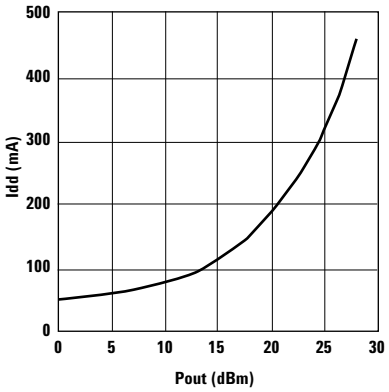


Figure 11. Idd vs. Pout.

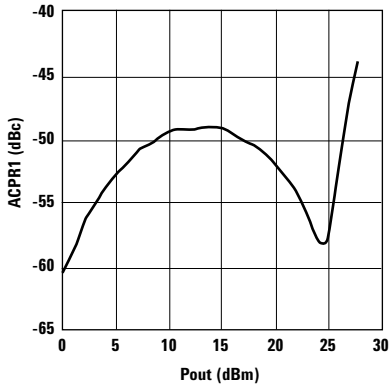


Figure 12. ACPR (1.25 MHz offset) vs. Pout.

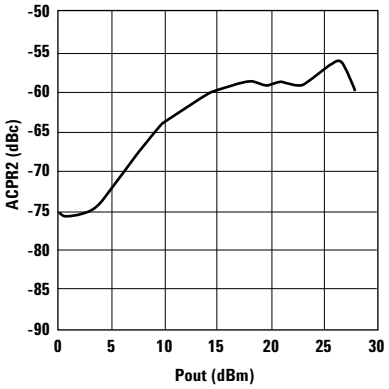


Figure 13. ACPR (1.98 MHz offset) vs. Pout.

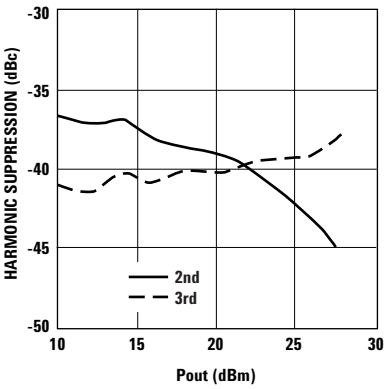


Figure 14. Harmonic Suppression vs. Pout.

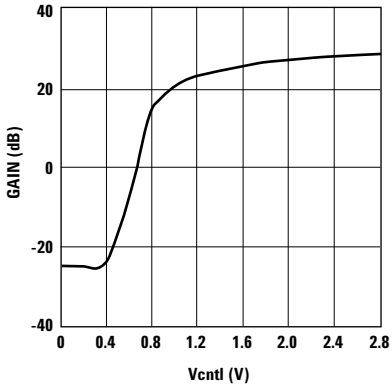


Figure 15. Gain vs. Vcntl.

cdma 2000 1xRTT Characterization

System Description

CDMA2000 is the TIA's standard for third generation (3G) technology and is an evolution of the IS-95 CDMA format. CDMA2000 includes 1X RTT in the single-carrier mode and 3X RTT in the multi-carrier mode. This paper describes the CDMA2000 1X RTT approach and its performance with Avago Technologies 4x4 CDMA PAs, ACPM-7833. CDMA2000 1X RTT, being an extension of the IS-95 standard, has a chip rate of 1.2288Mchip/s. However, in 1xRTT, the reverse link transmits more than one code channel to accommodate the high data rates. The minimum configuration consists of a reverse pilot (R-Pilot) channel for synchronous detection by the Base Transceiver System (BTS) and a reverse fundamental channel (R-FCH) for voice. Additional channels such as the reverse supplemental channels (R-SCHs) and the reverse dedicated channel (R-DCCH) are used to send data or signaling information. Channels can exist at different rates and power levels.

Table 1 shows the transmitter specification in CDMA2000 reverse link.

Table 1. Transmitter Specification in Reverse Link.

Specification		Spread Rate1
ERP at Maximum Output Power		Lower limit +23 dBm Upper limit +30 dBm
Minimum Controlled Output Power		-50 dBm/1.23 MHz
Waveform Quality Factor and Frequency Accuracy		>0.944
	SR1, Band Class 0(Cellular band)	SR1, Band Class1(PCS band)
Spurious Emission at Maximum RF output power offset frequency within the range	885 kHz to 1.98 MHz Less stringent of -42 dBc/30 kHz or -54 dBm/1.23 MHz	1.25 MHz to 1.98 MHz Less stringent of -42 dBc/30 kHz or -54 dBm/1.23 MHz
	1.98 MHz to 3.125 MHz Less stringent of -54 dBc/30 kHz or -54 dBm/1.23 MHz	1.98 MHz to 2.25 MHz Less stringent of -50 dBc/30 kHz or -54 dBm/1.23 MHz
	3.125 MHz to 5.625 MHz -13 dBm/100 kHz	2.25 MHz to 6.25 MHz -13 dBm/1 MHz

Typical channel configurations below are based on the transmitter test condition in the reverse link.

1) "Basic" Voice only configuration
   - R-PICH @ -5.3 dB
   - R-FCH @ -1.5 dB 9.6 kbps

2) Voice and Data configuration
   - R-PICH @ -5.3 dB
   - R-FCH @ -4.54 dB 9.6 kbps
   - R-SCH1 @ -4.54 dB 9.6 kbps

3) Voice and Control configuration
   - R-PICH @ -5.3 dB
   - R-FCH @ -3.85 dB 9.6 kbps
   - R-DCCH @ -3.85 dB 9.6 kbps

4) Control channel only configuration
   - R-PICH @ -5.3 dB
   - R-DCCH @ -1.5 dB 9.6 kbps

Combinations of these channels will increase the peak to average power ratio for higher data rates. The complementary cumulative distribution function (CCDF) measurement characterizes the peak to average power statistics of CDMA2000 reverse link. For reference, the system specifications of peak to average power ratio of IS-95 and CDMA2000 IX RTT are 3.9 dB and 5.4 dB at 1% CCDF respectively.

Higher peak to average power ratio requires a higher margin, both in higher power gain and in improved thermal stability for PA linearity to meet the minimum system specifications.

The test results below for the ACPM-7833 show the compliance to the system linearity specifications with 4 channel configurations, representing a broad cross-section of CDMA2000 1X RTT environments.

Test result of ACPM-7833 using CDMA2000 1X RTT signal

Test condition - PA Evaluation board with Vdd1=Vdd2=Vbias = 3.4V, Vcntl = 2.5V, Frequency = 1880 MHz.
Test result with each channel configuration.

Channel	IVdd(mA)	Pin(dBm)	1.25 MHz ACPR(dBc)	1.25 MHz ACPR(dBc)	-1.98 MHz ACPR(dBc)	+1.98 MHz ACPR(dBc)	Pout(dBm)
Basic	451.0	-0.14	-52.6	-51.5	-60.2	-60	28
Voice+Data	435.0	0.52	-46.2	-45.7	-58.0	-58.3	28
Voice+Cntl	439.0	0.50	-45.5	-44.9	-60.1	-60	28
Cntl only	299.0	-2.56	-49.1	-48.8	-57.7	-57.5	25.5

EIA/TIA-98-D indicates a 2.5 dB allowed back off in power for control channel only configuration.

Peak to average power ration (Pout = 16 dBm)

CCDF(%)	Basic	Voice + Data	Voice + CNTL	CNTL only
10	2.11	3.37	3.44	4.00
1	3.74	4.83	5.21	5.75
0.1	4.68	5.68	6.24	6.73
0.01	5.15	6.20	6.76	7.18
0.001	5.36	6.53	7.11	7.39
0.0001	5.48	6.63	7.17	7.45

Design Tips to use Vcntl pin

Power Amplifier Control Using Vcntl Pin on ACPM-7833

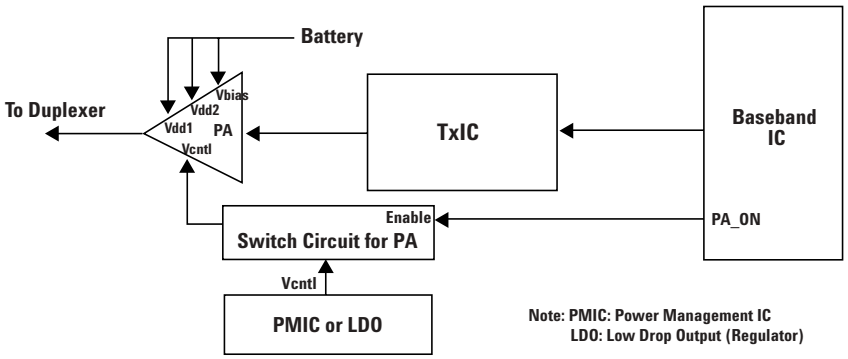
Power amplifier control scheme in CDMA systems is one of the important and challenging aspects of CDMA-based handset design. Handset designers must balance maintaining adequate linearity while optimizing efficiency at high, medium and low output power levels. The primary method to achieve these goals is to adjust the bias of the PA as a function of output power. Theoretically, the best efficiency would be achieved when the bias of the PA is continually adjusted based on the output power requirement of the PA. However, implementing this type of circuit can be complex and costly. Therefore several different approaches have been developed to provide an acceptable trade-off between optimum efficiency and optimum manufacturability. This application section reviews four methods of controlling the bias of a CDMA power amplifier: fixed, step, logical and dynamic.

1. Fixed Bias Control

Using a fixed bias point on the PA is the traditional method, and it is the simplest. For example, the recommended value of the fixed control voltage on the Vcntl pin for the ACPM-7833 is 2.5V. The Vcntl pin on the PA is controlled by PA_ON pin of the baseband IC. When PA_ON is HIGH, the output RF signal of the PA is enabled, enabling the subscriber unit to transmit the required data. The switch circuit also controls the on/off state of the PA.

Below is an example of how to control the the output of the PA using PA_ON and Vcntl pins.

Power Mode	PA_ON	Vcntl	Power Range
Shut Down	LOW	0V	—
High Power	HIGH	2.5V	- 28.5 dBm

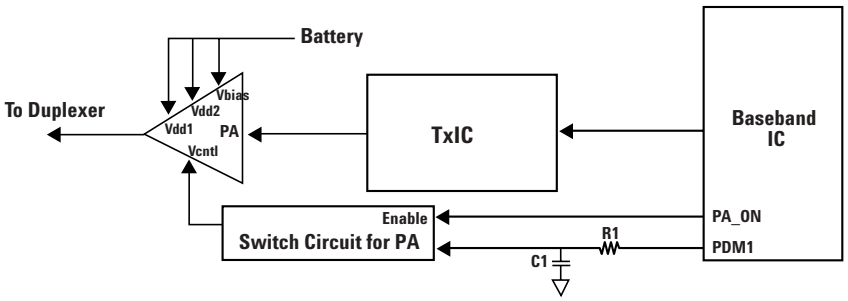


2. Step Bias Control and Dynamic Bias Control (if controled PDM1)

The PDM1 output from the baseband IC can be used to create a software-programmable voltage, to be used at the phone designer's discretion. To get high efficiency and better ACPR, the phone designers can change control voltage of the PA by adjusting PDM1 voltage according to output power of PA. A caution when using this approach—careful consideration must be made to to avoid an abrupt discontinuity in the output signal when the step bias control voltage is applied.

The figure below is an example of how to control the PA for multiple bias points using the PA_ON and Vcntl pins.

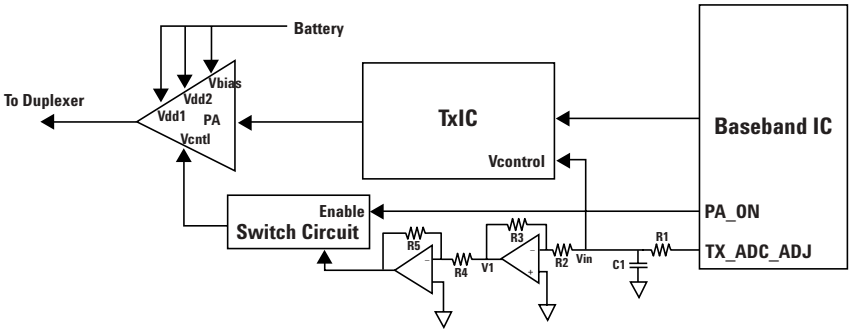
Power Mode	PA_ON	Vcntl	Power Range
Shut Down	LOW	0V	—
Low Power	HIGH	1.2V	~ -5 dBm
Mid Power	HIGH	1.6V	-5 dBm ~ 13 dBm
High Power	HIGH	2.5V	13 dBm ~ 28.5 dBm



If PDM1 can be controlled then same circuit can be used for Dynamic bias control

3. Dynamic Bias Control Alternate Implementation

Phone designers can use TX_ADC_ADJ pin of the baseband IC to get dynamic bias control with Vcntl pin of PA. TX_ADC_ADJ is a PDM output pin produced by the TX AGC subsystem and used to control the gain of the Tx signal prior to the PA. The variable output levels from two inverting operational amplifiers, generated and compared by TX_ADC_ADJ, provide dynamic control voltages for the Vcntl of 1.0V ~ 2.7V with a 0.1V step.

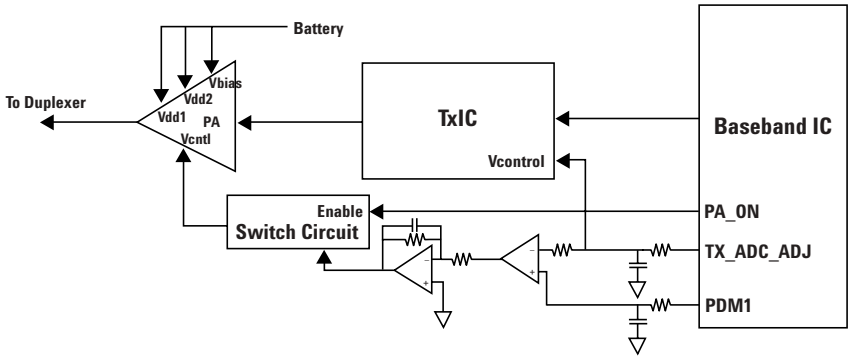


Av = -(V1/Vin) = -R3/R2,

V1 = -(R3/R2)Vin,

Vo = -(R5/R4)V1= [(R5*R3)/(R4*R2)]*Vin

The using of combination of two pins, PDM1 and TX_ADC_ADJ, is another method of realizing a dynamic bias control scheme. The two OP Amps control the Vcntl voltage levels with compared and integrated circuits.



ACPR Measurement Method

Adjacent-channel power ratio (ACPR) is used to characterize the distortion of power amplifiers and other subsystems for their tendency to cause interference with neighboring radio channels or systems. The ACPR measurement often is specified as the ratio of the power spectral density (PSD) of the CDMA main channel to the PSD measured at several offset frequencies. For the Cellular band (824 ~ 849 MHz transmitter channel), the two offsets are at ±885 kHz and ±1.98 MHz and the measurement resolution bandwidth specified is 30 kHz. These offsets are at ±1.25 MHz and ±1.98 MHz for the PCS band (1850 ~ 1910 MHz transmitter channel).

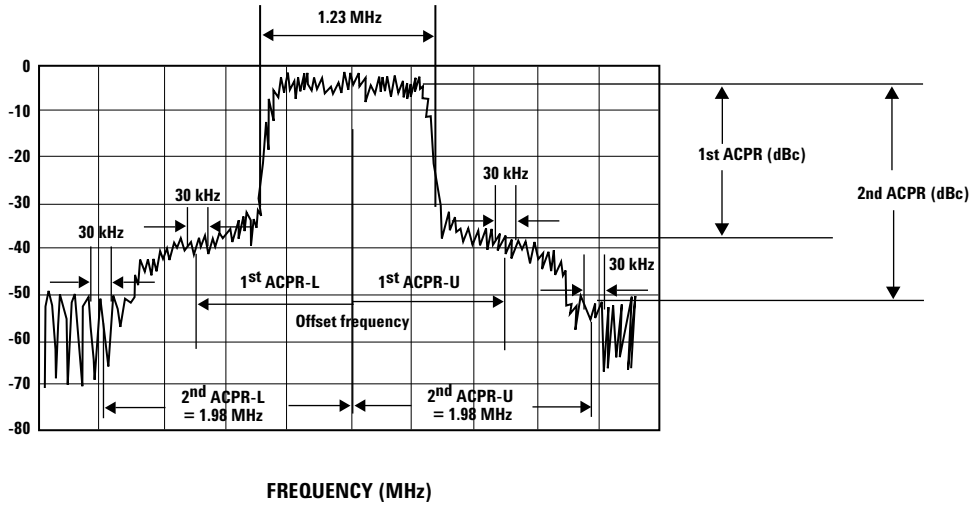


Figure 16. CDMA Adjacent-Channel Power Ratio Measurement.

ACPR Testing Diagram Test

PA Test Setup

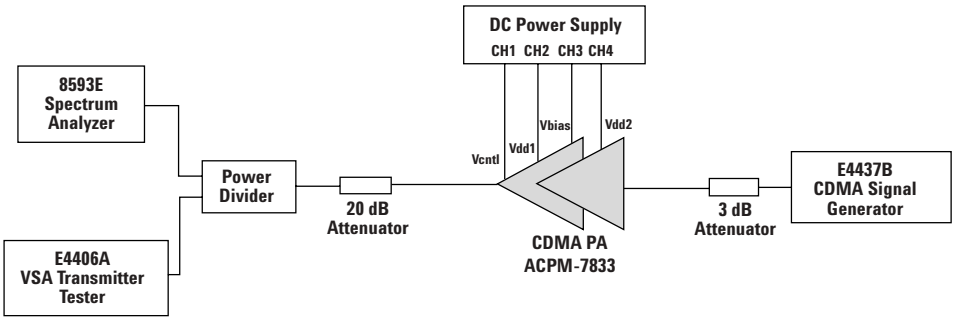


Figure 17. ACPR test equipment setup.

ACPM-7833 Test Result using VSA Transmitter Tester

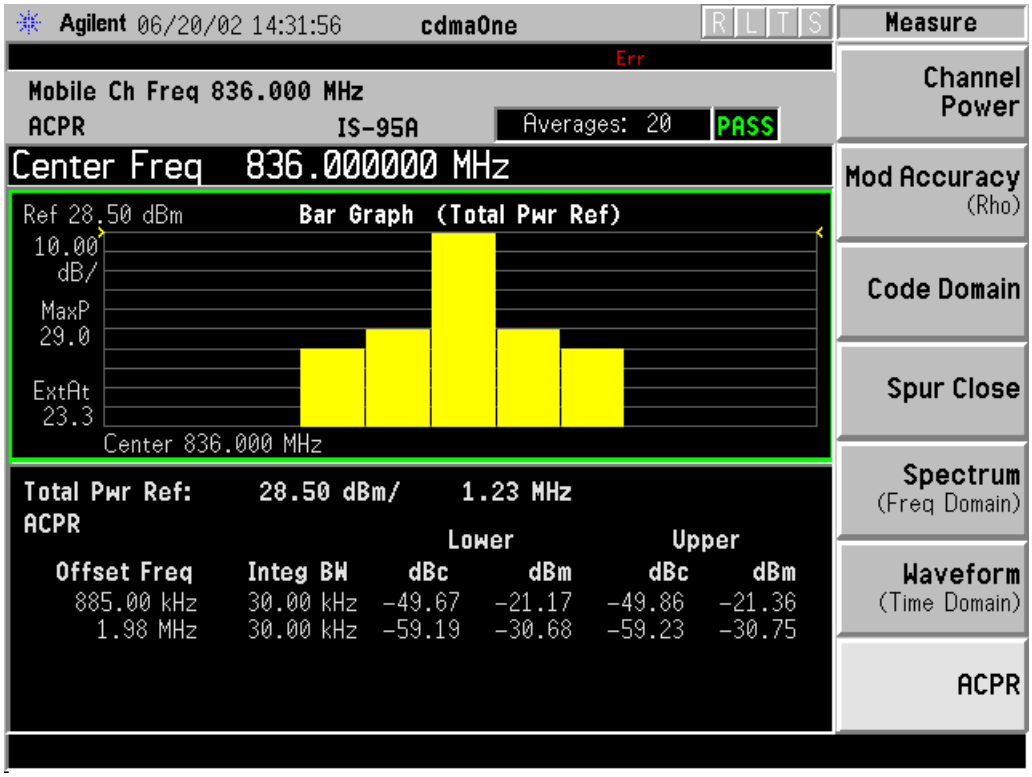


Figure 18. ACPR measurement using VSA Transmitter tester.

ACPR Test Results using Spectrum Analyzer

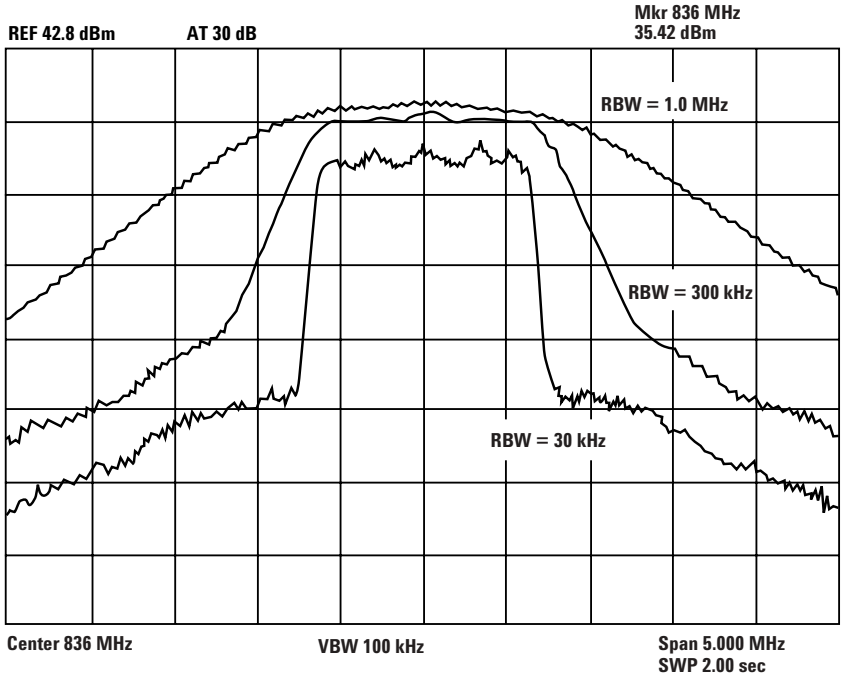


Figure 19. Example ACPR measurement using Spectrum Analyzer.

The meaning of 16 dB

The accurate ACPR measurement using Spectrum Analyzer needs to consider the normalization factor that is dependent on the Resolution Bandwidth, RBW, settings. The above figure (measurement shown at 836 MHz for general example) shows a comparison of the different ACPR measurement results as a function of various RBW values. As the RBW is reduced, less power is captured during the measurement and consequently the channel power is recorded as a smaller value. For example, if the main channel power is measured as 28 dBm in a 1.23 MHz bandwidth, its power spectral density is 28 dBm/1.23 MHz, which can be normalized to 11.87 dBm/30 kHz. The equation used to calculate the normalization factor of power spectral density is:

Normalization Factor =
10log[Normalization BW/Current BW
(Spectrum Analyzer RBW)]

$= 10\log[1.23X10^6/30X10^3]$

$= 16.13$ dB

Since the ACPR in an IS95 system is specified in a 1.23 MHz bandwidth, a channel power that is measured using a different RBW, can be normalized to reflect the channel power as if it was measured in a 1.23 MHz bandwidth. The difference in channel power measured in 30 kHz bandwidth and the channel power measured in a 1.23 MHz bandwidth is 16 dB.

ACPM-7833 Demoboard Operation Instructions

1) Module Description

The ACPM-7833 is a fully matched Power Amplifier. The sample devices are provided on a demonstration PC Board with SMA connectors for RF inputs and outputs, and a DC connector for all bias and control I/O's. Please refer to Figures 20 through 23 and the Pin configuration table for I/O descriptions and connections.

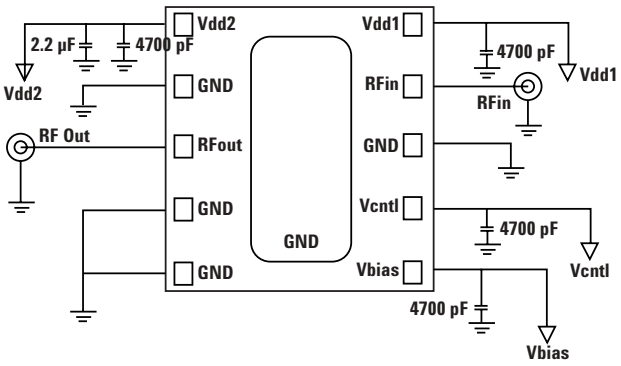


Figure 20. ACPM-7833 Evaluation Board Schematic and Layout.

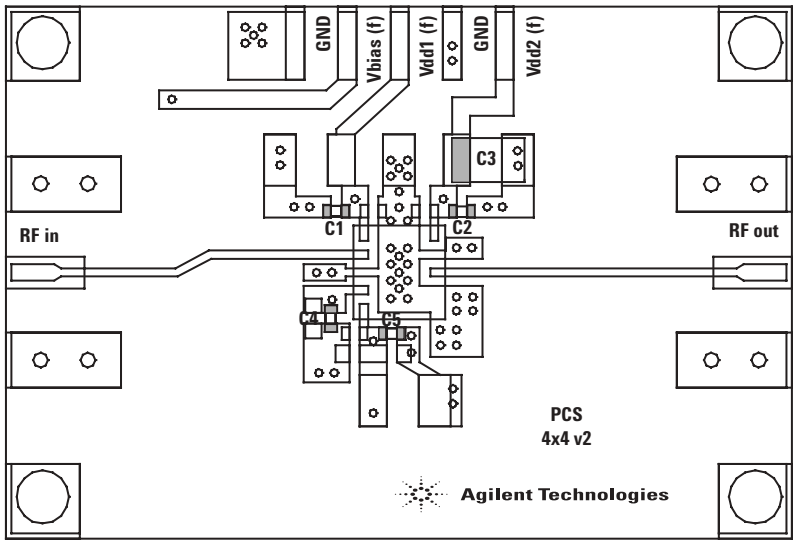


Figure 21. Layer 1 – Top Metal & Solder Mask.

PIN Configuration Table

Top side		Back side	
1	GND	1b	Vdd2 (s)
2	Vbias	2b	GND
3	Vdd1	3b	Vdd1 (s)
4	GND	4b	Vcntl
5	Vdd2	5b	Vbias (s)

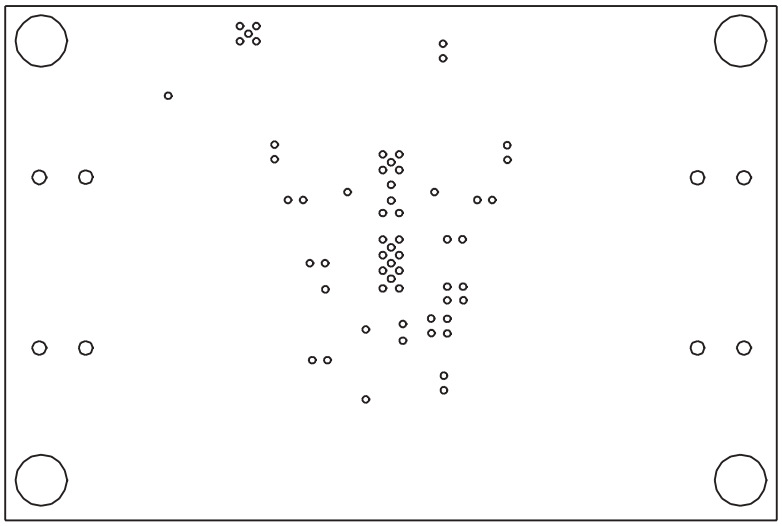


Figure 22. Layer 2 – Ground.

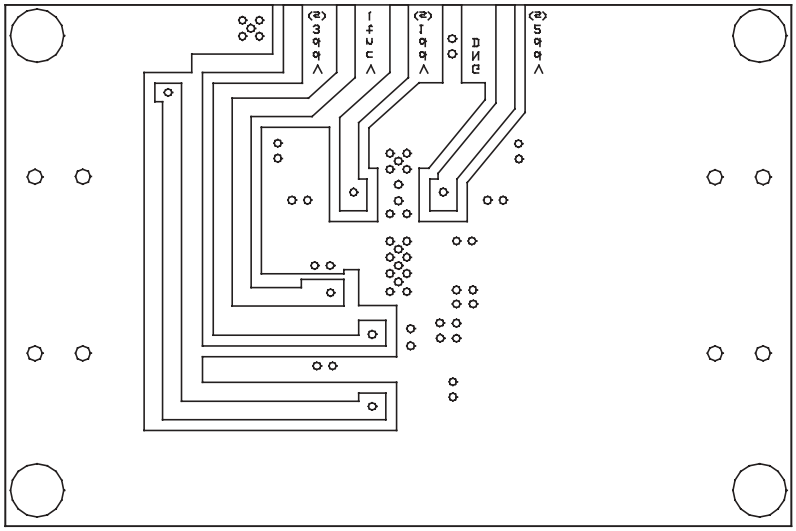


Figure 23. Layer 3 – Bottom Metal & Solder Mask.

2) Circuit Operation

The design of the power module (PAM) provide bias control via Vcntl to achieve optimal RF performance and power control. The control pin is labeled Vcntl. Please refer to for the block diagram of this PAM.

Typical Operation Conditions
(Vdd1=Vdd2=Vbias = 3.4V)

Parameter	ACPM-7833
Frequency Range	1850 – 1910 MHz
Output Power	28.5 dBm
Vcntl	2.5 V

3) Maximum Ratings

Vdd 5.0V
Drain Current 1.5A
Vcntl 3V
RF input 10 dBm
Temperature -30 to 85°C
Please Note: Avoid Electrostatic Discharge on all I/O's.

4) Heat Sinking

The demonstration PC Board provides an adequate heat sink. Maximum device dissipation should be kept below 2.5 Watts.

5) Testing

- Signal Source

The CDMA modulated signal for the test is generated using an Agilent ESG-D4000A (or ESG-D3000A) Digital Signal Generator with the following settings:

CDMA Setup : Reverse
Spreading: On
Bits/Symbol: 1
Data: PN15
Modulation: OQPSK
Chip Rate: 1.2288 Mcps
High Crest: On
Filter: Std
Phase Polarity: Invert

- ACPR Measurement

The ACPR (and channel power) is measured using an Avago Technologies 4406 VSA with corresponding ACPR offsets for IS-98c and JSTD-8. Averaging of 10 is used for ACPR measurements.

- DC Connection

A DC connector is provided to allow ease of connection to the I/Os. Wires can be soldered to the connector pins, or the connector can be removed and I/Os contacted via clip leads or direct soldered connections. The wiring of I/Os are listed in Figures 20 through 23 and the Pin configuration table. The Vdd sense connections are provided to allow the use of remote-sensing power supplies of compensation for PCB traces and cable resistance.

- Device Operation

1) Connect RF Input and Output for the band under test.
2) Terminate all unused RF ports into 50 Ohms.
3) Connect Vdd1, Vdd2 and Vdd3 supplies (including remote sensing labeled Vdd1 S, Vdd2 S and Vbias S on the board). Nominal voltage is 3.4V.
4) Connect Vcntl supply and set reference voltage to the voltage shown in the data packet. Note that the Vcntl pin is on the back side of the demonstration board. Please limit Vcntl to not exceed the corresponding listed "DC Biasing Condition" in the Data Packet. Note that increasing Vcntl over the corresponding listed "DC Biasing Condition" can result in power decrease and current can exceed the rated limit.
5) Apply RF input power according to the values listed in "Operation Data" in Data Packet.
6) Power down in opposite sequence.

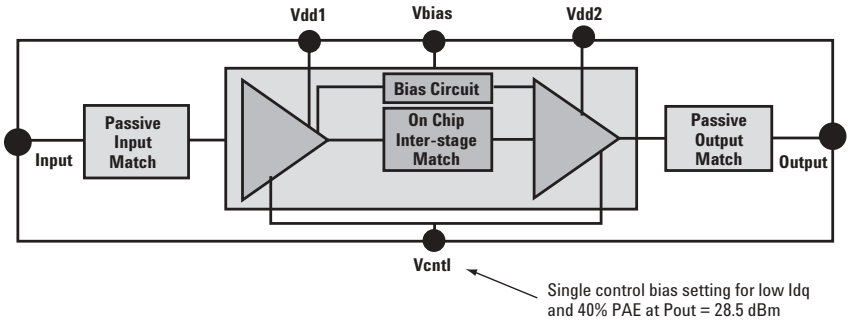


Figure 24. Power Module Block Diagram.

IR Reflow Soldering

Figure 25 is a straight-line representation of the recommended nominal time-temperature profile from JESD22-A113-B IR reflow.

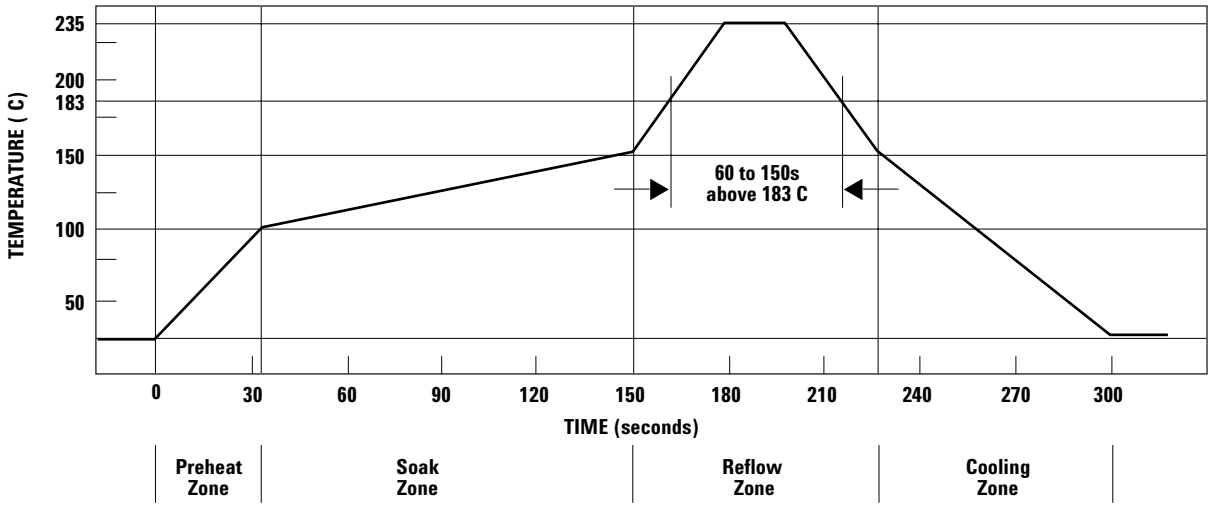


Figure 25. Time-temperature Profile for IR Reflow Soldering Process.

Table 2. IR Reflow Process Zone.

Process Zone	ΔTemperature	ΔTemperature/ΔTime
Preheat Zone	25°C to 100°C	3°C/s MAX
Soak Zone	100°C to 150°C	0.5°C/s MAX (120s MAX)
Reflow Zone	150°C to 235°C (240°C MAX) 235°C to 150°C	4.5°C/s TYP -4.5°C/s TYP
Cooling Zone	150°C to 25°C	-6°C/s MAX

Table 3. Classification Reflow Profiles.

	Convection or IR/Convection
Average ramp-up rate (183°C to peak)	3°C/second max.
Preheat temperature 125 (± 25)°C	120 seconds max.
Temperature maintained above 183°C	60 – 150 seconds
Time within 5°C of actual peak temperature	10 – 20 seconds
Peak temperature range	220 +5/-0°C or 235 +5/-0°C
Ramp-down rate	6°C/second max.
Time 25°C to peak temperature	6 minutes max.

Note:
All temperatures measured refer to the package body surface.

Zone 1 – Preheat Zone

The average heat up rate for surface-mount component on PCB shall be less than 3°C/second to allow even heating for both the component and PCB. This ramp is maintained until it reaches 100°C where flux activation starts.

Zone 2 – Soak Zone

The flux is being activated here to prepare for even and smooth solder joint in subsequent zone. The temperature ramp is kept gradual to minimize thermal mismatch between solder, PC Board and components. Over-ramp rate here can cause solder splatter due to excessive oxidation of paste.

Zone 3 – Reflow Zone

The third process zone is the solder reflow zone. The temperature in this zone rises rapidly from 183°C to peak temperature of 235°C for the solder to transform its phase from solid to liquids. The dwell time at melting point 183°C shall maintain at between 60 to 150 seconds. Upon the duration of 10-20 seconds at peak temperature, it is then cooled down rapidly to allow the solder to freeze and form solid.

Extended duration above the solder melting point can potentially damage temperature sensitive components and result in excessive inter-metallic growth that causes brittle solder joint, weak and unreliable connections. It can lead to unnecessary damage to the PC Board and discoloration to component's leads.

Zone 4 – Cooling Zone

The temperature ramp down rate is 6°C/second maximum. It is important to control the cooling rate as fast as possible in order to achieve the smaller grain size for solder and increase fatigue resistance of solder joint.

Solder Paste

The recommended solder paste is type Sn6337A or Sn60Pb40A of J-STD-006.

Note: Solder paste storage and shelf life shall be in accordance with manufacturer's specifications.

Stencil or Screen

The solder paste may be deposited onto PCB by either screen printing, using a stencil or syringe dispensing. The recommended stencil thickness is in accordance to JESD22-B102-C.

Nominal stencil thickness	Component lead pitch
0.102 mm (0.004 in)	Lead pitch less than 0.508 mm (0.020 in)
0.152 mm (0.006 in)	0.508 mm to 0.635 mm (0.02 in to 0.025 in)
0.203 mm (0.008 in)	Lead pitch greater than 0.635 mm (0.025 in)

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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