VMMK-2303

0.5 to 6 GHz 1.8 V E-pHEMT Shutdown LNA in Wafer Level Package

Data Sheet

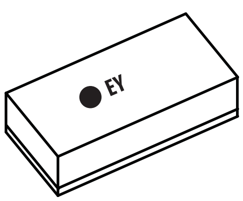
Lead (Pb) Free
RoHS 6 fully compliant

Description

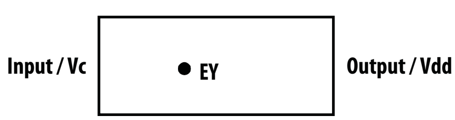
Avago's VMMK-2303 is an easy-to-use GaAs MMIC amplifier that offers excellent noise figure and flat gain from 0.5 to 6 GHz in a miniaturized wafer level package (WLP). It operates from 1.8V CMOS supply or 3.3V battery supply. The bias circuit has incorporated a power down feature which is accessed from the input port.

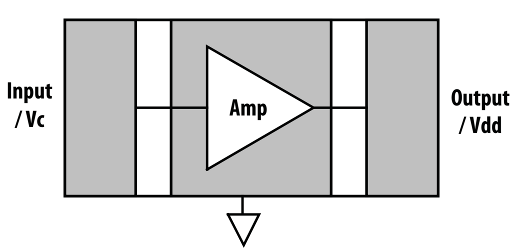
The input and output are matched to 50 Ω (better than 2:1 SWR) across the entire bandwidth; no external matching is needed. This amplifier is fabricated with enhancement E-pHEMT technology and industry leading revolutionary wafer level package. The wafer level package is small and ultra thin yet can be handled and placed with standard 0402 pick and place assembly.

WLP 0402, 1mm x 0.5mm x 0.25 mm



Pin Connections (Top View)





Note:
"E" = Device Code
"Y" = Month Code

Features

- 1 x 0.5 mm Surface Mount Package
- Ultrathin (0.25mm)
- Power down function
- 1.8V Supply
- 50Ohm Input and Output Match
- RoHs6 + Halogen Free

Specifications (3GHz, 1.8V, 21mA Typ.)

- Noise Figure: 2.0dB typical
- Associated Gain: 14dB
- Output IP3: +22dBm
- Output P1dB: +9dBm

Applications

- Low Noise and Driver for Cellular/PCS and WCDMA Base Stations
- 2.4 GHz, 3.5GHz, 5-6GHz WLAN and WiMax notebook computer, access point and mobile wireless applications
- 802.16 & 802.20 BWA systems
- WLL and MMDS Transceivers
- Radar, radio and ECM systems

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A)
ESD Human Body Model (Class 1A)
Refer to Avago Application Note A004R: Electrostatic Discharge, Damage and Control.

Table 1. Absolute Maximum Ratings

Sym	Parameters/Condition	Unit	Absolute Max
Vd	Supply Voltage (RF Output) [2]	V	5
Vc	Power Down Control Voltage	V	3
Id	Device Current [2]	mA	60
$P_{in, max}$	CW RF Input Power (RF Input) [3]	dBm	+13
P_{diss}	Total Power Dissipation	mW	300
Tch	Max channel temperature	°C	150
T_{STG}	Storage Temperature	°C	150
θjc	Thermal Resistance [4]	°C/W	140

Notes
1. Operation of this device above any one of these parameters may cause permanent damage
2. Bias is assumed DC quiescent conditions
3. With the DC (typical bias) and RF applied to the device at board temperature Tb = 25°C
4. Thermal resistance is measured from junction to board using IR method

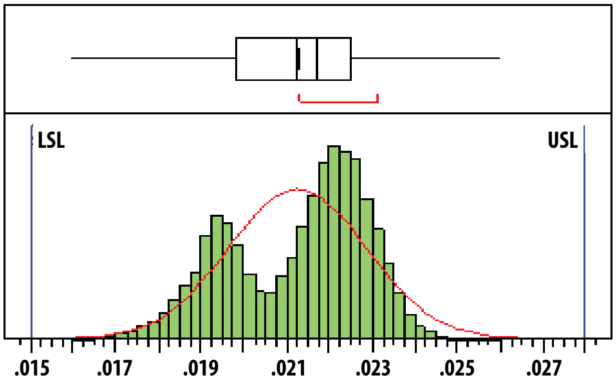
Table 2. DC and RF Specifications

T_A = 25°C, Frequency = 3 GHz, Vd = 1.8V, Vc = 1.8V, I_d = 21mA, Z_{in} = Z_{out} = 50Ω (unless otherwise specified)

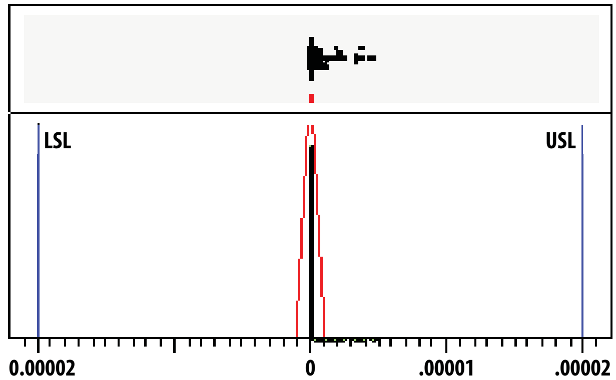
Sym	Parameters/Condition	Unit	Minimum	Typ.	Maximum
Id	Device Current	mA	15	21	28
Id_leakage	Current in Shut Down Mode	µA		0.03	20
NF [1]	Noise Figure	dB	–	2	2.6
Ga [1]	Associated Gain	dB	12	14	16
OIP3 [2,3]	Output 3rd Order Intercept	dBm		+22	–
Output P-1dB [2]	Output Power at 1dB Gain Compression	dBm		+9	–
IRL [2]	Input Return Loss	dB	–	-13	–
ORL [2]	Output Return Loss	dB	–	-19	–

Notes:
1. Measure data obtained using 300um G-S probe on production wafers
2. Measure data obtained using 300um G-S-G probe on PCB substrate
3. OIP3 test condition: F1=3.0GHz, F2=3.01GHz, Pin=-20dBm

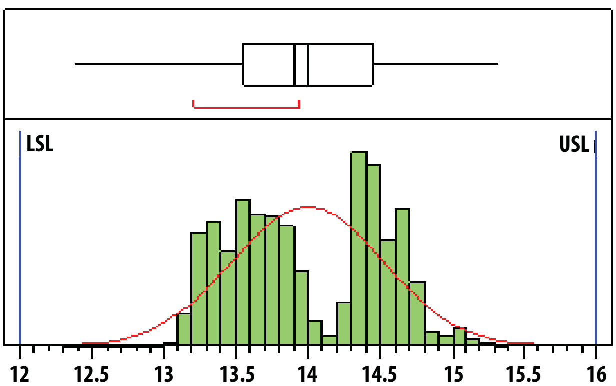
Product Consistency Distribution Charts at 3.0 GHz, Vd = 1.8 V, Vc = 1.8V



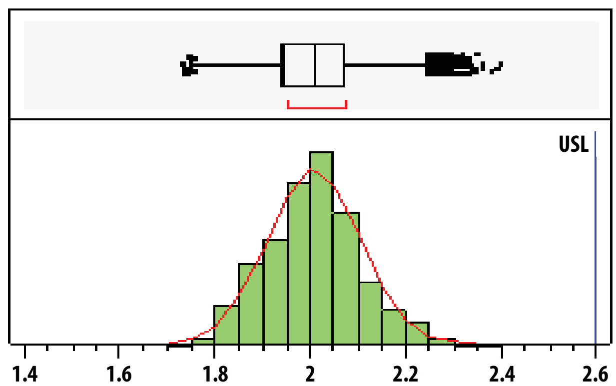
Id at Vd=Vc=1.8V, LSL=15mA, Mean=21mA, USL=28mA



Id_Off at Vd=1.8V & Vc=0V, Mean=0.025uA, USL=20uA



Gain at 3GHz, LSL=12 dB, Mean=14 dB, USL=16 dB



NF at 3GHz, Mean=2 dB, USL=2.6 dB

Note:
Distribution data based on 500 part sample size from 3 lots during initial characterization.
Measurements were obtained using 300um G-S production wafer probe.

VMMK-2303 Typical Performance

(T_A = 25°C, Vdd = 1.8V, Vc = 1.8V, Idd = 21mA, $Z_{in} = Z_{out}$ = 50 Ω unless noted)

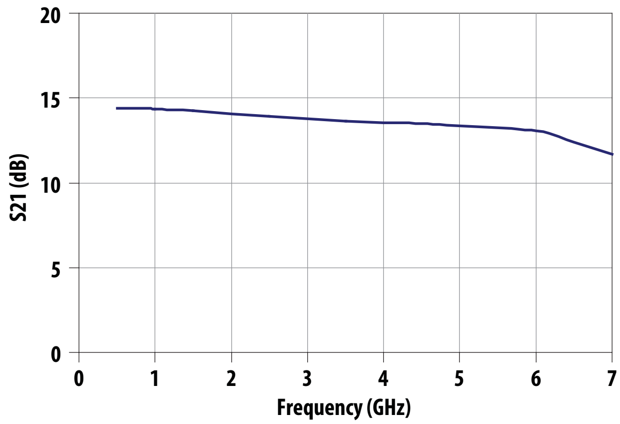


Figure 1. Small-signal Gain [1]

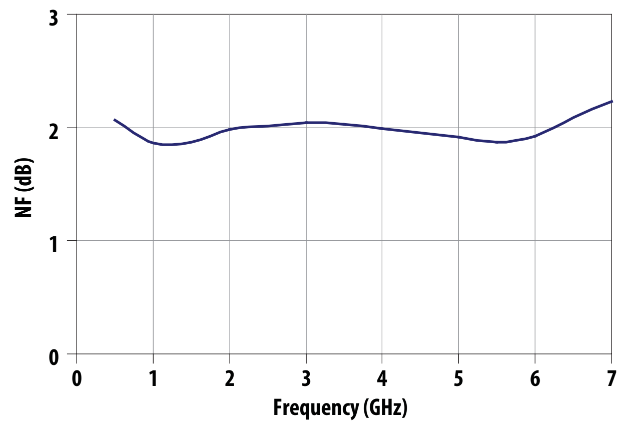


Figure 2. Noise Figure [1]

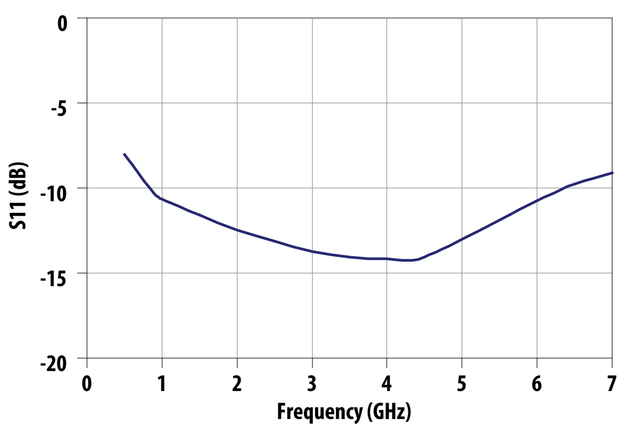


Figure 3. Input Return Loss [1]

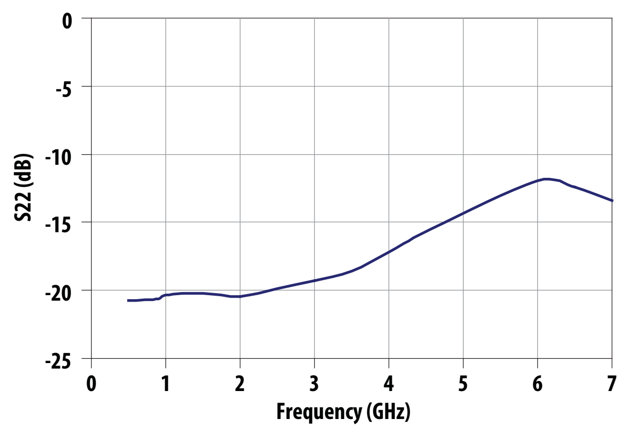


Figure 4. Output Return Loss [1]

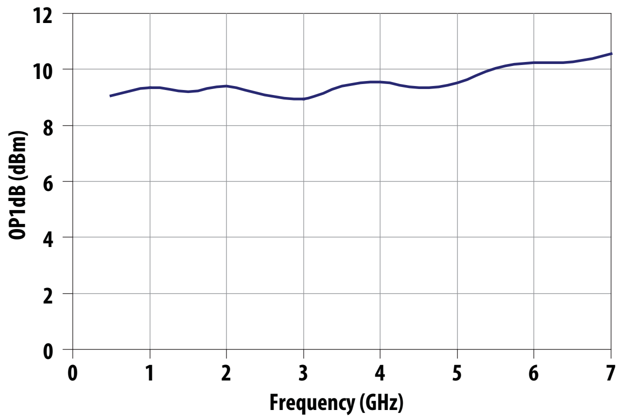


Figure 5. Output P-1dB [1]

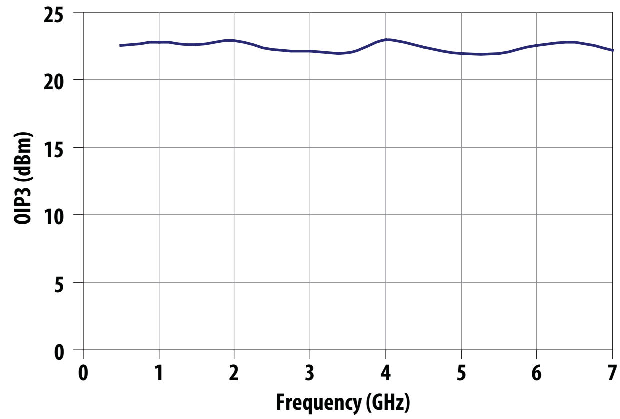


Figure 6. Output IP3 [1,2]

Notes:
1. Data taken on a G-S-G probe substrate fully de-embedded to the reference plane of the package
2. Output IP3 data taken at Pin=-15dBm

VMMK-2303 Typical Performance (continue)

(T_A = 25°C, Vdd = 1.8V, Vc = 1.8V, Idd = 21mA, $Z_{in} = Z_{out}$ = 50 Ω unless noted)

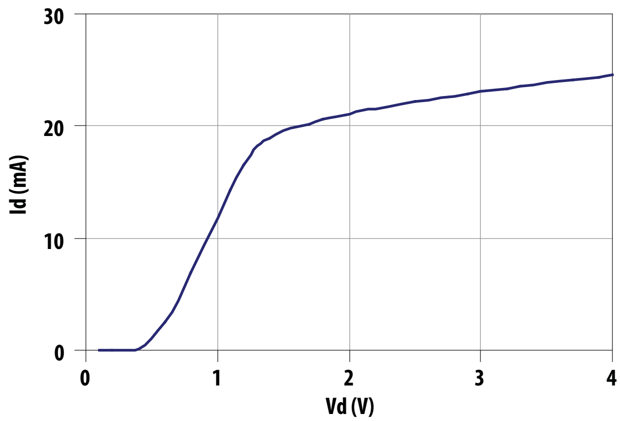


Figure 7. Total Current over Vdd [1]

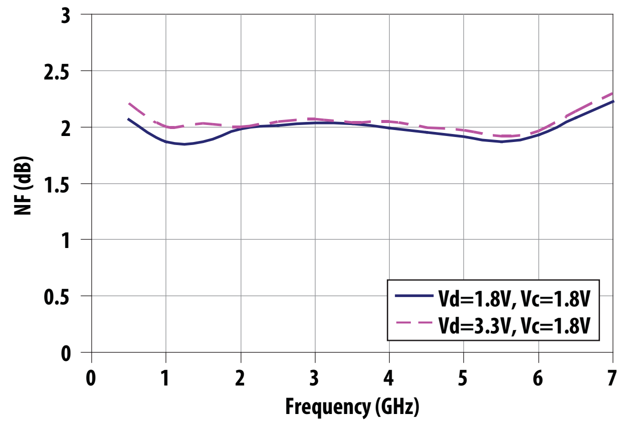


Figure 8. Noise Figure over Vdd [1]

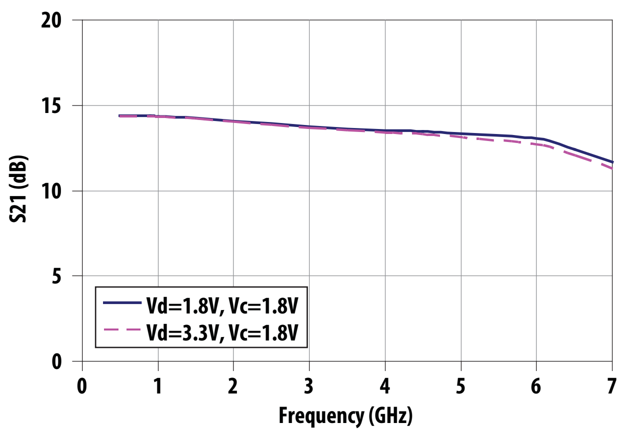


Figure 9. Gain over Vdd [1]

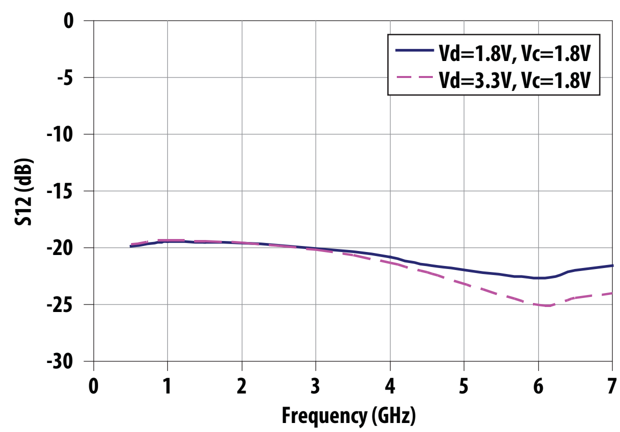


Figure 10. Isolation over Vdd [1]

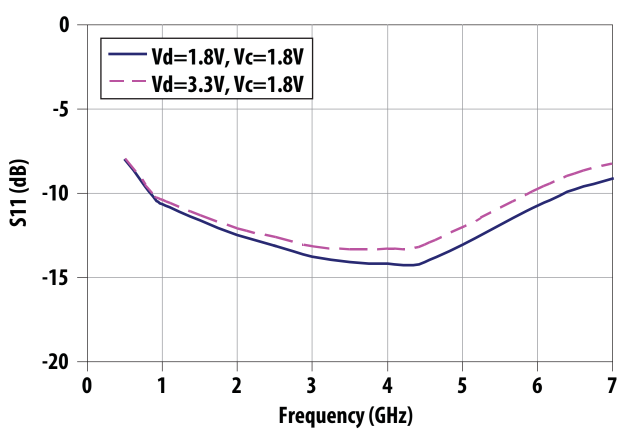


Figure 11. Input Return Loss Over Vdd [1]

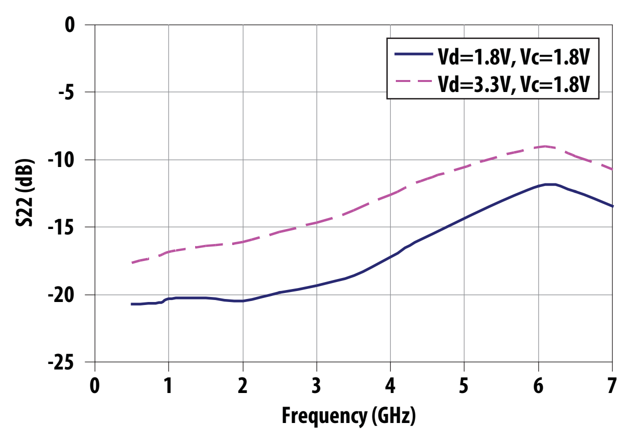


Figure 12. Output Return Loss Over Vdd [1]

Notes:
1. Data taken on a G-S-G probe substrate fully de-embedded to the reference plane of the package

VMMK-2303 Typical Performance (continue)

(T_A = 25°C, Vdd = 1.8V, Vc = 1.8V, Idd = 21mA, Z_{in} = Z_{out} = 50 Ω unless noted)

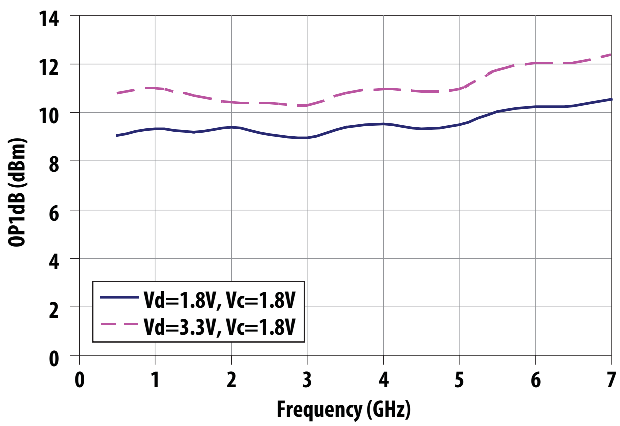


Figure 13. Output P-1dB over Vdd [1]

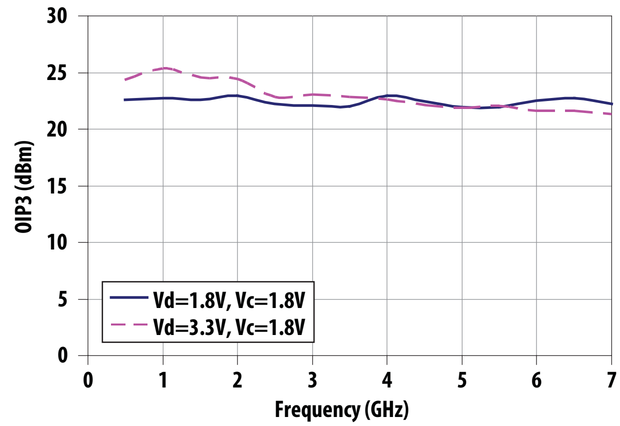


Figure 14. Output IP3 Over Vdd [1,2]

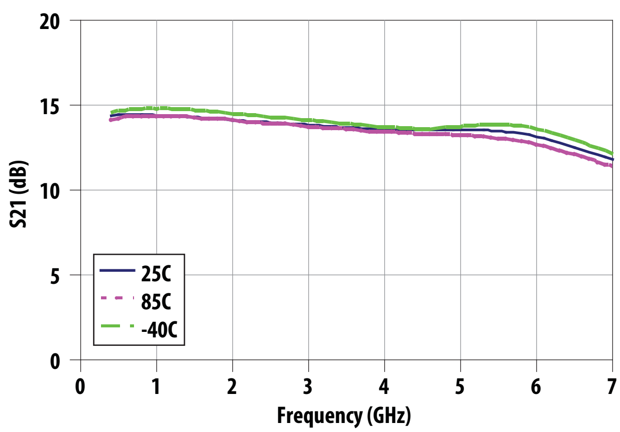


Figure 15. Gain over Temp [3]

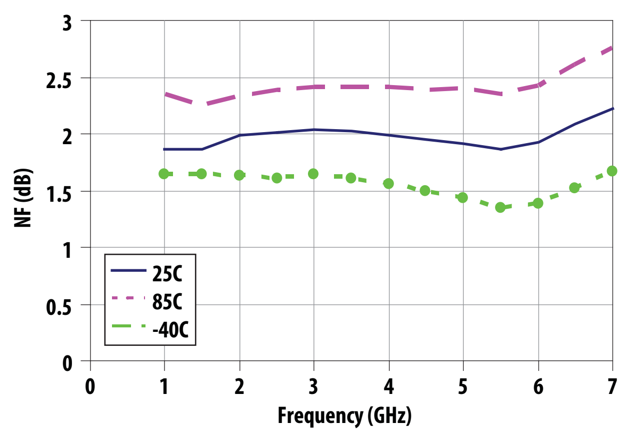


Figure 16. Noise Figure over Temp [3]

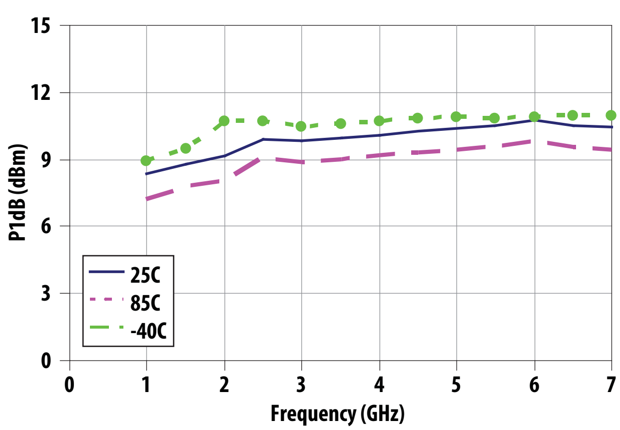


Figure 17. P1dB Over Temp [3]

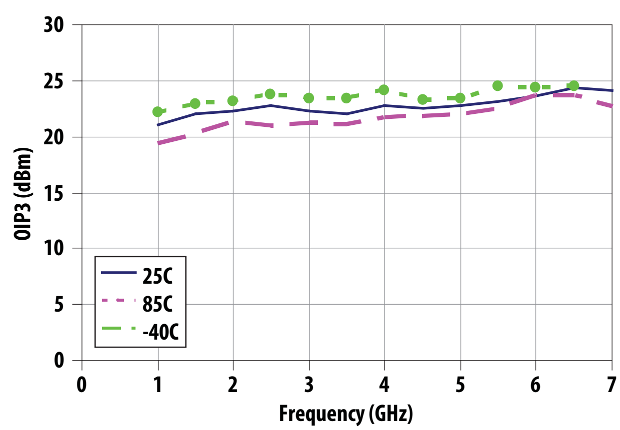


Figure 18. Output IP3 Over Temp [2,3]

Notes:

1. Data taken on a G-S-G probe substrate fully de-embedded to the reference plane of the package
2. Output IP3 data taken at Pin=-15dBm
3. Over temp data taken on a test fixture (Figure 20) without de-embedding

VMMK-2303 Typical S-parameters

(Data obtained using 300um G-S-G PCB substrate, losses calibrated out to the package reference plane;
T_A = 25°C, Vdd = 1.8V, Vc = 1.8V, Idd = 21mA, $Z_{in} = Z_{out}$ = 50 Ω unless noted)

Freq GHz	S11			S21			S12			S22		
	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase
0.1	-1.189	0.872	-25.218	13.588	4.780	-178.071	-25.597	0.053	59.673	-28.754	0.037	102.740
0.2	-3.285	0.685	-40.252	14.034	5.032	178.844	-21.873	0.081	39.048	-24.013	0.063	56.683
0.3	-5.171	0.551	-48.030	14.274	5.173	175.178	-20.621	0.093	25.793	-22.476	0.075	36.971
0.4	-6.965	0.449	-48.479	14.334	5.209	174.141	-20.114	0.099	20.372	-20.819	0.091	43.571
0.5	-8.033	0.397	-49.998	14.383	5.238	171.490	-19.862	0.102	14.988	-20.734	0.092	34.642
0.9	-10.340	0.304	-55.088	14.389	5.241	161.829	-19.502	0.106	2.738	-20.602	0.093	17.406
1	-10.633	0.294	-56.660	14.355	5.221	159.550	-19.469	0.106	0.569	-20.327	0.096	14.799
1.5	-11.604	0.263	-66.322	14.237	5.151	148.646	-19.510	0.106	-7.764	-20.247	0.097	5.593
2	-12.465	0.238	-77.367	14.066	5.050	138.043	-19.609	0.105	-14.262	-20.455	0.095	-4.429
2.5	-13.120	0.221	-92.069	13.921	4.967	127.967	-19.777	0.103	-20.126	-19.854	0.102	-10.667
3	-13.756	0.205	-105.553	13.761	4.876	117.996	-20.044	0.100	-25.917	-19.315	0.108	-16.656
3.5	-14.080	0.198	-121.275	13.625	4.800	108.216	-20.355	0.096	-31.482	-18.577	0.118	-19.883
4	-14.164	0.196	-138.080	13.528	4.747	98.536	-20.819	0.091	-36.539	-17.215	0.138	-24.628
4.5	-14.080	0.198	-155.711	13.469	4.715	88.588	-21.473	0.084	-41.043	-15.682	0.164	-28.934
6	-10.734	0.291	137.934	13.064	4.500	53.142	-22.639	0.074	-39.719	-11.962	0.252	-67.155
6.5	-9.789	0.324	112.577	12.421	4.179	41.188	-21.971	0.080	-42.502	-12.385	0.240	-84.103
7	-9.114	0.350	90.524	11.686	3.840	30.984	-21.598	0.083	-49.096	-13.416	0.213	-97.269
7.5	-8.552	0.374	71.896	11.011	3.553	21.893	-21.639	0.083	-56.813	-14.572	0.187	-106.937
8	-7.985	0.399	55.866	10.407	3.314	13.237	-21.927	0.080	-64.022	-15.783	0.163	-114.375
8.5	-7.414	0.426	41.571	9.855	3.110	4.832	-22.395	0.076	-71.213	-16.936	0.142	-119.103
9	-6.934	0.450	28.414	9.336	2.930	-3.596	-22.987	0.071	-78.204	-18.048	0.125	-123.159
9.5	-6.519	0.472	16.304	8.820	2.761	-12.097	-23.702	0.065	-85.057	-19.188	0.110	-125.957
10	-6.152	0.493	5.143	8.292	2.598	-20.481	-24.539	0.059	-92.301	-20.175	0.098	-128.274
10.5	-5.857	0.510	-5.889	7.753	2.442	-28.823	-25.449	0.053	-98.980	-21.412	0.085	-129.273
11	-5.698	0.519	-16.421	7.207	2.293	-37.155	-26.558	0.047	-106.295	-22.418	0.076	-129.884
11.5	-5.647	0.522	-26.546	6.634	2.146	-45.392	-27.894	0.040	-114.058	-23.504	0.067	-129.694
12	-5.668	0.521	-36.450	6.034	2.003	-53.627	-29.499	0.034	-122.428	-24.657	0.059	-128.305
12.5	-5.769	0.515	-46.265	5.403	1.863	-61.689	-31.437	0.027	-131.444	-25.900	0.051	-125.420
13	-6.024	0.500	-56.018	4.750	1.728	-69.652	-33.893	0.020	-143.164	-26.859	0.045	-119.561
13.5	-6.384	0.480	-65.570	4.058	1.596	-77.410	-36.954	0.014	-157.876	-27.597	0.042	-113.832
14	-6.786	0.458	-74.640	3.346	1.470	-84.974	-40.537	0.009	176.577	-28.382	0.038	-107.341

VMMK-2303 Application and Usage

Biasing and Operation

The VMMK-2303 can be used as a low noise amplifier or as a driver amplifier. The nominal bias condition for the VMMK-2303 is Vd=Vc=1.8V. At this bias condition the VMMK-2303 provides an optimal compromise between power consumption, noise figure, gain, power output and OIP3. The VMMK-2303 can also be operated a Vd of 3.3V and a Vc of 1.8V which will result in higher P1dB and OIP3. At Vc=1.8V, the corresponding drain currents are approximately 21 and 23 mA at Vd of 1.8V and 3.3V respectively.

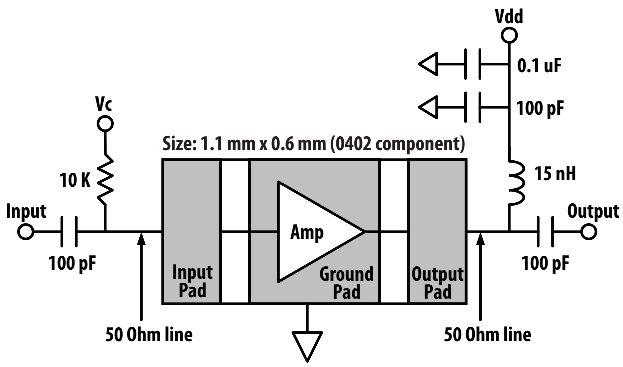


Figure 19. Example application of VMMK-2303 at 3GHz

The VMMK-2303 is biased with a positive supply connected to the output pin through an external user supplied bias-tee as shown in Figure 19. The power down feature (Vc) at the input port is accessed through an external 10kΩ resistor. The resistor will have minimal effect on circuit performance. The LNA is turned on when Vc is at 1.8V and shut off when Vc is at 0V. In a typical application, the bias-tee on the output port can be constructed using lumped elements. The value of the output inductor can have a major effect on both low and high frequency operation. The demo board uses a 15 nH inductor that has self resonant frequency higher than the maximum desired frequency of operation. If the self-resonant frequency of the inductor is too close to the operating band, the value of the inductor needs to be adjusted so that the self-resonant frequency is significantly higher than the highest frequency of operation. Extending the low frequency response of the VMMK-2303 is possible by using two different value inductors in series with the smaller value inductor placed closest to the device and favoring the higher frequencies. The larger value inductor will then offer better low frequency performance by not loading the output of the device. The parallel combination of the 100pF and 0.1uF capacitors provide a low impedance in the band of operation and at lower frequencies and should be placed as close as possible to the inductor. The low frequency bypass provides good rejection of power supply noise and also provides a low impedance termination for third order low frequency mixing products that will be generated when multiple in-band signals are injected into any amplifier. It is also suggested that a 0.1uF capacitor be used to bypass the 10kΩ resistor that feeds the Vc terminal. This will prevent noise and other spurious from affecting the noise figure of the VMMK-2303.

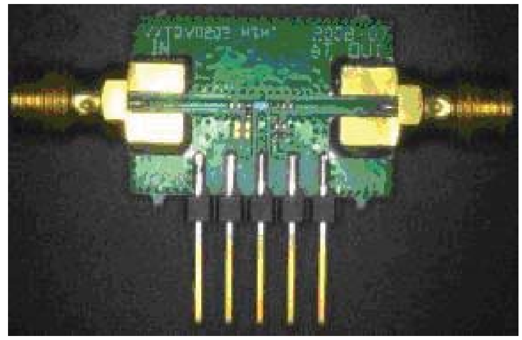


Figure 20. Evaluation/Test Board (available to qualified customer request)

Refer the Absolute Maximum Ratings table for allowed DC and thermal conditions.

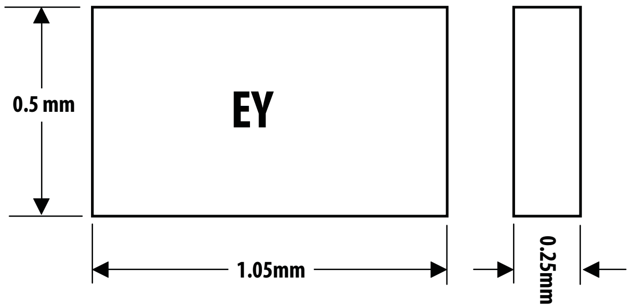
S Parameter Measurements

The S parameters are measured on a 300um G-S-G (ground signal ground) printed circuit board substrate. Calibration is achieved with a series of through, short and open substrates from which an accurate set of S parameters is created. The test board is .016 inch thickness RO4350. Grounding of the device is achieved with a single plated through hole directly under the device. The effect of this plated through hole is included in the S parameter measurements and is difficult to de-embed accurately. Since the maximum recommended printed circuit board thickness is nominally .020 inch, then the nominal effect of printed circuit board grounding can be considered to have already been included the published S parameters.

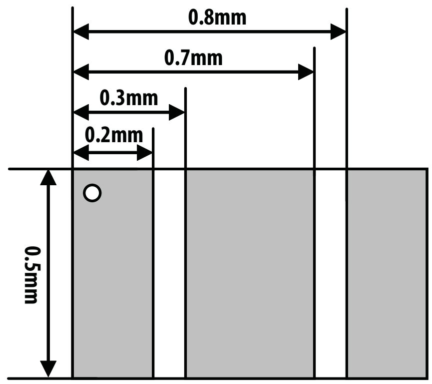
The product consistency distribution charts shown on page 2 represent data taken by the production wafer probe station using a 300um G-S wafer probe. The ground-signal probing that is used in production allows the device to be probed directly at the device with minimal common lead inductance to ground. Therefore there will be a slight difference in the nominal gain obtained at the test frequency using the 300um G-S wafer probe versus the 300um G-S-G printed circuit board substrate method.

Outline Drawing

Top and Side View

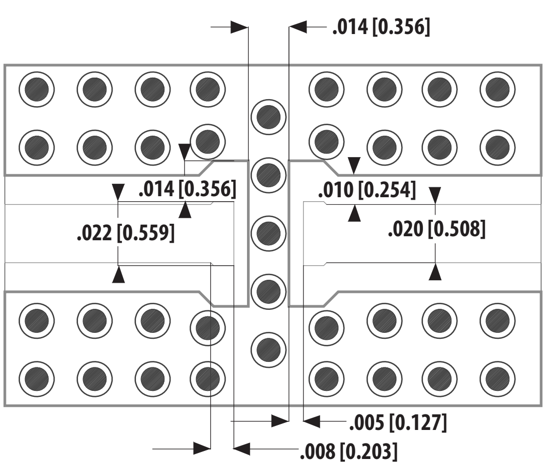


Bottom View



Notes:
1. • indicates pin 1
2. Dimensions are in millimeters
3. Pad Material is minimum 5.0 um thick Au

Suggested PCB Material and Land Pattern



Notes:
1. 0.010" Rogers RO4350

Recommended SMT Attachment

The VMMK Packaged Devices are compatible with high volume surface mount PCB assembly processes.

Manual Assembly for Prototypes

1. Follow ESD precautions while handling packages.
2. Handling should be along the edges with tweezers or from topside if using a vacuum collet.
3. Recommended attachment is solder paste. Please see recommended solder reflow profile. Conductive epoxy is not recommended. Hand soldering is not recommended.
4. Apply solder paste using either a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance. **Excessive solder will degrade RF performance.**
5. Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temp to avoid damage due to thermal shock.
6. Packages have been qualified to withstand a peak temperature of 280°C for 15 sec. Verify that the profile will not expose device beyond these limits.
7. Clean off flux per vendor's recommendations.
8. Clean the module with Acetone. Rinse with alcohol. Allow the module to dry before testing.

Note: These devices are ESD sensitive. The following precautions are strongly recommended. Ensure that an ESD approved carrier is used when die are transported from one destination to another. Personal grounding is to be worn at all times when handling these devices. For more detail, refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control

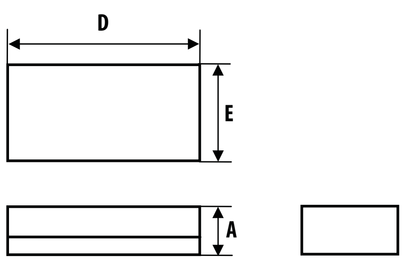
ESD Machine Model (Class A)

ESD Human Body Model (Class A)

Ordering Information

Part Number	Devices Per Container	Container
VMMK-2303-BLKG	100	Antistatic Bag
VMMK-2303-TR1G	5000	7" Reel

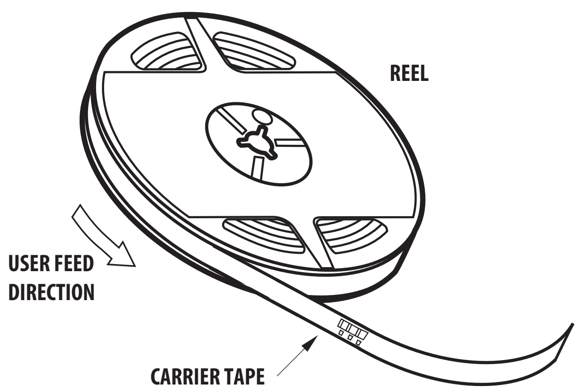
Package Dimension Outline



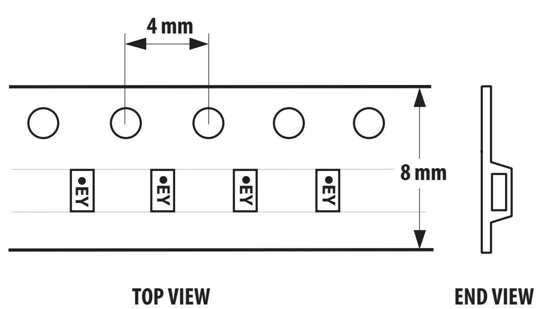
Symbol	Min (mm)	Max (mm)
E	0.500	0.566
D	1.004	1.066
A	0.235	0.265

Note:
All dimensions are in mm

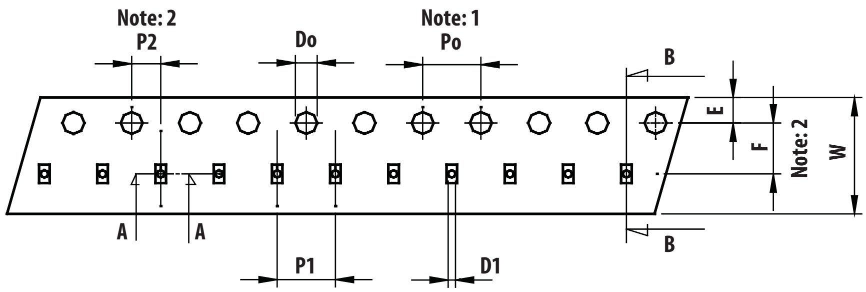
Reel Orientation

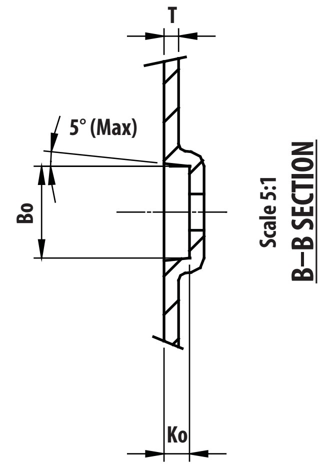


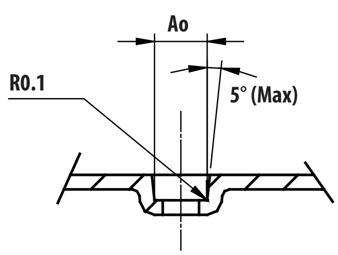
Device Orientation



Tape Dimensions







Scale 5:1

A–A SECTION

Ao = 0.73±0.05 mm

Bo = 1.26±0.05 mm

Ko = 0.35 $^{+0.05}_{+0}$ mm

Unit: mm

Symbol	Spec.
K1	–
Po	4.0±0.10
P1	4.0±0.10
P2	2.0±0.05
Do	1.55±0.05
D1	0.5±0.05
E	1.75±0.10
F	3.50±0.05
10Po	40.0±0.10
W	8.0±0.20
T	0.20±0.02

Notice:
1. 10 Sprocket hole pitch cumulative tolerance is ±0.1mm.
2. Pocket position relative to sprocket hole measured as true position of pocket not pocket hole.
3. Ao & Bo measured on a place 0.3mm above the bottom of the pocket to top surface of the carrier.
4. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. Carrier camber shall be not than 1m per 100mm through a length of 250mm.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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