



Package: QFN, 4 mm x 4 mm

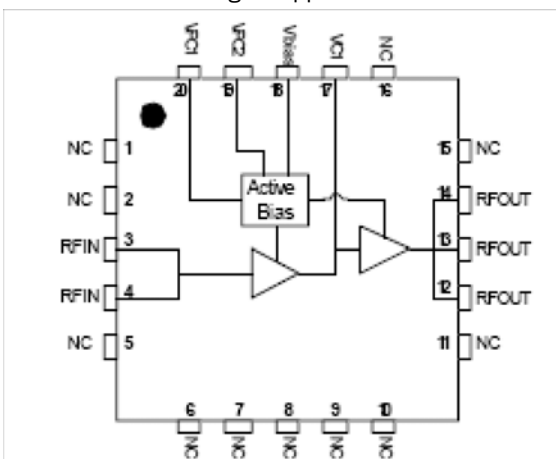


### Product Description

RFMD's SZA-6044 is a high linearity Class A GaAs Heterojunction Bipolar Transistor (HBT) amplifier housed in a low-cost surface-mountable plastic package. These HBT amplifiers are fabricated using molecular beam epitaxial growth technology which produces reliable and consistent performance from wafer to wafer and lot to lot. This product is specifically designed as a driver or final stage amplifier for equipment in the 5.1GHz to 5.9GHz band. It can run from a 3V to 5V supply. Load line optimization for target band is possible outside the package. Its high linearity makes it an ideal choice for multicarrier and digital applications.

#### Optimum Technology Matching® Applied

- GaAs HBT
- GaAs MESFET
- InGaP HBT
- SiGe BiCMOS
- Si BiCMOS
- SiGe HBT
- GaAs pHEMT
- Si CMOS
- Si BJT
- GaN HEMT
- RF MEMS



### Features

- Single 3V to 5V Operation
- High Linearity Class A  
OIP<sub>3</sub> = 39dBm at 5V
- 802.11a 54 Mb/s  
P<sub>OUT</sub> = 17 dBm at 3% EVM
- P<sub>1dB</sub> 24dBm at 5V, 21dBm at 3.3V
- Surface Mount Plastic Package
- Power Up/Down Control < 1μs

### Applications

- OFDM
- Multicarrier Applications
- 802.11a WLAN Driver Stage
- Fixed Wireless, UNII

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Frequency of Operation,	5100		5900	MHz	
Output Power at 1dB Compression		24.9		dBm	5.1GHz
		24.6		dBm	5.5GHz
	22.5	24.0	26.0	dBm	5.9GHz
Small Signal Gain	17.0	18.5	20.0	dB	5.1GHz
		17.3		dB	5.5GHz
	14.9	16.4	17.9	dB	5.9GHz
Worst Case Input Return Loss	8.0	11.0		dB	5.1GHz to 5.9GHz
Worst Case Output Return Loss	12.0	17.0		dB	5.1GHz to 5.9GHz
Output IP <sub>3</sub>	37.0	39.0		dBm	P <sub>OUT</sub> per tone = +8dBm @ 5.9GHz
P <sub>OUT</sub>		17.0		dBm	802.11a 54 Mb/s P <sub>OUT</sub> @ 3% EVM @ 5.9GHz, I = 165 mA
Noise Figure,		7.8	9.8	dB	5.9GHz
Total Device Current	145.0	165.0	185.0	mA	I <sub>VBIAS</sub> + I <sub>CTOTAL</sub> = 150 mA, I <sub>VPC12</sub> = 15 mA
Thermal Resistance		56		°C/W	junction - lead

Test Conditions: Z<sub>0</sub> = 50Ω, V<sub>CC</sub> = 5V, I = 165 mA, T<sub>BP</sub> = 30 °C

## Absolute Maximum Ratings

Parameter	Rating	Unit
1st stage Collector Bias Current ( $I_{VC1}$ )	100	mA
2nd Stage Collector Bias Current ( $I_{VC2}$ )	190	mA
Device Voltage ( $V_D$ )	6.0	V
Power Dissipation	1.5	W
Operating Lead Temperature ( $T_L$ )	-40 to +85	°C
RF Input Power	20	dBm
Junction Temp ( $T_J$ )	+150	°C
Storage Temperature Range	-40 to +150	°C
ESD Rating - Human Body Model, Class 1B (HBM)	500	V



**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

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Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one.

Bias Conditions should also satisfy the following expression:

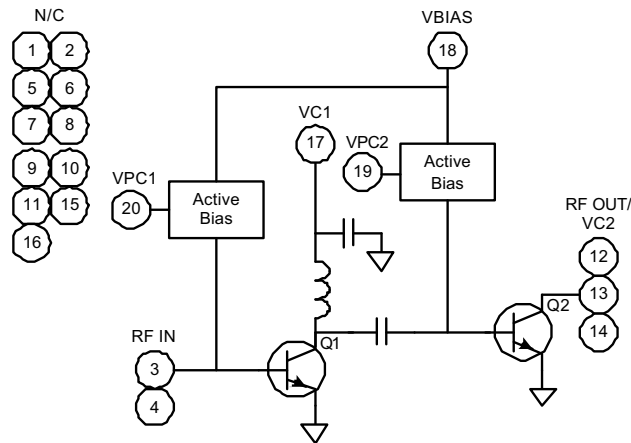
$$I_D V_D < (T_J - T_L) / R_{TH, j-l}$$

## Typical Performance with 2.45GHz Application Circuit

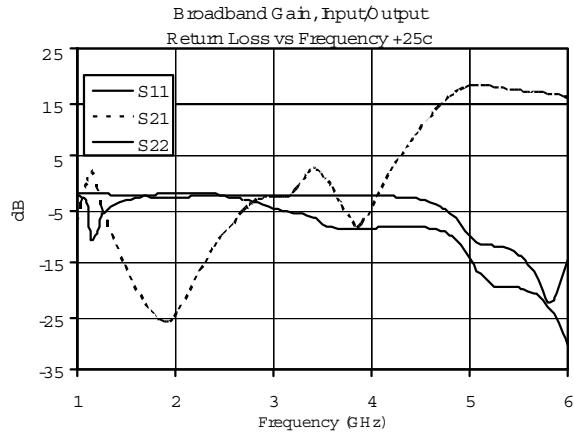
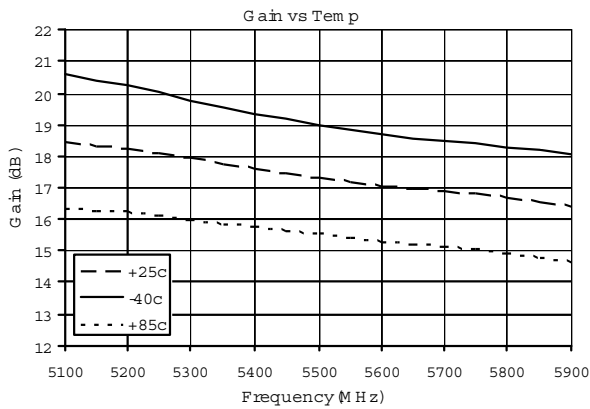
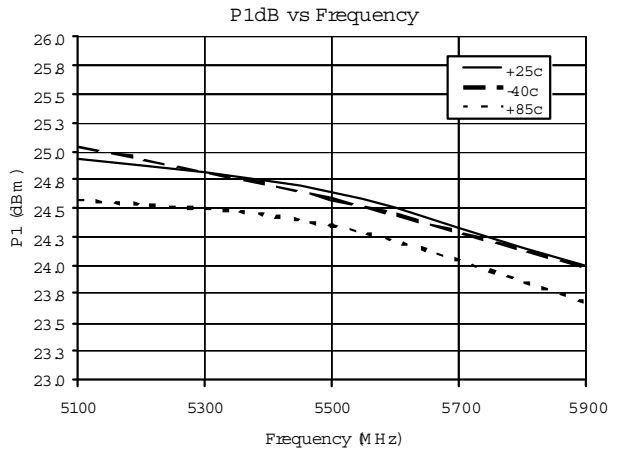
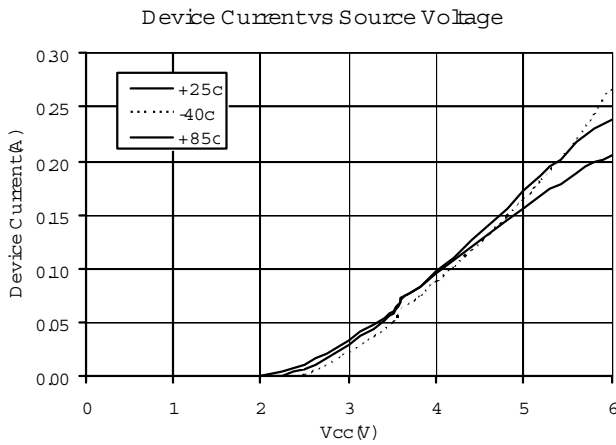
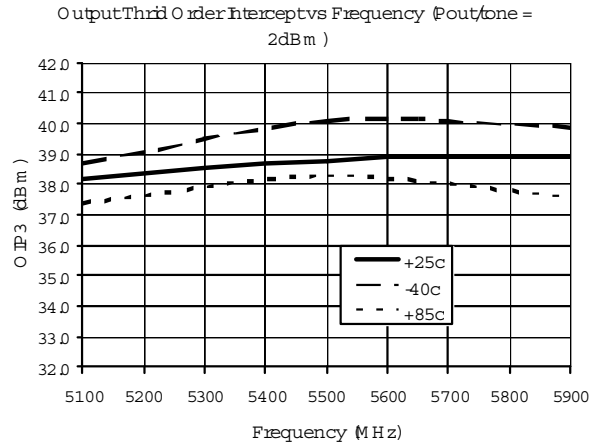
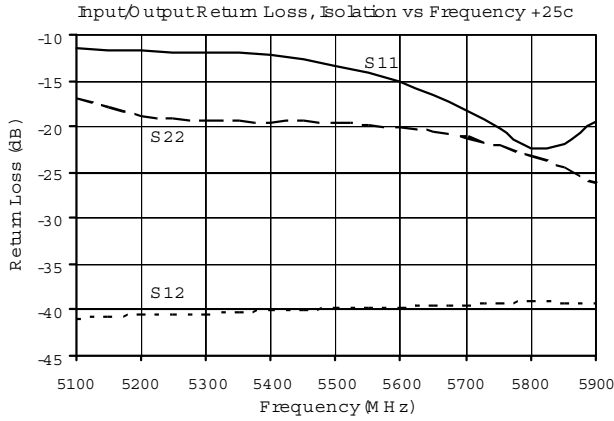
Freq (MHz)	VS (v)	VCE (V)	IDQ (mA)	P1dB (dBm)	OIP3 (dBm)	Gain (dB)	S11 (dB)	S22 (dB)	NF (dB)	Comments
2.4	3.3	2.7	11.0	9.6	27.0	15.0	16.5	17.0	1.4	Series Feedback
2.45	3.3	2.7	11.0	9.9	27.0	14.8	18.0	18.0	1.5	
2.5	3.3	2.7	11.0	9.8	27.0	14.6	18.5	19.0	1.5	

Test Conditions: OIP3 Tone Spacing= 1 MHz,  $P_{OUT}$  per tone=-5 dBm.  $T_L = 25^\circ C$

## Simplified Device Schematic

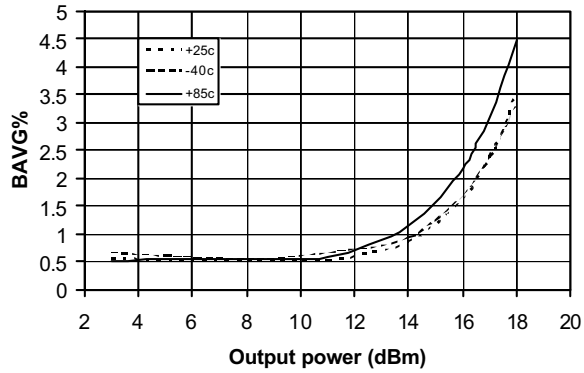


5.1 - 5.9 GHz Evaluation Board Data ( $V_{BAS} = 5.0V$ ,  $I_{BAS} = 165mA$ )

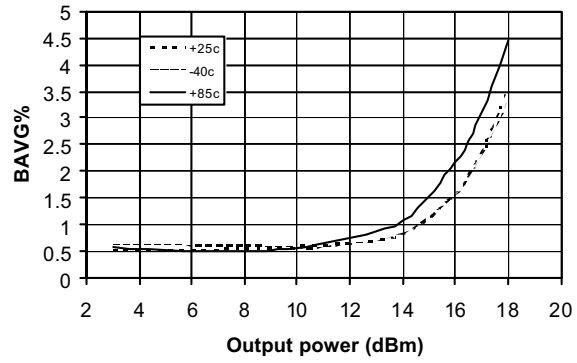


802.11a 64QAM 54Mb/s Error Vector Magnitude Data ( $V_{BIAS} = 5.0V$ ,  $I_{BIAS} = 165mA$ )

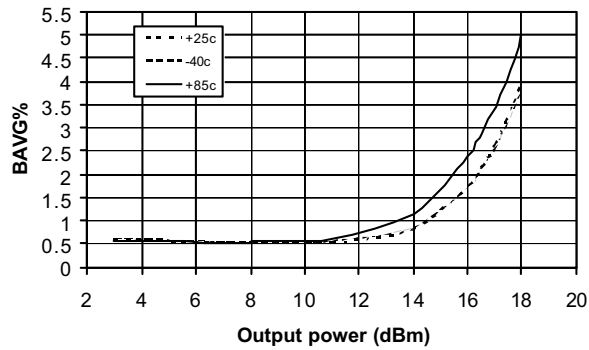
**EVM Burst Average% vs Output Power (dBm)**  
Freq = 5.15GHz



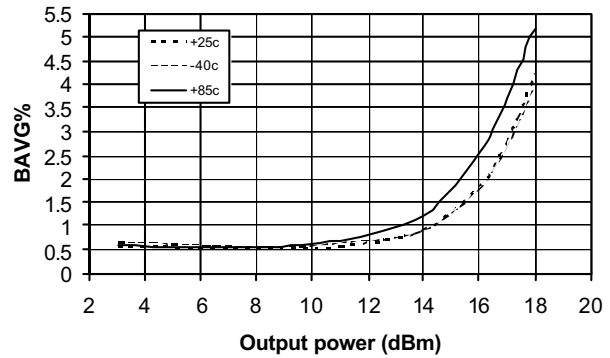
**EVM Burst Average% vs Output Power (dBm)**  
Freq = 5.35GHz



**EVM Burst Average% vs Output Power (dBm)**  
Freq = 5.725GHz



**EVM Burst Average% vs Output Power (dBm)**  
Freq = 5.875GHz

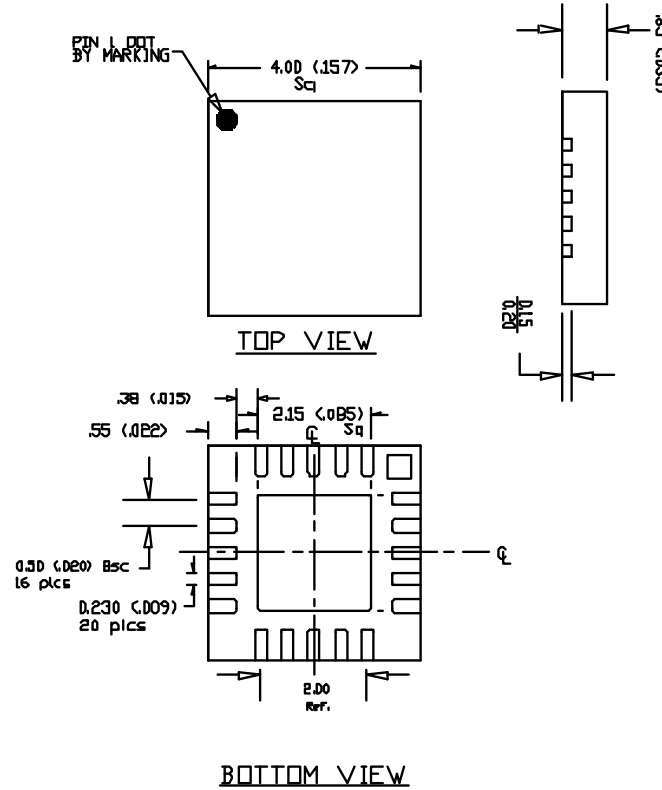


Pin	Function	Description
<b>1, 2, 5, 6, 7, 8, 9, 10, 11, 15, 16</b>	<b>N/C</b>	Pins are not used. May be grounded, left open or connected to adjacent pin.
<b>19</b>	<b>VPC2</b>	VPC2 is the bias control pin for the stage 2 active bias circuit. An external series resistor is required for proper setting of bias levels. Refer to the evaluation board schematic for resistor value.
<b>20</b>	<b>VPC1</b>	VPC1 is the control pin for the stage 1 active bias circuits. An external series resistor is required for proper setting of bias levels. Refer to the evaluation board schematic for resistor value.
<b>18</b>	<b>VBIAS</b>	VBIAS is the active bias circuit supply voltage. Can be operated from 3V to 5V.
<b>3, 4</b>	<b>RFIN</b>	RF input pin. This is DC grounded internal to the IC. Do not apply voltage to this pin. Both pins 3 and 4 must be used for proper operation.
<b>12, 13, 14</b>	<b>RFOUT/ VC2</b>	RF output and second stage collector supply voltage pin. VC2 in the range of 3V to 5V voltage should be supplied to this pin through an external RF choke. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see evaluation board schematic). The supply side of the bias network should be well bypassed. The output network and board layout specified in the app circuit is recommended for optimum performance. All pins 12-14 are required to be wired together at lead foot for proper operation.
<b>17</b>	<b>VC1</b>	VC1 is the first stage collector supply voltage. Can be operated over the range of 3V to 5V.
<b>EPAD</b>	<b>Gnd</b>	Exposed area on the bottom side of the package needs to be soldered to the ground plane of the board for optimum thermal and RF performance. Several vias should be located under the EPAD as shown in the recommended land pattern.

## Package Drawing

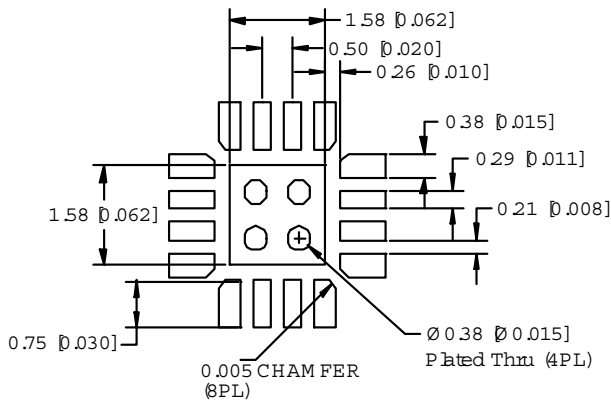
Dimensions in inches (millimeters)

Refer to drawing posted at [www.rfmd.com](http://www.rfmd.com) for tolerances.

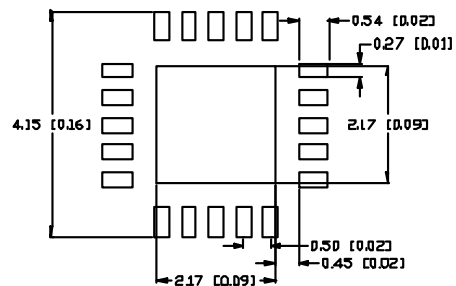


## Land Pattern and PCB Soldermask

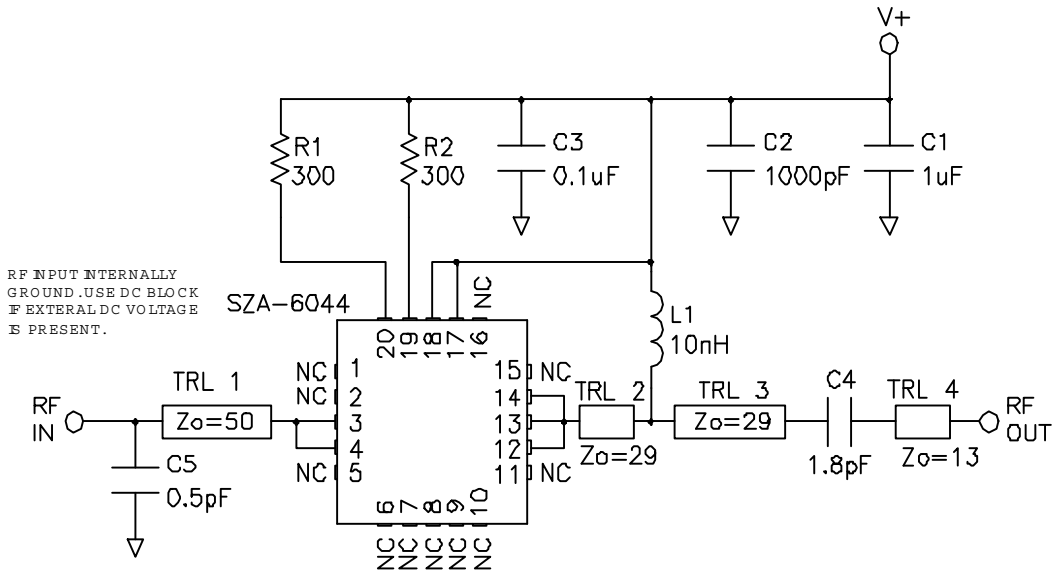
Recommended Land Pattern (dimensions in mm [in]):



Recommended PCB Soldermask (SMBOC) for Land Pattern (dimensions in mm [in]):

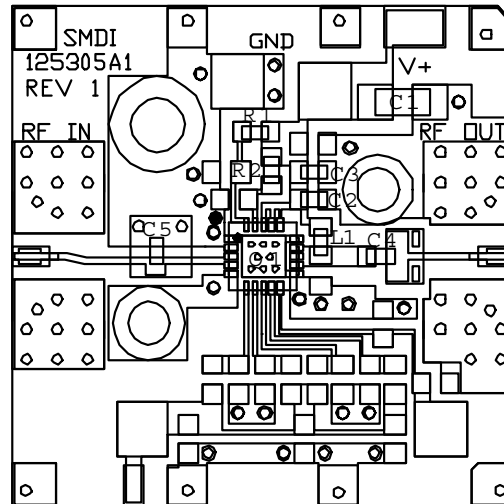


5.1GHz to 5.9GHz Evaluation Board Schematic For 5V Supply



Evaluation Board Layout and Bill of Materials

DESG	DESCRIPTION
Q1	SZA-6044
R1,2	300 OHM, 0603
C1	1uF CERAMIC CAP
C2	1000pF CAP, 0603
C3	0.1uF CAP, 0603
C4	1.8pF CAP, 0603
C5	0.5pF CAP, 0603
L1	10nH INDUCTOR, 0603 Toko LL1608-FS10NJ
TRL 1	Zo=50v ,54.2° @ 5.5GHz
TRL 2	Zo=29v ,22.3° @ 5.5GHz
TRL 3	Zo=29v ,38.4° @ 5.5GHz
TRL 4	Zo=13v ,16° @ 5.5GHz



Note: For 3.3V 140mA operation, lower V+ to 3.3V and change R1 and R2 to 50 ohm.  
 RF Performance at 3.3V, 140mA: Gain increases 0.5dB, IP3 drops ~3dB and P1dB drops ~3dB relative to 5V data.  
 Return loss is essentially unchanged relative to 5V data. Contact factory for more details.

### Part Identification

The part will be symbolized with an “SZA-6044” marking designator on the top surface of the package.

### Ordering Information

Part Number	Reel Size	Devices/Reel
SZA6044	13"	3000
SZA6044Z-EVB1	5.1GHz to 5.9GHz Frequency Range	