XE1283

433/868/915MHz low-power integrated UHF transceiver with low-power dedicated microcontroller

GENERAL DESCRIPTION

The XE1283 combines the functionality of a low-power transceiver operating in the 433, 868 and 915 MHz license-free ISM (Industry Scientific and Medical) frequency bands and an ultra low power microcontroller including the revolutionary BitJockey™, a UART-like peripheral dedicated to radio communication. The highly integrated architecture of the circuit allows for minimum external components while maintaining design flexibility. The XE1283 offers the advantage of high data rate communication at rates up to 152.3 kbit/s, without the need to modify the values or number of external components. Pre-routed internal connections and an available Application Program Interface (API) greatly simplify development while the BitJockey™ dedicated hardware frees up microcontroller resources available for implementing the application layer. The XE1283 is optimized for low power consumption while offering high RF output power and exceptional receiver sensitivity. The device is suitable for circuit applications which have to satisfy either the European (ETSI-300-220) or the North American (FCC part 15) regulatory standards.

APPLICATIONS

- Automated Meter Reading (AMR)
- Home Automation and Access Control
- Music, High-Quality Speech, and Data over RF
- Applications requiring Konnex-compatibility

KEY PRODUCT FEATURES

- Supply voltage down to 2.4V
- Small package size 10x10 mm

TRANSCEIVER

- Output power: up to +15 dBm into a 50Ω load
- Reception sensitivity: down to –113 dBm
- Low consumption:14 mA in Rx; 72 mA inTx@15 dBm
- Data rate from 1.2 to 152.3 kbit/s
- Konnex-compatible operation mode
- On-chip frequency synthesizer 500 Hz steps
- Continuous phase 2-level FSK modulation
- Received data pattern recognition (for microcontroller wake-up)
- Bit-Synchronizer for incoming data/clock synchronization and recovery
- RSSI & FEI

MICROCONTROLLER

- 8-bit RISC core; one cycle per instruction
- Up to 6 MIPS, 300 uA at 1 MIPS operation
- Up to 22 kbytes (8 k instructions) MTP,
- 512 bytes RAM
- 4 counters, PWM, UART, BitJockey™
- 4 low-power analog comparators

ORDERING INFORMATION

Part number	Temperature range	Package
XE1283I076TRLF	-40°C to 85°C	LFBGA72

Table of Contents

1 GLOBAL OVERVIEW

The XE1283 offers the unique advantage of combining an ultra low power high performance RF transceiver and a microcontroller on a single chip, reducing solution size, costs and development time.

As illustrated below, the XE1283 combines the functionalities of the XE1203F transceiver and the XE8806A/XE8807A "radio machine" microcontroller. It also includes the Semtech standard API bus (Application Program Interface) between the two functional blocks in help reduce schematic, layout, and software development.

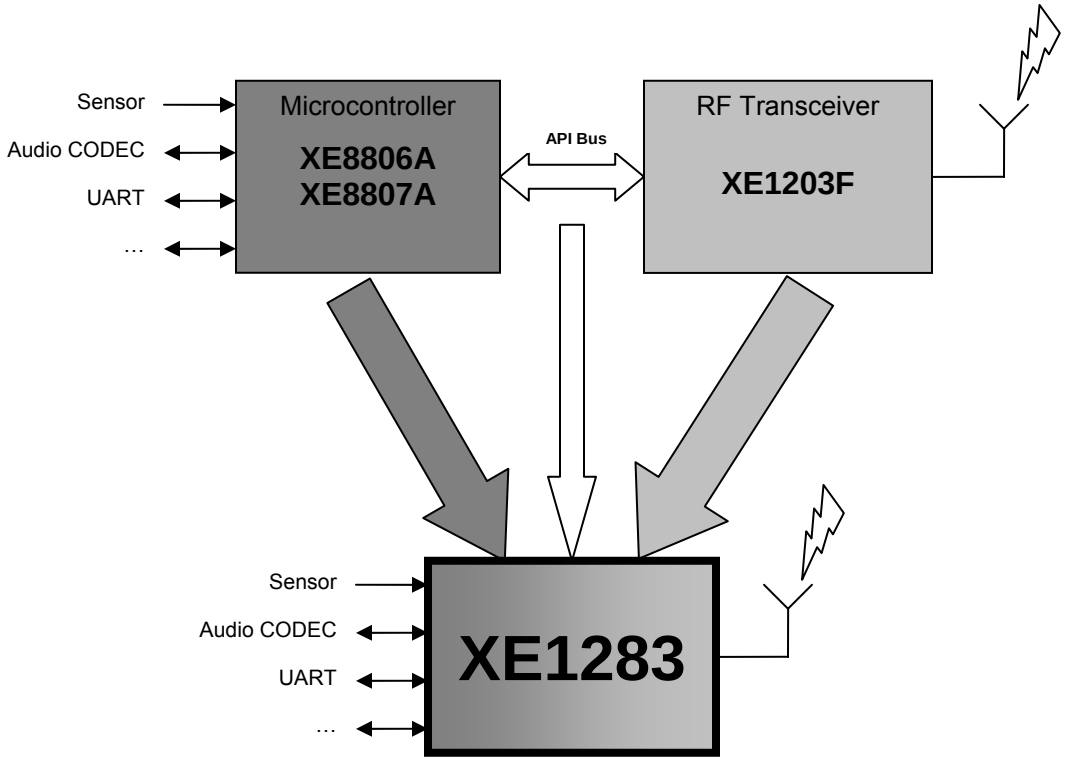


Figure 1: *XE1283 global structure*

The design sacrifices neither flexibility nor performance: both the XE1203F and XE8806A/XE8807A are high performance, low power, validated products and the quasi totality of the microcontroller resources remain available for upper level application design and development.

The XE1203F's high data rate and the XE8806A/XE8807A's BitJockey™ peripheral make the XE1283 ideal for embedded RF applications requiring high performance, small size and low power consumption.

2 PIN INFORMATION

2.1 PIN MAP

The XE1283 comes in an LFBGA-72 package with following pin map.

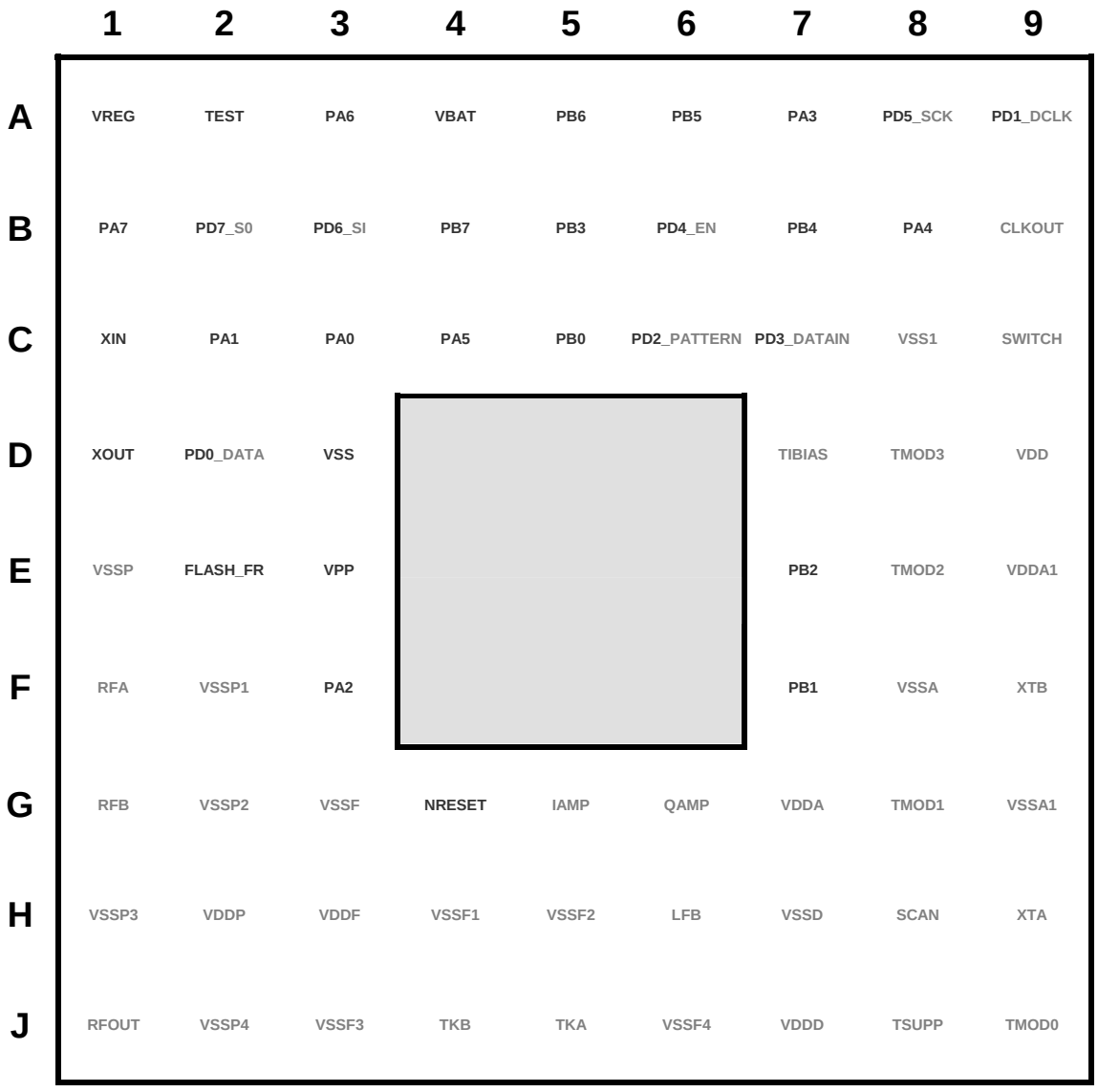


Figure 2: XE1283 pin map (Top view)

2.2 PIN DESCRIPTION

2.2.1 RF part

PIN	NAME	I/O	DESCRIPTION
D9	VDD	IN	VDD for low frequency digital blocks
J7	VDDD	IN	VDD for high frequency digital blocks
E9, G7	VDDA, VDDA1	IN	VDD for low frequency analog blocks
H3	VDDF	IN	VDD for high frequency analog blocks
H2	VDDP	IN	VDD for the power amplifier
C8	VSS1	IN	VSS for low frequency digital blocks
H7	VSSD	IN	VSS for high frequency digital blocks
F8, G9	VSSA, VSSA1	IN	VSS for low frequency analog blocks
G3, H4, H5, J3, J6	VSSF, VSSF(1:4)	IN	VSS for high frequency analog blocks
J2, E1, F2, G2, H1	VSSP, VSSP(1:4)	IN	VSS for the power amplifier
F1	RFA	IN	RF input
G1	RFB	IN	RF input
J1	RFOUT	OUT	RF output
J5	TKA	IN/OUT	VCO tank
J4	TKB	IN/OUT	VCO tank
H6	LFB	IN/OUT	Loop filter of the PLL
H9	XTA	IN/OUT	Crystal connection or input of external clock
F9	XTB	IN/OUT	Crystal connection
C9	SWITCH	IN/OUT	RF mode selection or indication
B9	CLKOUT	OUT	Output clock at quartz frequency divided by 4, 8, 16 or 32
G5	IAMP	OUT	Output of I low pass filter
G6	QAMP	OUT	Output of Q low pass filter
J8, D8, E8, G8, J9, D7, H8	TSUPP, TMOD(3:0), TIBIAS, SCAN	IN	Test pins. Connected to ground in normal operation.

2.2.2 API bus

PIN	NAME	I/O	DESCRIPTION
D2	PD0_DATA	OUT	Received RF data
A9	PD1_DCLK	OUT	Received RF clock
C6	PD2_PATTERN	OUT	Pattern recognition signal
C7	PD3_DATAIN	OUT	Transmitted RF data
B6	PD4_EN	OUT	Enable signal of the 3-wire interface
A8	PD5_SCK	OUT	Clock of the 3-wire interface
B3	PD6_SI	OUT	Data send to the transceiver via the 3-wire interface
B2	PD7_SO	OUT	Data read from the transceiver via the 3-wire interface

2.2.3 MicroController

PIN	NAME	I/O	DESCRIPTION
A4	VBAT	IN	Positive power supply
D3	VSS	IN	Negative power supply
A1	VREG	IN	Connection for the mandatory external capacitor of the voltage regulator
E3	VPP	IN	High voltage supply for flash memory programming
E2	FLASH_FR	IN	uC mode selection (‘0’=XE8807A ‘1’=XE8806A)
G4	NRESET	IN	Resets the circuit when the voltage is low
A2	TEST	IN	Sets the pin to flash programming mode
C1	XIN	IN/OUT	Crystal connection or input of external clock
D1	XOUT	IN/OUT	Crystal connection
B1, A3, C4, B8, A7, F3, C2, C3	PA(7:0)	IN	Parallel input port A pins
B4, A5, A6, B7, B5, E7, F7, C5	PB(7:0)	IN/OUT	Parallel I/O port B pins

3 ELECTRICAL CHARACTERISTICS

3.1 GLOBAL

3.1.1 Absolute maximum ratings

Stresses above those values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Description	Min.	Max.	Unit
Tmr1	Storage temperature (unprogrammed microcontroller)	-55	125	°C
Tmr2	Storage temperature (programmed microcontroller)	-40	85	°C

The device is ESD sensitive and should be handled with precaution.

3.1.2 Operating range

Symbol	Description	Min.	Max.	Unit
Top	Operating temperature	-40	85	°C

3.2 RF

3.2.1 Absolute maximum ratings

Stresses above those values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Description	Min.	Max.	Unit
VDDmr	Supply voltage	-0.5	3.9	V

3.2.2 Operating range

Symbol	Description	Min.	Max.	Unit
VDDop	Supply voltage	2.4	3.6	V
Clop	Load capacitance on digital ports	-	25	pF

3.2.3 Specifications

The table below gives the electrical specifications of the transceiver under the following conditions: Supply Voltage = 3.3 V, temperature = 25 °C, 2-level FSK without pre-filtering, fc = 915 MHz, Δf = 55 kHz, Bit rate = 4.8 kb/s, BW_{DSB} = 200 kHz, BER = 0.1 % (measured at the output of the bit synchronizer), LNA input and PA output matched to 50 Ω, environment as defined in section 5, unless otherwise specified.

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in sleep mode		-	0.2	1	µA
IDDST	Supply current in standby mode	Quartz oscillator (39 MHz) enabled	-	0.85	1.10	mA
IDDR	Supply current in receiver mode		-	14	17	mA
IDDT	Supply current in transmitter mode	RFOP = 5 dBm RFOP = 15 dBm	- -	33 72	40 85	mA mA
RFS	RF sensitivity	BR = 4.8 kbit/s Mode A	-	-113	-110	dBm
		BR = 4.8 kbit/s Mode B	-	-101	-98	dBm
		BR = 32.7 kbit/s Mode A	-	-109	-106	dBm
		BR = 32.7 kbit/s Mode B	-	-96	-93	dBm
		Δf = 200 kHz, BW_{DSB} = 600 kHz BR = 152.3 kbit/s Mode A	-	-101	-98	dBm
		BR = 152.3 kbit/s Mode B	-	-89	-86	dBm
RFSB	RF sensitivity with Barker Coding/decoding	BR = 1154 bit/s Mode A	-	-113	-110	dBm
		BR = 1154 bit/s Mode B	-	-100	-97	dBm
FDA	Frequency deviation	Programmable	1	-	255	KHz
CCR	Co-channel rejection		-13	-10	-	dBc
IIP3	Input intercept point	funw = f_{LO} + 10 MHz and f_{LO} + 19.945 MHz Mode A Mode B	 -27 -12	 -24 -9	 - -	 dBm dBm
BBW	Base band filter bandwidth DSB	Programmable	- -	200 600	- -	kHz kHz
ACR	Adjacent channel rejection	funw = f_{LO} + 650 kHz Pw= - 108 dBm, Mode A	45	48	-	dBc
BR	Bit rate	Programmable	1.2		152.3	kb/s
RFOP	RF output power	Programmable: RFOP1 RFOP2 RFOP3 RFOP4	-3 +2 +7 +12	0 +5 +10 +15	- - - -	dBm dBm dBm dBm
FR	Synthesizer frequency range	Programmable Each range with its own external components	433 868 902	- - -	435 870 928	MHz MHz MHz
TS_TR	Transmitter wake-up time	From oscillator enabled	-	150	250	µs
TS_RE	Receiver Baseband wake-up time	From oscillator enabled	-	0.5	0.8	ms
TS_RSSI	RSSI wake-up time	From receiver enabled	-	-	1	ms
TS_RSSIM	RSSI measurement time		-	0.5	-	ms

Symbol	Description	Conditions	Min	Typ	Max	Unit
TS_OS	Quartz oscillator wake-up time	Fundamental	-	0.3	0.5	ms
		3rd overtone	-	2.5	-	ms
TS_FEI	FEI wake-up time		-	-	2/BR	ms
TS_SYNC_AQ	Time for synchronization of the barker decoder	Input power of –106 dBm Data rate = 1154 bps Chip rate = 12.7 kcps From Rx enabled	-	5	-	ms
XTAL	Quartz oscillator frequency	Fundamental or 3rd overtone	-	39	-	MHz
FSTEP	Frequency synthesizer step	Exact step is XTAL / 77'824	-	500	-	Hz
VTHR	Equivalent input thresholds of the RSSI	Mode A				
		Low range:VTHR1	-	-95	-	dBm
		VTHR2	-	-90	-	dBm
		VTHR3	-	-85	-	dBm
		High range:VTHR1	-	-80	-	dBm
		VTHR2	-	-75	-	dBm
		VTHR3	-	-70	-	dBm
SPR	Spurious emission in receiver mode	(*)	-	-65	-	dBm
VIH	Digital input level high	in % VDD	75	-	-	%
VIL	Digital input level low	in % VDD	-	-	25	%
VOH	Digital output level high	in % VDD	75	-	-	%
VOL	Digital output level low	in % VDD	-	-	25	%

(*) SPR strongly depends on the design of the application board and the choice of the external components. Values down to -70 dBm can be achieved with careful design.

3.3 MICROCONTROLLER

3.3.1 Absolute maximum ratings

	Min.	Max.	Unit	Note
Voltage applied to VBAT with respect to VSS	-0.3	6.0	V	
Voltage applied to VPP with respect to VSS	VBAT-0.3	12	V	
Voltage applied to all pins except VPP and VBAT	VSS-0.3	VBAT+0.3	V	

Stresses beyond the absolute maximal ratings may cause permanent damage to the device. Functional operation at the absolute maximal ratings is not implied. Exposure to conditions beyond the absolute maximal ratings may affect the reliability of the device.

3.3.2 Operating range

	Min	Max	Unit	Note
Voltage applied to VBAT with respect to VSS	2.4	5.5	V	
Voltage applied to VBAT with respect to VSS during the flash programming	4.5	5.5	V	1
Voltage applied to VPP with respect to VSS	VBAT	11.5	V	
Voltage applied to all pins except VPP and VBAT	VSS	VBAT	V	
Capacitor on VREG	0.8	1.2	µF	
Retention time at 85°C	10		years	2
Retention time at 55°C	100		years	2
Number of programming cycles	10			3

1. During the programming of the device, the supply voltage should at least be equal to the supply voltage used during normal operation, and temperature between 10°C and 40°C.
2. Valid only if programmed using a programming tool that is qualified
3. Circuits can be programmed more than 10 times but in that case, the retention time is no longer guaranteed.

3.3.3 Current consumption

The tables below give the current consumption for the circuit in different configurations. The figures are indicative only and may change as a function of the actual software implemented in the circuit.

The peripherals (USRT, UART, CNT, VLD, CMPD) are disabled. The parallel ports are configured in input with pull up. Their pins are not connected externally.

Operation mode	CPU	RC	Xtal	Consumption	Comments	Note
High speed CPU	1 MIPS	1 MHz	Off	200 µA	2.4V<>5.5V, 27°C	1
				320 µA		2
				410 µA		3
				310 µA		4
Low speed CPU	.1 MIPS	100 kHz	Off	21 µA	2.4V <>5.5V, 27°C	1
				33 µA		2
				42 µA		3
Low power CPU	32 kIPS	Off	32 kHz	7.5 µA	2.4V <>5.5V, 27°C	1
				11.0 µA		2
				14.5 µA		3
Low power time keeping	HALT	Off	32 kHz	1.9 µA	2.4V <>5.5V, 27°C	
Fast wake-up time keeping	HALT	Ready	32kHz	2.3 µA	2.4V <>5.5V, 27°C	
Immediate wake-up time keeping	HALT	1 MHz	Off	35 µA	2.4V <>5.5V, 27°C	
VLD static current				15 µA	2.4V <>5.5V, 27°C	
CMPD static current				2 µA	2.4V <>5.5V, 27°C	

1. Software without data access
2. 100% low power RAM access

3. 100% RAM access
4. Typical software

Hints for low power operation:

1. Use the low power RAM instead of the RAM for all parameters that are accessed frequently. The average current consumption for the low power RAM is about 40 times lower than for the RAM.
2. Rather than using the circuit at low speed, it is better to use the circuit at higher speed and switch off the blocks when not needed.
3. The power consumption of the program memory is an important part of the overall power consumption.

3.3.4 Operating speed

The speed is not highly dependent upon the supply voltage. However, by limiting the temperature range, the speed can be increased. The minimal guaranteed speed as a function of the supply voltage and maximal temperature operating temperature is given below.

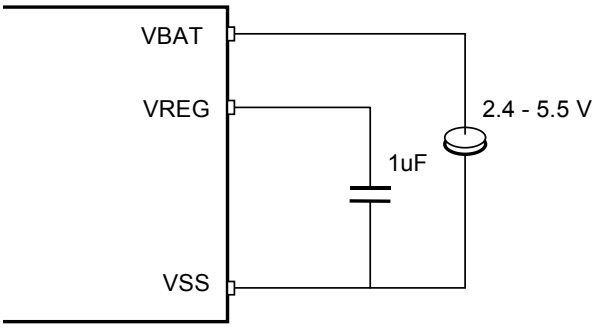


Figure 3: Supply configuration for circuit operation.

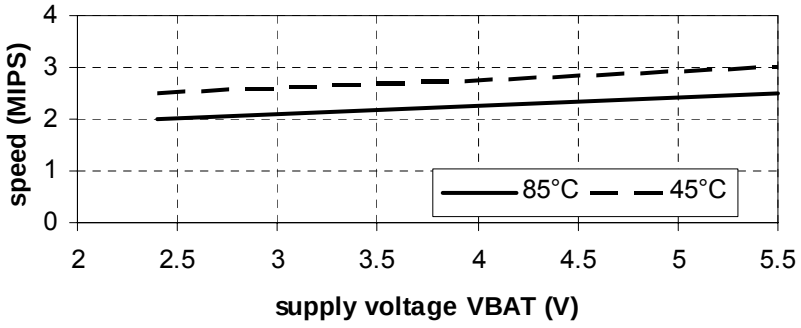


Figure 4: Guaranteed speed as a function of the supply voltage and maximal temperature with pin FLASH_FR set to VDD (XE8806A mode).

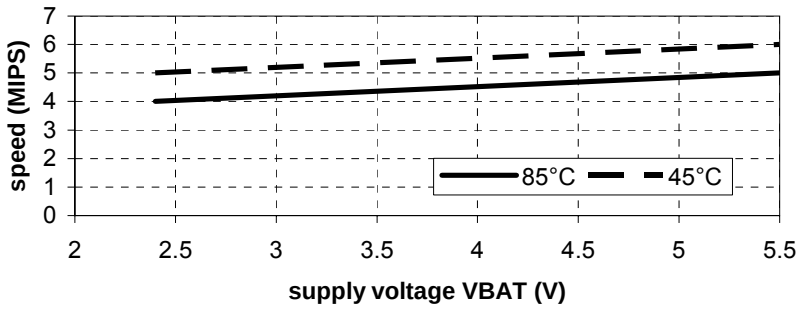


Figure 5: Guaranteed speed as a function of the supply voltage and maximal temperature with pin FLASH_FR set to VSS (XE8807A mode).

4 GENERAL DESCRIPTION

4.1 XE1203F BRIEF DESCRIPTION

The XE1203F is a direct conversion (Zero-IF) half-duplex data transceiver. It includes a receiver, a transmitter, a frequency synthesizer and some service blocks. The circuit operates in the three ISM frequency ranges (434 MHz, 868MHz and 915MHz) and uses 2-level FSK modulation. In a typical application, the XE1203F is programmed by the microcontroller through the 3-wire serial bus SI, SO, SCK to write to and read from the configuration registers.

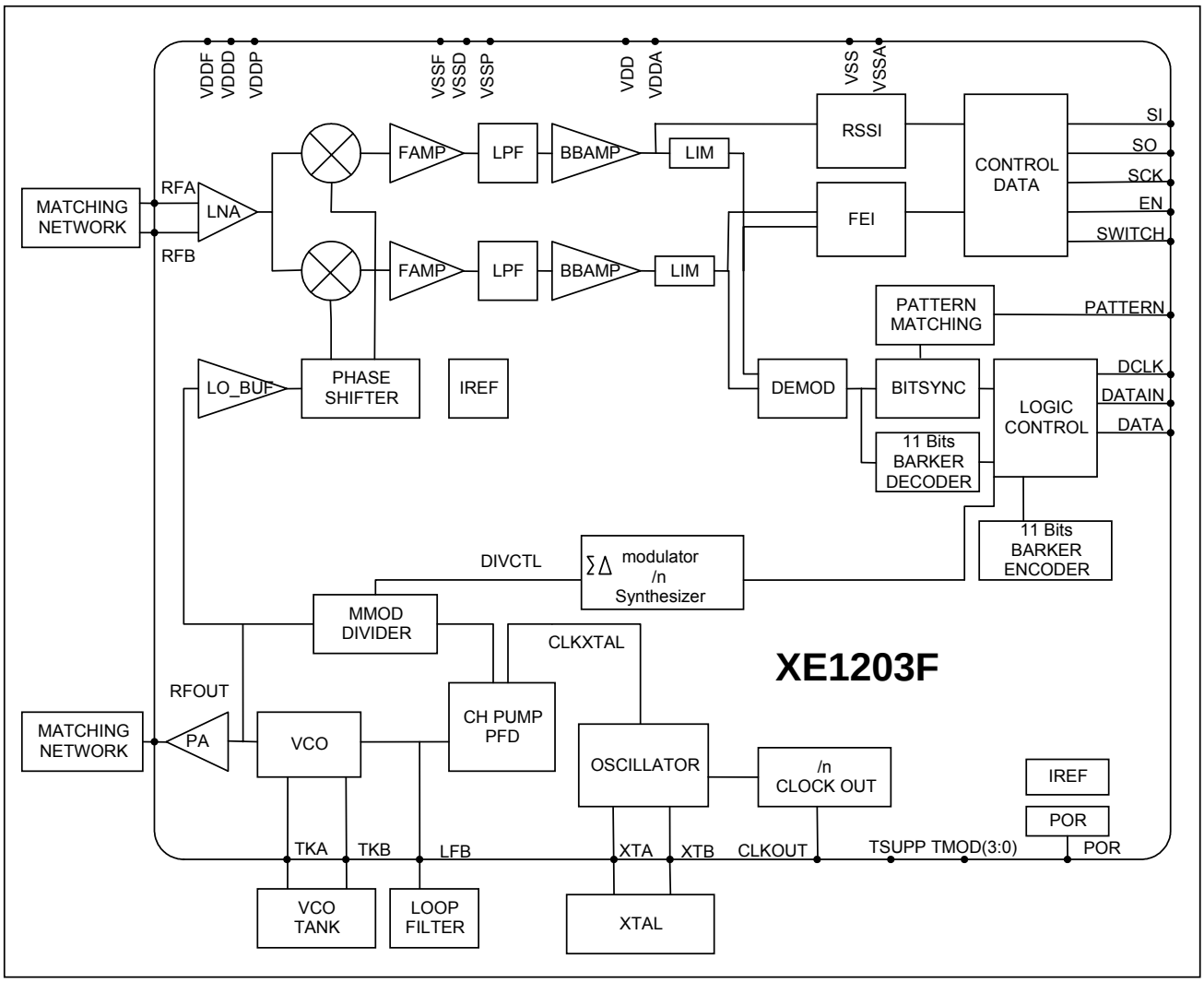


Figure 6: XE1203 functional block diagram

The XE1203F consists of 4 main functional blocks.

The receiver converts the incoming 2-level FSK modulated signal into a synchronized bit stream. The receiver is composed of a low-noise amplifier, down-conversion mixers, base band filters, base band amplifiers, limiters, demodulator and bit synchronizer. The bit synchronizer transforms the data output of the demodulator into a glitch-free bit

stream DATA and generates a synchronized clock DCLK to be used to sample the DATA signal easily without loading an external processor with heavy signal processing. In addition, the receiver includes a Received Signal Strength Indicator function (RSSI), a Frequency Error Indicator function (FEI) that gives indication about the frequency error of the local oscillator, and pattern recognition function to detect programmable reference word in the incoming bit stream. A user-selectable Barker coding/decoding block can be activated to spread the data with an 11-bit Barker code upon transmission and decode the data upon reception by making a correlation between the spread data and the same 11-bit Barker code. The bandwidth of the base-band filters, the frequency deviation of the expected incoming FSK signal as well as the bit rate of this bit stream are programmable.

The transmitter performs the modulation of the carrier by an input bit stream and the transmission of the modulated signal. The modulation is made directly through the frequency synthesizer. An on-chip power amplifier then amplifies the signal. The output power is programmable among 4 possible values. The frequency deviation and the bit rate for the transmit signal are the same as those programmed for the receiver section.

The frequency synthesizer generates the local oscillator (LO) signal for the receiver section as well as the FSK modulated signal for the transmitter section. The core of the synthesizer is implemented with a Delta-Sigma PLL architecture. The frequency is programmable with a step of 500 Hz in 3 frequency bands, 433-, 868-, and 915-MHz. This section includes a crystal oscillator whose signal is the reference for the PLL. This reference frequency can also be used as a reference clock for the external microcontroller through CLKOUT pin with a user selectable division ratio of 4,8,16 or 32.

The control block generates the control signals according to the setting in its set of configuration registers.

The service block performs all the necessary functions for the circuit to work properly, including the internal voltage and current sources.

For more complete information please refer to the XE1203F datasheet [1]. This can be found on the website at http://www.semtech.com

4.2 XE8806A/XE8807A BRIEF DESCRIPTION

The top level block schematic of the circuit is shown in figure below. The heart of the circuit consists of the Coolrisc816 CPU (central processing unit) core. This core includes an 8x8 multiplier and 16 internal registers.

The bus controller generates all control signals for access to all data registers other than the CPU internal registers.

The reset block generates the adequate reset signals for the rest of the circuit as a function of the set-up contained in its control registers. Possible reset sources are the power-on-reset (POR), the external pin NRESET, the watchdog (WD), a bus error detected by the bus controller or a programmable pattern on Port A.

The clock generation and power management block sets up the clock signals and generates internal supplies for different blocks. The clock can be generated from the RC oscillator (this is the start-up condition), the crystal oscillator (XTAL) or an external clock source (given on the XIN pin).

The test controller generates all set-up signals for different test modes. In normal operation, it is used as a set of 8 low power RAM. If power consumption is important for the application, the variables that need to be accessed frequently should be stored in these registers rather than in the RAM.

The IRQ handler routes the interrupt signals of the different peripherals to the IRQ inputs of the CPU core. It allows masking of the interrupt sources and it flags which interrupt source is active.

Events are generally used to restart the processor after a HALT period without jumping to a specified address, i.e. the program execution resumes with the instruction following the HALT instruction. The EVN handler routes the event signals of the different peripherals to the EVN inputs of the CPU core. It allows masking of the event sources and it flags which event source is active.

The instruction memory is a 22-bit wide flash memory. The maximal number of instructions in XE8806A mode (FLASH_FR='1') is 8192 while in XE8807A mode (FLASH_FR='0') it is 4096.

The data memory on this product is a 512 byte SRAM.

Port A is an 8 bit parallel input port. It can also generate interrupts, events or a reset. It can be used to input external clocks for the timer/counter/PWM block.

Port B is an 8 bit parallel IO port with analog capabilities. The USRT, UART, PWM and CMPD blocks also make use of this port.

Port D is originally a general purpose 8 bit parallel I/O port used in the XE1283 for the API bus.

The USRT (universal synchronous receiver/transmitter) contains some simple hardware functions in order to simplify the software implementation of a synchronous serial link.

The UART (universal asynchronous receiver/transmitter) contains a full hardware implementation of the asynchronous serial link.

The RFIF interface (or **BitJockey™**) is a serial interface dedicated to communication with RF circuits and more specifically with the XE1203 in the XE1283. From the CPU side, it very much looks like an ordinary UART but it also implements low level coding/decoding and frame synchronization. The input/output pins are multiplexed on port D.

The counters/timers/PWM can take their clocks from internal or external sources (on Port A) and can generate interrupts or events. The PWM is output on Port B.

The VLD (voltage level detector) detects the battery end of life with respect to a programmable threshold.

The CMPD contains a 4 channel comparator. It is intended to monitor analog or digital signals whilst having a very low power consumption.

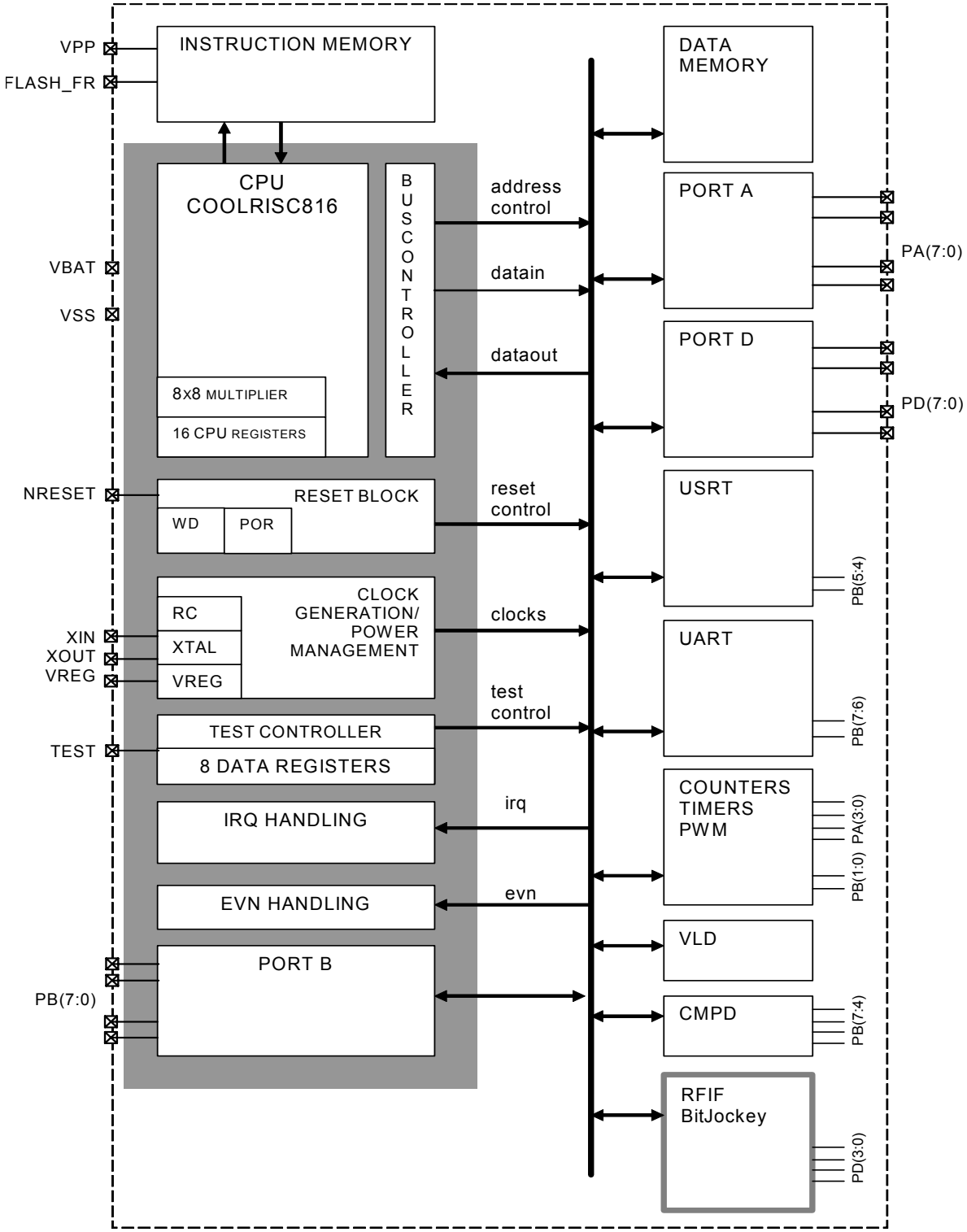


Figure 7: XE8806A/XE8807A functional block diagram

For more complete information please refer to the XE8806A/XE8807A datasheet [2]. This can be found on the website at http://www.semtech.com .

4.3 INTERNAL CONNECTIONS (API BUS)

XE1283 is not only made of an XE1203F and an XE8806A/XE8807A integrated together: it also includes internal connections - the API bus, which reduces schematic, layout, and software development by ensuring compatibility with the free API developed by Semtech.

These connections are illustrated in the figure below:

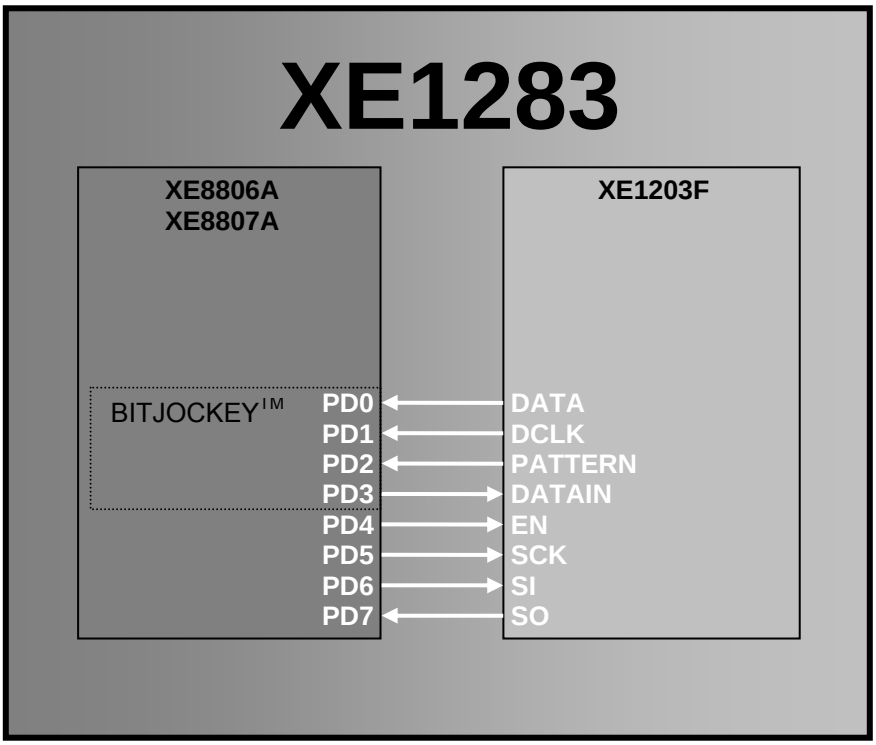


Figure 8: XE1283 internal connections

This bus enables one to send/receive RF data through the BitJockey™ and write/read the transceiver's configuration registers.

Notes:

- Pin DATA of the XE1203F is used in unidirectional mode
- Pin PD2 of the BitJockey™ is used as pattern detection input
- The BitJockey™'s PCM Encoder/Decoder should be programmed for NRZ data.
- Port B which has miscellaneous analog capabilities is kept completely available unless a Tx/Rx antenna switch is going to be driven.
- Like all the remaining pins of both chips, the internal connections are also bonded out for debug and flexibility purposes.

5 APPLICATION INFORMATION

5.1 EXTERNAL COMPONENTS

5.1.1 RF PART

5.1.1.1 Receiver matching network

The schematic of the recommended matching network at the input of the receiver is given below.

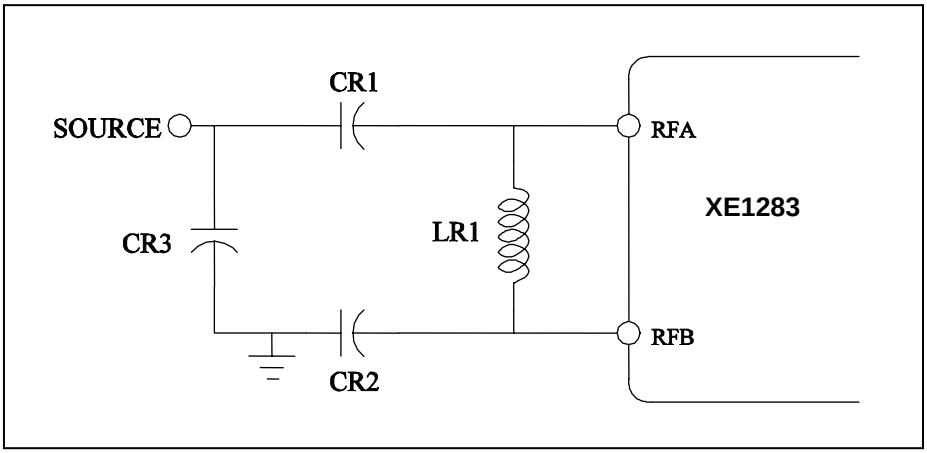


Figure 9: XE1283 Receiver matching network

The typical component values of the matching circuit are given below.

Name	Typical Value for 434MHz	Typical Value for 868 MHz	Typical Value for 915 MHz	Tolerance
CR1	1.5 pF	1.5 pF	1 pF	± 5 %
CR2	1.5 pF	1.2 pF	1 pF	± 5 %
CR3	NC	NC	NC	± 5 %
LR1	100 nH	27 nH	27 nH	± 5 %

5.1.1.2 Transmitter matching network

The schematic of the recommended matching network at the output of the transmitter is given below.

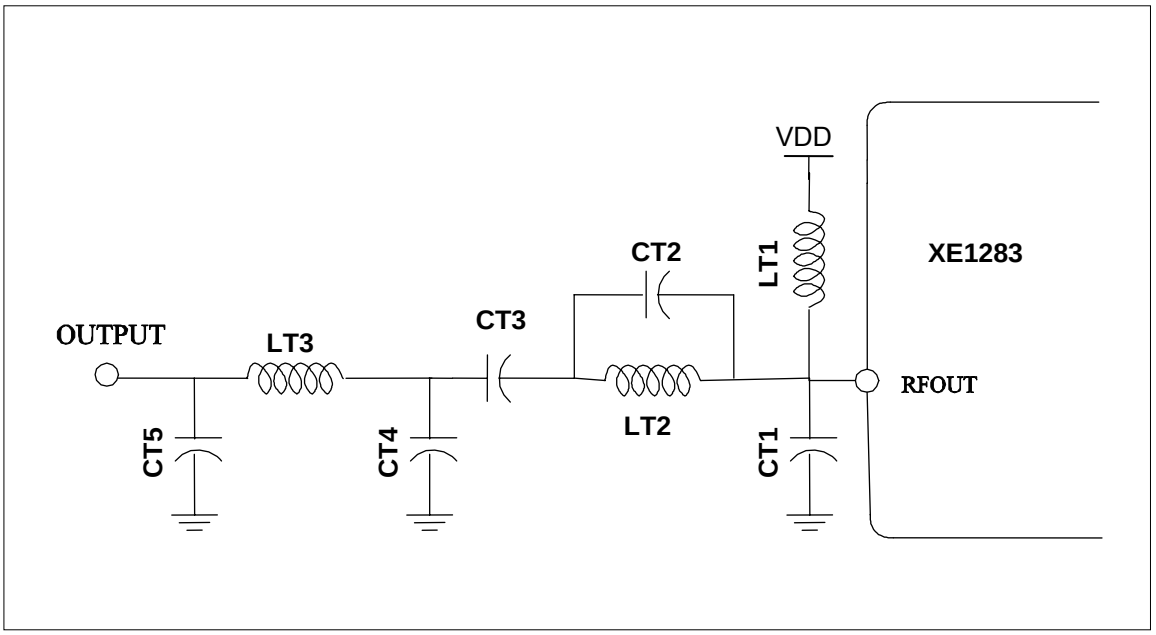


Figure 10: XE1283 Transmitter matching network

The typical component values of this matching circuit are given below.

Name	Typical Value for 434MHz	Typical Value for 868 MHz	Typical Value for 915 MHz	Tolerance
CT1	6.8 pF	1.5 pF	1.8 pF	± 5%
CT2	1 pF	0.56 pF	NC	± 5%
CT3	22 pF	15 pF	33 pF	± 5%
CT4	6.8 pF	3.3 pF	3.3 pF	± 5%
CT5	4.7 pF	2.2 pF	2.2 pF	± 5%
LT1	33 nH	39 nH	47 nH	± 5%
LT2	22 nH	10 nH	10 nH	± 5%
LT3	22 nH	8.2 nH	8.2 nH	± 5%

5.1.1.3 VCO Tank

The tank of the VCO will be implemented with one inductor in parallel with one capacitor. The recommended characteristics of these components must be as follows (if possible the capacitor has to be avoided):

Name	Typical Value for 434MHz	Typical Value for 868 MHz	Typical Value for 915 MHz	Tolerance
CV1	1 pF	NC	NC	± 5 %
LV1	33 nH	8.2 nH	6.8 nH	± 2 %

5.1.1.4 Loop filter

The loop filter of the frequency synthesizer is shown below.

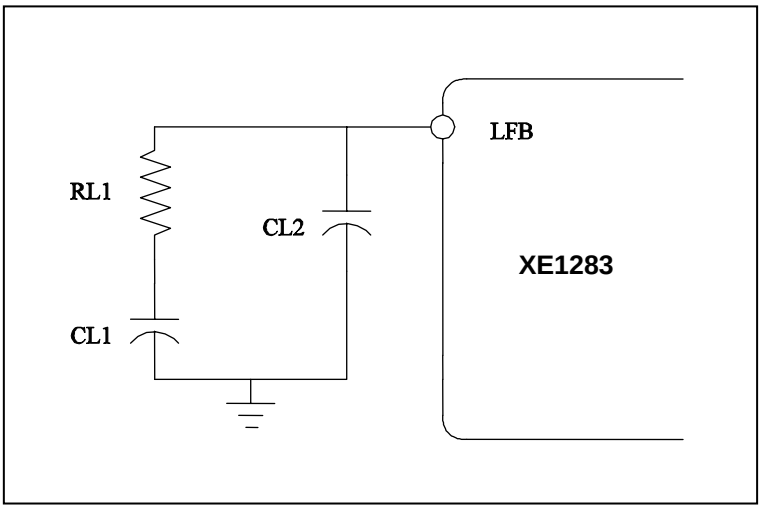


Figure 11: *XE1283 Loop filter*

The values recommended for applications using bit rates up to 38.4kbit/s are given in the table below.

Name	Typical Value for 434 MHz	Typical Value for 868 MHz	Typical Value for 915 MHz	Tolerance
CL1	22 nF	22 nF	22 nF	± 5%
CL2	1.2 nF	1.2 nF	1.2 nF	± 5%
RL1	560 Ω	470 Ω	470 Ω	± 5%

The values recommended for applications using bit rates higher than 38.4 kbit/s are given in the table below.

Name	Typical Value for 434MHz	Typical Value for 868 MHz	Typical Value for 915 MHz	Tolerance
CL1	3.3 nF	4.7 nF	4.7 nF	± 5%
CL2	220 pF	330 pF	330 pF	± 5%
RL1	1.2 kΩ	1 kΩ	1 kΩ	± 5%

5.1.1.5 Reference crystal

For narrow band applications, where users select the lowest frequency deviation and the narrowest baseband filter, the crystal for reference oscillator of the frequency synthesizer should have the following characteristics:

Name	Description	Min. value	Typ. value	Max. value
Fs	Nominal frequency	-	39.0 MHz (fundamental)	-
CL	Load capacitance for fs (on-chip)	-	8 pF (*)	-
Rm	Motional resistance	-	-	40 Ω
Cm	Motional capacitance	-	-	30 fF
C0	Shunt capacitance	-	-	7 pF (*)
Δfs(0)	Calibration tolerance at 25 °C	-	-	10 ppm
Δfs(ΔT)	Stability over temperature range (-40 °C to 85 °C)	-	-	10 ppm
Δfs(Δt)	Aging tolerance in first 5 years	-	-	5 ppm

(*) The on-chip oscillator mode is user-defined by programming ADParam_Xsel in the configuration register: the first for CL = 8 pF and C0 = 7 pF, and the second for CL = 8 pF and C0 = 3 pF; the latter will allow higher amplitude for the internal signal with a slightly lower consumption. For the explanation of this parameter ADParam_Xsel, please refer to the XE1203F datasheet.

The electrical specifications given in section 3.2.3 are valid for a crystal having the specifications given in the table above. For wide band applications requiring less frequency stability, the values for Δfs(0), Δfs(ΔT), and/or Δfs(Δt) can be relaxed. In this case foffset + BWssb should be lower than BWfilter, where foffset is the offset (error) on the carrier frequency (the sum of Δfs(0), Δfs(ΔT), and/or Δfs(Δt)), BWssb is the single side-band bandwidth of the signal, and BWfilter is the single side-band bandwidth of the base-band filter.

The overtone crystal usage can result in higher oscillator start-up time than fundamental mode. The overtone crystal should be designed for Cload = 8 to 10pF and has parameters of Rm < 60 ohm, C0 < 7pF.

5.1.2 MicroController

5.1.2.1 Vreg capacitor

This capacitor is compulsory and must be connected between pin VREG and ground.

Description	Min	Typ	Max	Unit
Capacitor on VREG	0.8	1	1.2	µF

5.1.2.2 Reference crystal

This reference crystal must be mounted between XIN and XOUT and is used by the software DFLL to set precisely the RC's frequency.

The crystal oscillator has been designed for a crystal with the specifications given below. The oscillator precision can only be guaranteed for this crystal.

Symbol	Description	Min	Typ	Max	Unit
Fs	Resonance frequency	-	32768	-	Hz
CL	CL for nominal frequency	-	8.2	15	pF
Rm	Motional resistance	-	40	100	kΩ
Cm	Motional capacitance	1.8	2.5	3.2	fF
C0	Shunt capacitance	0.7	1.1	2.0	pF
Rmp	Motional resistance of 6^{th} overtone (parasitic)	4	8	-	kΩ
Q	Quality factor	30k	50k	400k	-

For safe operation, low power consumption and to meet the specified precision, careful board layout is required:

Keep lines XIN and XOUT short and insert a VSS line in between them.
Connect the crystal package to VSS.
No noisy or digital lines near XIN or XOUT.
Insert guards where needed.
Respect the board specifications below.

Symbol	Description	Min	Typ	Max	Unit
Rh_xin	Resistance XIN-VSS	10			MΩ
Rh_xout	Resistance XOUT-VSS	10			MΩ
Rh_xin_xout	Resistance XIN-XOUT	50			MΩ
Cp_xin	Capacitance XIN-VSS	0.5		3.0	pF
Cp_xout	Capacitance XOUT-VSS	0.5		3.0	pF
Cp_xin_xout	Capacitance XIN-XOUT	0.2		1.0	pF

The oscillator characteristics are given below. The characteristics are valid only if the crystal and board layout meet the specifications above.

Symbol	Description	Min	Typ	Max	Unit
f_{Xtal}	Nominal frequency		32768		Hz
St_xtal	Start-up time		1	2	s
Fstab	Frequency deviation	-100		300	ppm

Note: Fstab gives the relative frequency deviation from nominal value for a crystal with CL=8.2 pF and within the temperature range -40°C to 85°C. The crystal tolerance, crystal aging and crystal temperature drift are not included in this figure.

5.2 PROGRAMMING

Programming of XE1283's integrated microcontroller can be done with the XE8000MP board through one of its "In-Circuit programming connectors".
On the other side, the XE1283 target board should have the programming connector described below or equivalent.

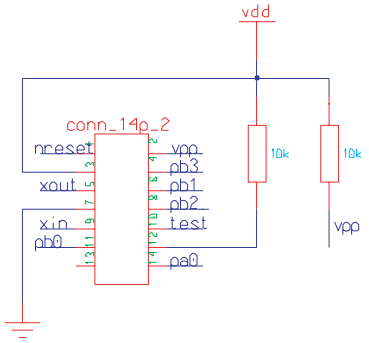


Figure 12: XE1283 programming connector

5.3 APPLICATION PROGRAM INTERFACE (API)

Application Program Interface (API) is a set of basic drivers for XE8000 developers to easily drive the XE1200 series transceivers. In our case XE8806A/XE8807A drives the XE1203F. This API allows easy and fast start to development, using standard calls to low level functions (Send RF Frame, Receive RF Frame, Write Register, Read Register …).

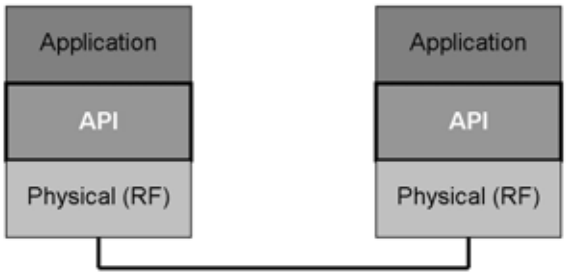


Figure 13: API layer

These functions, written in C language, are completely free and open source, they will allow the developers to replace them, if necessary, with optimized object code from third parties through wrapper function.

Because the API is provided in source code, it also allows the developers to see how the transceiver works and modify or optimize the code to their needs.

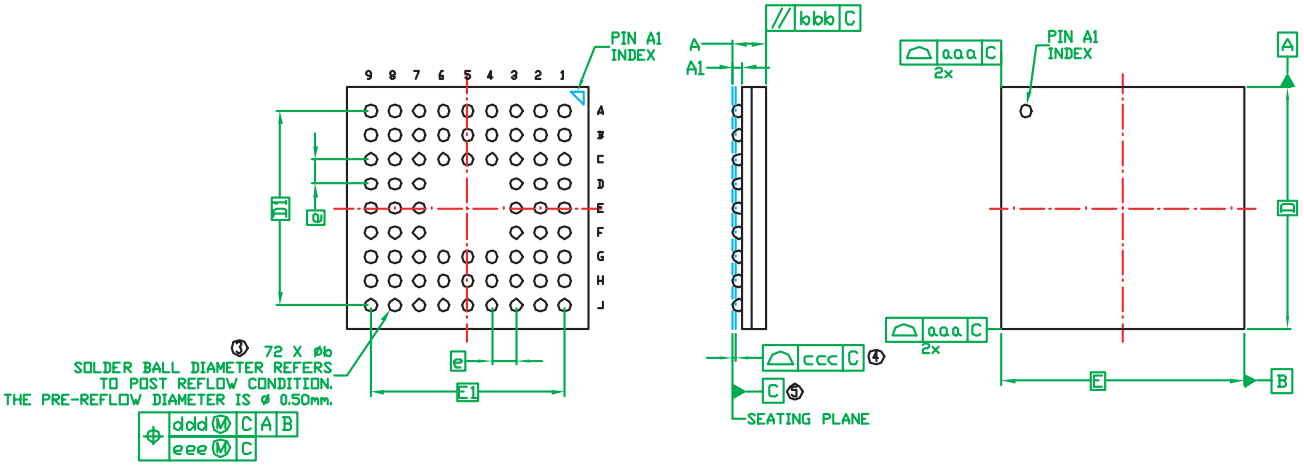
Application Program Interface greatly simplifies development while the BitJockey™ leaves microcontroller resources quasi completely available for implementing the application layer.

Complete source code is available on the Semtech web site at the following address: http://www.semtech.com

In an XE1283 based application one should just copy and include the XE1203F drivers to the RIDE project and set the microcontroller target to XE8806A or XE8807A.
For more complete information please refer to the technical note TN8000.18 [3].

6 PACKAGING INFORMATION

XE1283 comes in a 72-pin LFBGA 10x10 as shown in figure below.



DIMENSIONAL REFERENCES Units mm

REF.	Min.	Nom.	Max.
A	1.28	1.36	1.44
A1	0.35	0.40	0.45
b	0.47	0.52	0.57
D		10.00 BSC	
E		10.00 BSC	
D1		8.00 BSC	
E1		8.00 BSC	
e		1.00 BSC	

DIMENSIONAL REFERENCES Units mm

REF.	TOLERANCE OF FORM AND POSITION
aaa	0.20
bbb	0.25
ccc	0.20
ddd	0.25
eee	0.10

Figure 14: *Package dimensions*

7 REFERENCES

[1] XE1203F datasheet:
[2] XE8806A/XE8807A datasheet:
[3] TN8000.18. XE8000 driving XE1200 transceivers. Standard API Definitions:

http://www.semtech.com

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