Low Power Mixer/Limiter/RSSI 3 V Receiver IF Subsystem

AD608

FEATURES

Mixer
- **−15 dBm, 1 dB compression point**
- **−5 dBm IP3**
- **24 dB conversion gain**
- **>500 MHz input bandwidth**

Logarithmic/limiting amplifier
- **80 dB RSSI range**
- **±3° phase stability over 80 dB range**

Low power
- **21 mW at 3 V power consumption**
- **CMOS-compatible power-down to 300 µW typical**
- **200 ns enable/disable time**

APPLICATIONS

PHS, GSM, TDMA, FM, or PM receivers
Battery-powered instrumentation
Base station RSSI measurements

GENERAL DESCRIPTION

The AD608 provides a low power, low distortion, low noise mixer as well as a complete, monolithic logarithmic/limiting amplifier that uses a successive-detection technique. In addition, the AD608 provides both a high speed received signal strength indicator (RSSI) output with 80 dB dynamic range and a hard-limited output. The RSSI output is from a two-pole postdemodulation low-pass filter and provides a loadable output voltage of 0.2 V to 1.8 V. The AD608 operates from a single 2.7 V to 5.5 V supply at a typical power level of 21 mW at 3 V.

The RF and local oscillator (LO) bandwidths both exceed 500 MHz. In a typical IF application, the AD608 can accept the output of a 240 MHz surface acoustic wave (SAW) filter and down-convert it to a nominal 10.7 MHz IF with a conversion gain of 24 dB (Z_{IF} = 165 Ω). The AD608 logarithmic/limiting amplifier section handles any IF from low frequency (LF) up to 30 MHz.

The mixer is a doubly balanced gilbert-cell mixer and operates linearly for RF inputs spanning −95 dBm to −15 dBm. It has a nominal −5 dBm third-order intercept. An on-board LO pre-amplifier requires only −16 dBm of LO drive. The current output of the mixer drives a reverse-terminated, industry-standard 10.7 MHz, 330 Ω filter.

The nominal logarithmic scaling is such that the output is +0.2 V for a sinusoidal input to the IF amplifier of −75 dBm and +1.8 V at an input of +5 dBm; over this range, the logarithmic conformance is typically ±1 dB. The logarithmic slope is proportional to the supply voltage. A feedback loop automatically nulls the input offset of the first stage down to the submicrovolt level.

The AD608 limiter output provides a hard-limited signal output at 400 mV p-p. The voltage gain of the limiting amplifier to this output is more than 100 dB. Transition times are 11 ns and the phase is stable to within ±3° at 10.7 MHz for signals from −75 dBm to +5 dBm.

The AD608 is enabled by a CMOS logic-level voltage input, with a response time of 200 ns. When disabled, the standby power is reduced to 300 µW within 400 ns.

The AD608 is specified for the industrial temperature range of −25°C to +85°C for 2.7 V to 5.5 V supplies and −40°C to +85°C for 3.0 V to 5.5 V supplies. This device comes in a 16-lead plastic SOIC.

FUNCTIONAL BLOCK DIAGRAM

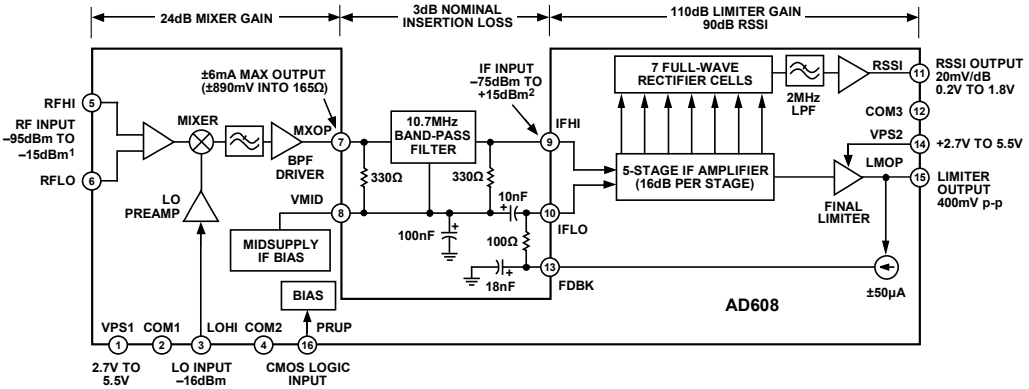

Figure 1.

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2/09—Rev. B to Rev. C

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SPECIFICATIONS

T_A = 25°C, supply = 3 V, dBm is referred to 50 Ω, unless otherwise noted.

Table 1.

Parameter	Conditions[1]	Min	Typ	Max	Unit
MIXER PERFORMANCE					
RF and LO Frequency Range			500		MHz
LO Power	Input terminated in 50 Ω		−16		dBm
Conversion Gain	Driving doubly terminated 330 Ω IF filter, Z_{IF} = 165 Ω	19	24	28	dB
Noise Figure	Matched input, f_{RF} = 100 MHz		11		dB
	Matched input, f_{RF} = 240 MHz		16		dB
1 dB Compression Point	Input terminated in 50 Ω		−15		dBm
Third-Order Intercept	f_{RF} = 240 MHz and 240.02 MHz, f_{LO} = 229.3 MHz		−5		dBm
Input Resistance	f_{RF} = 100 MHz (see Table 5)		1.9		kΩ
Input Capacitance	f_{RF} = 100 MHz (see Table 5)		3		pF
LIMITER PERFORMANCE					
Gain	Full temperature and supply range		110		dB
Limiting Threshold	3° rms phase jitter at 10.7 MHz		−75		dBm
	280 kHz IF bandwidth				
Input Resistance			10		kΩ
Input Capacitance			3		pF
Phase Variation	−75 dBm to +5 dBm IF input signal at 10.7 MHz		±3		Degrees
DC Level	Center of output swing (VPOS – 1 V)		2		V
Output Level	Limiter output driving 5 kΩ load		400		mV p-p
Rise and Fall Times	Driving a 5 pF load		11		ns
Output Impedance			200		Ω
RSSI PERFORMANCE	At 10.7 MHz				
Nominal Slope	At VPOS = 3 V; proportional to VPOS	17.27	20	23.27	mV/dB
Nominal Intercept			−85		dBm
Minimum RSSI Voltage	−75 dBm input signal		0.2		V
Maximum RSSI Voltage	+5 dBm input signal		1.8		V
RSSI Voltage Intercept	0 dBm input signal	1.57		1.82	V
Logarithmic Linearity Error	−75 dBm to +5 dBm input signal at IFHI		±1		dB
RSSI Response Time	90% RF to 50% RSSI		200		ns
Output Impedance	At midscale		250		Ω
POWER-DOWN INTERFACE					
Logic Threshold	System active on logic high		1.5		V
Input Current	For logic high		75		mA
Power-Up Response Time	Active limiter output		200		ns
Power-Down Response Time	To 200 µA supply current		400		ns
Power-Down Current			100		µA
POWER SUPPLY					
Operating Range	−25°C to +85°C	2.7		5.5	V
	−40°C to +85°C	3.0		5.5	V
Powered Up Current	VPOS = 3 V		7.3		mA
OPERATING TEMPERATURE					
T_{MIN} to T_{MAX}	VPOS = 2.7 V to 5.5 V	−25		+85	°C
	VPOS = 3.0 V to 5.5 V	−40		+85	°C

[1] VPOS is used to refer collectively to the VPS1 and VPS2 pins.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltages VPS1, VPS2	+6 V
Internal Power Dissipation	600 mW
Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3.

Package Type	θ_{JA}	Unit
16-Lead SOIC	110	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

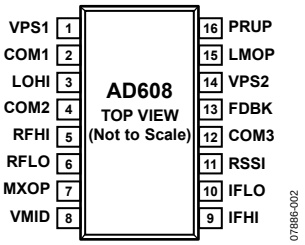


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VPS1[1]	Positive Supply Input
2	COM1	Common
3	LOHI	Local Oscillator Input Connection
4	COM2	Common
5	RFHI	RF Input, Noninverting
6	RFLO	RF Input, Inverting
7	MXOP	Mixer Output
8	VMID	Midpoint Supply Bias Output
9	IFHI	IF Input, Noninverting
10	IFLO	IF Input, Inverting
11	RSSI	Received Signal Strength Indicator Output
12	COM3	Output Common
13	FDBK	Offset-Null Feedback Loop Output
14	VPS2[1]	Limiter Positive Supply Input
15	LMOP	Limiter Output
16	PRUP	Power-Up

[1] VPOS is used to refer collectively to the VPS1 and VPS2 pins in this data sheet.

TYPICAL PERFORMANCE CHARACTERISTICS

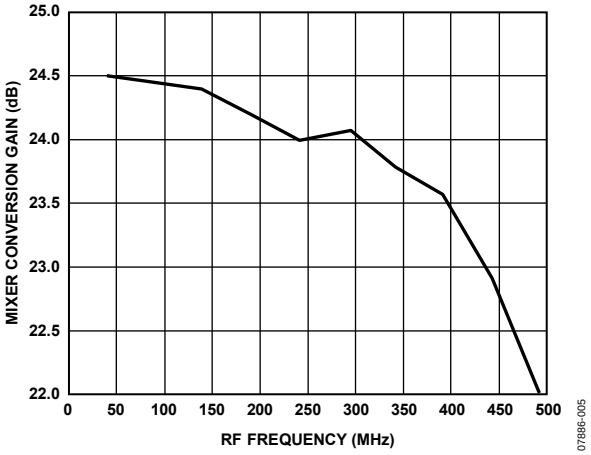


Figure 3. Mixer Conversion Gain vs. RF Frequency

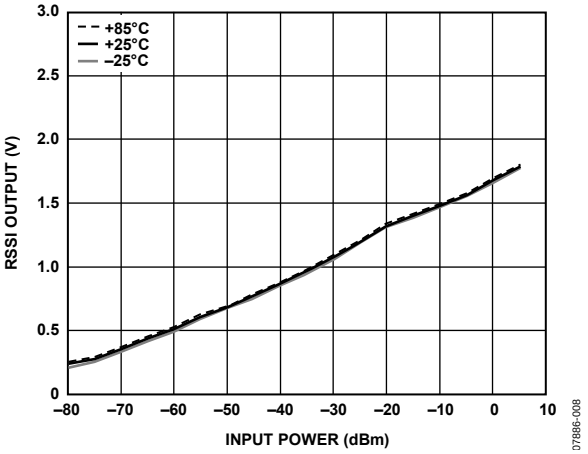


Figure 6. IF RSSI Output vs. Input Power and Temperature, 3 V Supply (See Figure 15)

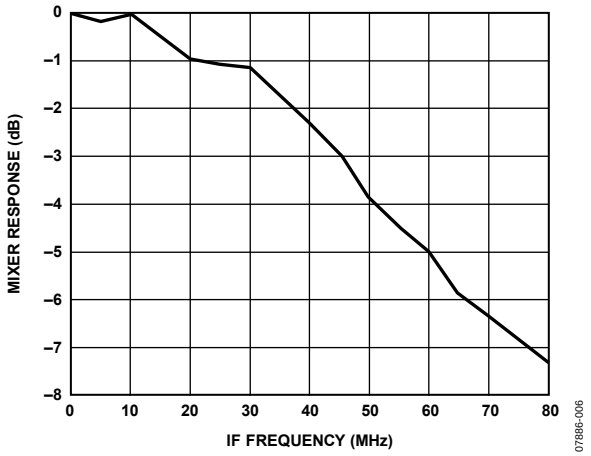


Figure 4. Mixer IF Port Bandwidth

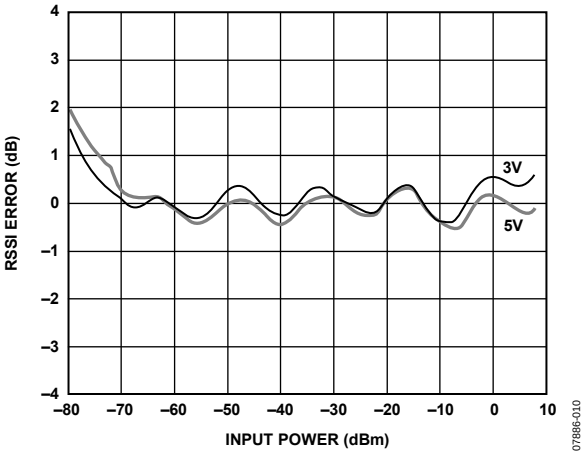


Figure 7. RSSI Error vs. Input Power (See Figure 15)

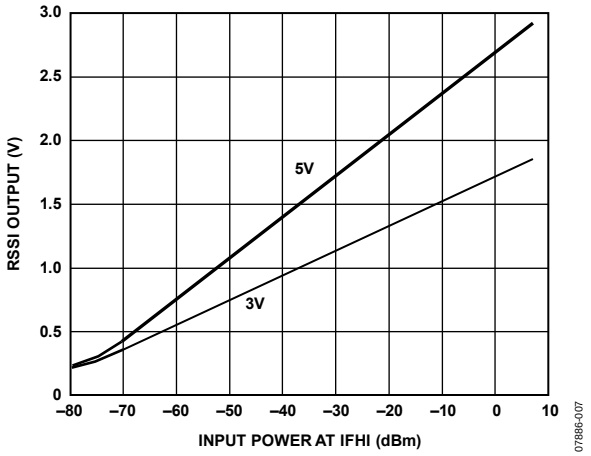


Figure 5. IF RSSI Output vs. Input Power at IFHI and Supply Voltage, Ambient Temperature (See Figure 15)

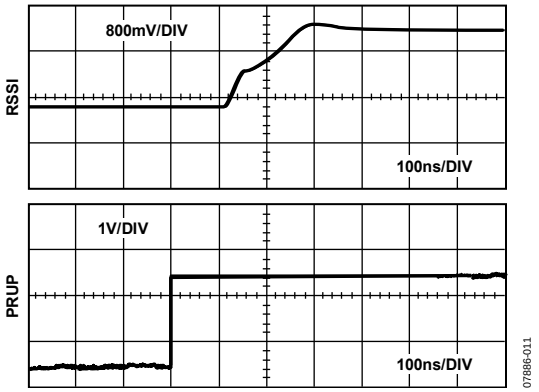


Figure 8. RSSI Power-Up Response (See Figure 19)

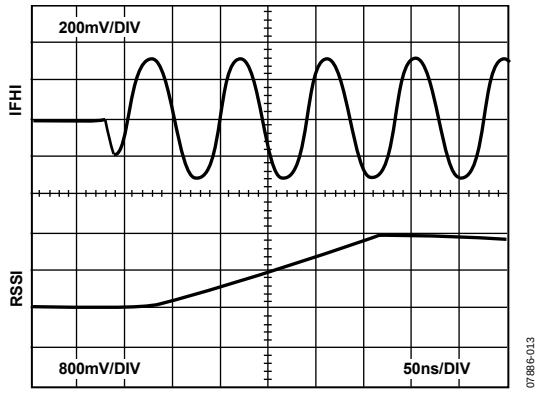


Figure 9. RSSI Pulse Response/RSSI Rise Time
(See Figure 16)

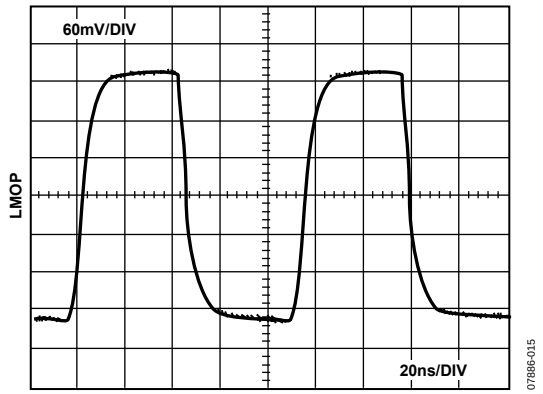


Figure 10. Limiter Rise and Fall Times
(See Figure 20)

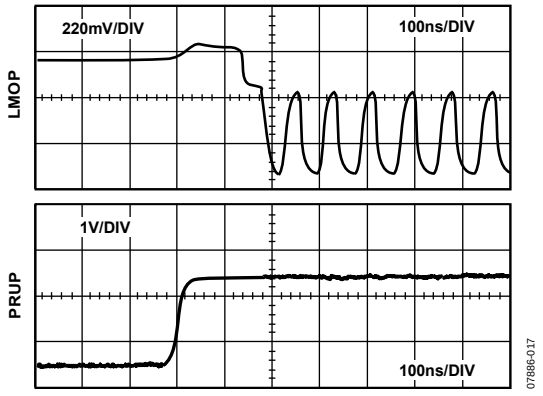


Figure 11. Limiter Power-Up Response Time
(See Figure 17)

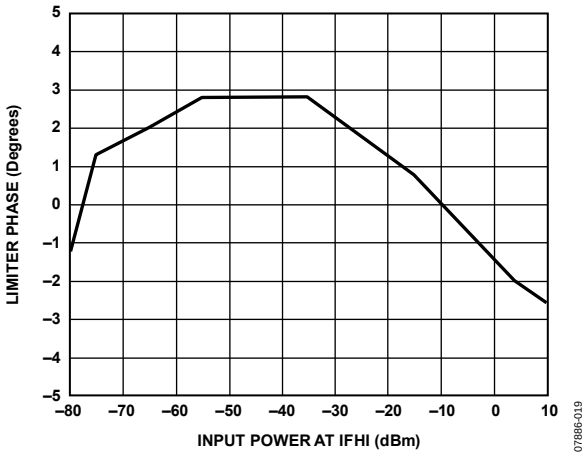


Figure 12. Limiter Phase Performance vs. Input Power at IFHI
(See Figure 21)

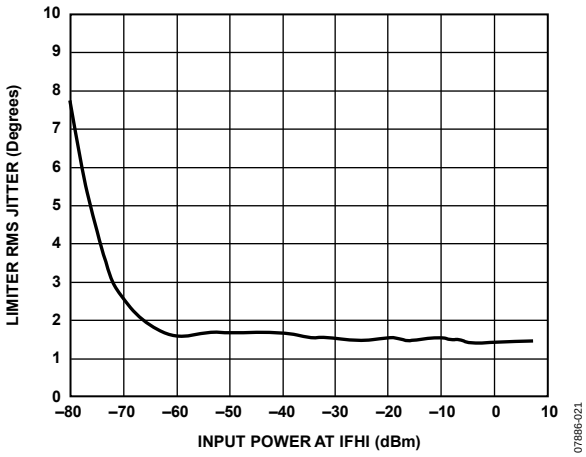


Figure 13. Limiter RMS Jitter Performance vs. Input Power at IFHI
(See Figure 21)

TEST CIRCUITS

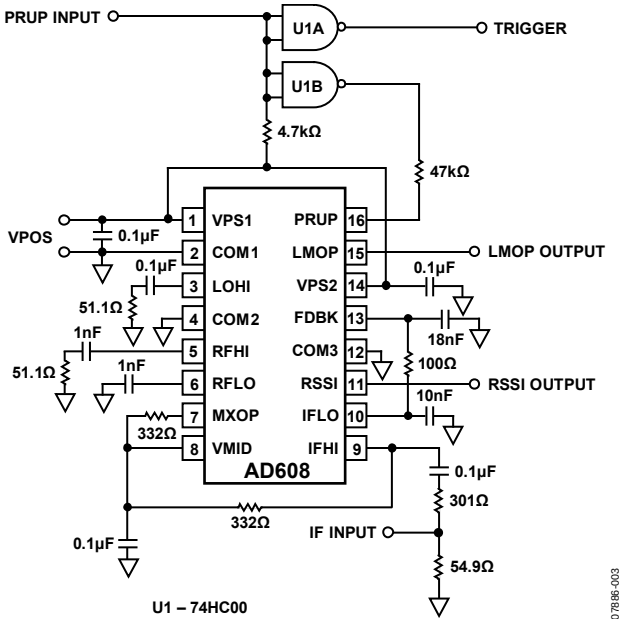


Figure 14. IF Test Board Schematic

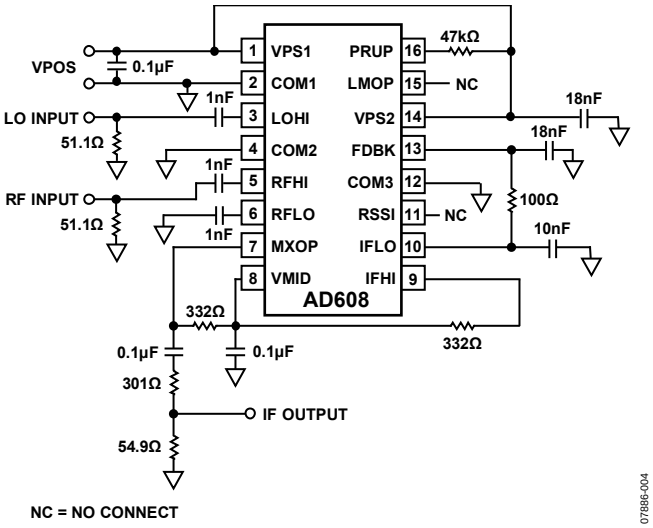


Figure 18. Mixer Test Board Schematic

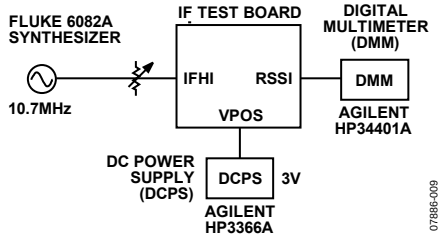


Figure 15. Test Circuit for IF RSSI Output vs. Input Power at IFHI and Supply Voltage, Ambient Temperature (Figure 5); IF RSSI Output vs. Input Power and Temperature, 3 V Supply (Figure 6); and RSSI Error vs. Input Power (Figure 7)

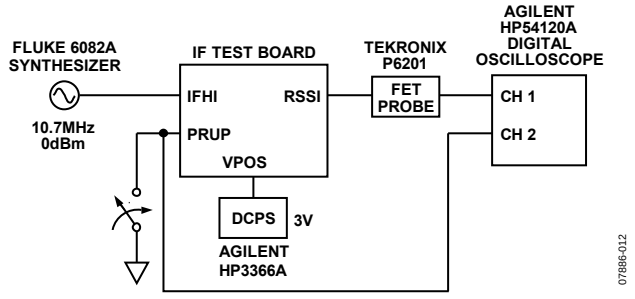


Figure 19. Test Circuit for RSSI Power-Up Response (Figure 8)

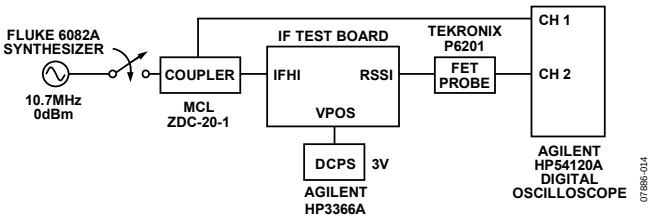


Figure 16. Test Circuit for RSSI Pulse Response/RSSI Rise Time (Figure 9)

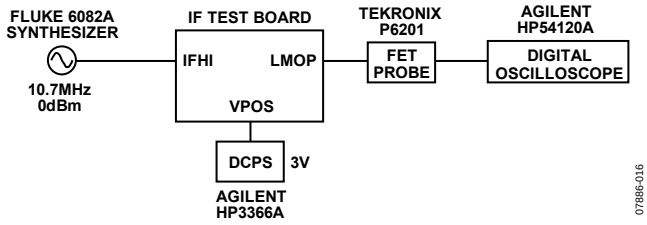


Figure 20. Test Circuit for Limiter Rise and Fall Times (Figure 10)

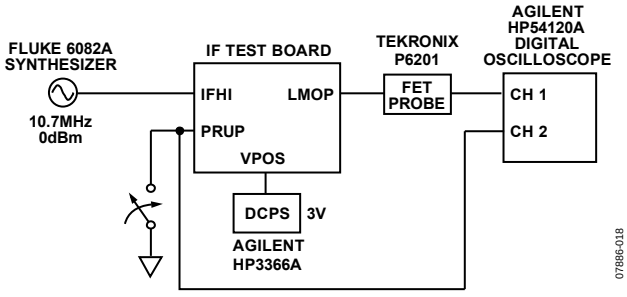


Figure 17. Test Circuit for Limiter Power-Up Response Time (Figure 11)

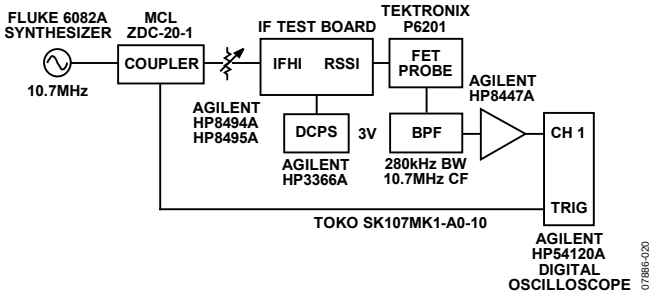


Figure 21. Test Circuit for Limiter Phase Performance vs. Input Power at IFHI (Figure 12) and Limiter RMS Jitter Performance vs. Input Power at IFHI (Figure 13)

THEORY OF OPERATION

The AD608 consists of a mixer followed by a logarithmic IF strip with RSSI and hard-limited outputs (see Figure 22).

MIXER

The mixer is a doubly balanced, modified gilbert-cell mixer. Its maximum input level for linear operation is either ±56.2 mV, regardless of the impedance across the mixer inputs, or −15 dBm for a 50 Ω input termination. The input impedance of the mixer can be modeled as a simple parallel RC network; the resistance and capacitance values vs. frequency are listed in Table 5. The bandwidth from the RF input to the IF output at the MXOP pin is −1 dB at 30 MHz and then rapidly decreases as frequency increases (see Figure 4).

MIXER GAIN

The conversion gain of the mixer is the product of its transconductance and the impedance seen at Pin MXOP. For a 330 Ω parallel-terminated filter at 10.7 MHz, the load impedance is 165 Ω, the gain is 24 dB, and the output is 15.85 × 56.2 mV (or ±891 mV) centered on the midpoint of the supply voltage. For other load impedances, the expression for the gain in decibels is

$$G_{dB} = 20 \log_{10}(0.0961\ R_L)$$

where:
G_{dB} is the gain in decibels.
R_L is the load impedance at Pin MXOP.

The gain of the mixer can be increased or decreased by changing R_L. The limitations on the gain are the ±6 mA maximum output current at MXOP and the maximum allowable voltage swing at Pin MXOP, which is ±1.0 V for a 3 V supply or 5 V supply.

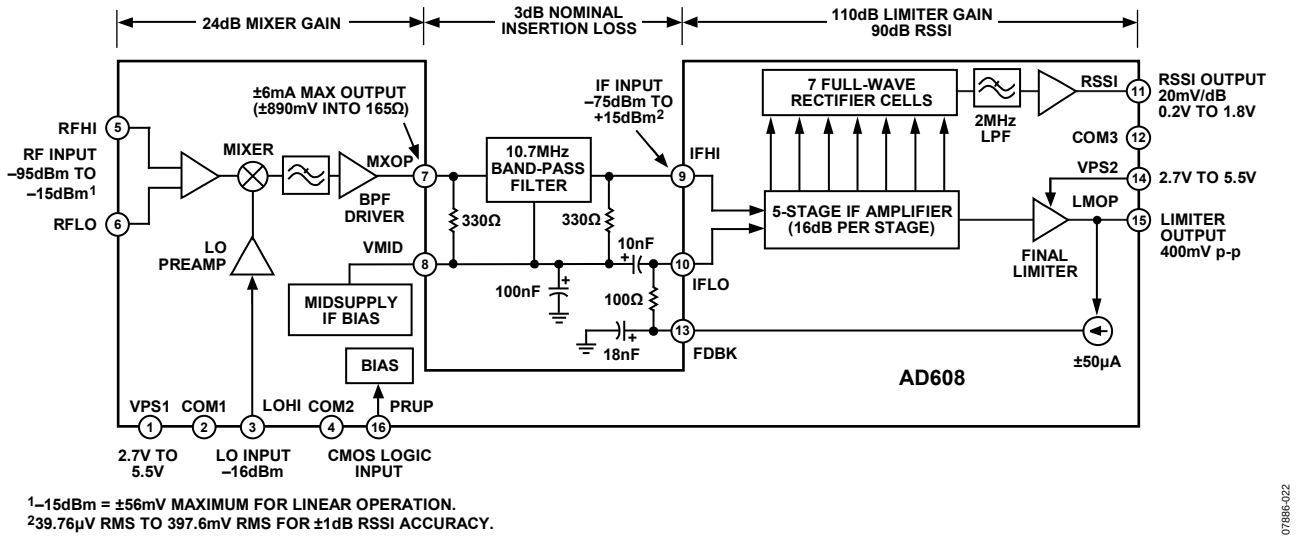


Figure 22. Functional Block Diagram

Table 5. Mixer Input Impedance vs. Frequency

Frequency (MHz)	Resistance (Ω)	Capacitance (pF)
45	2800	3.1
70	2600	3.1
100	1900	3.0
200	1200	3.1
300	760	3.2
400	520	3.4
500	330	3.6

IF FILTER TERMINATIONS

The AD608 was designed to drive a parallel-terminated 10.7 MHz band-pass filter (BPF) with a 330 Ω impedance. With a 330 Ω parallel-terminated filter, Pin MXOP sees a 165 Ω termination, and the gain is nominally 24 dB. Other filter impedances and gains can be accommodated by either accepting an increase or decrease in gain in proportion to the filter impedance or by keeping the impedance seen by MXOP at a nominal 165 Ω (by using resistive dividers or matching networks). Figure 23 shows a simple resistive voltage divider for matching an assortment of filter impedances, and Table 6 lists component values.

THE LOGARITHMIC IF AMPLIFIER

The logarithmic IF amplifier consists of five amplifier stages of 16 dB gain each, plus a final limiter. The IF bandwidth is 30 MHz (−1 dB), and the limiting gain is 110 dB. The phase skew is ±3° from −75 dBm to +5 dBm (approximately 111 μV p-p to 1.1 V p-p). The limiter output impedance is 200 Ω, and the limiter output drive is ± 200 mV (400 mV p-p) into a 5 kΩ load. In the absence of an input signal, the limiter output limits noise fluctuations, producing an output that continues to swing 400 mV p-p, but with random zero crossings.

OFFSET FEEDBACK LOOP

Because the logarithmic amplifier is dc-coupled and has more than 110 dB of gain from the input to the limiter output, a dc offset at its input of even a few microvolts causes the output to saturate. Therefore, the AD608 uses a low frequency feedback loop to null the input offset. Referring to Figure 23, the loop consists of a current source driven by the limiter, which sends 50 μA current pulses to Pin FDBK. The pulses are low-pass filtered by a π-network consisting of C1, R4, and C5. The smoothed dc voltage that results is subtracted from the input to the IF amplifier at Pin IFLO. Because this is a high gain amplifier with a feedback loop, care should be taken in layout and component values to prevent oscillation. Recommended values for the common IFs of 450 kHz, 455 kHz, 6.5 MHz, and 10.7 MHz are listed in Table 6.

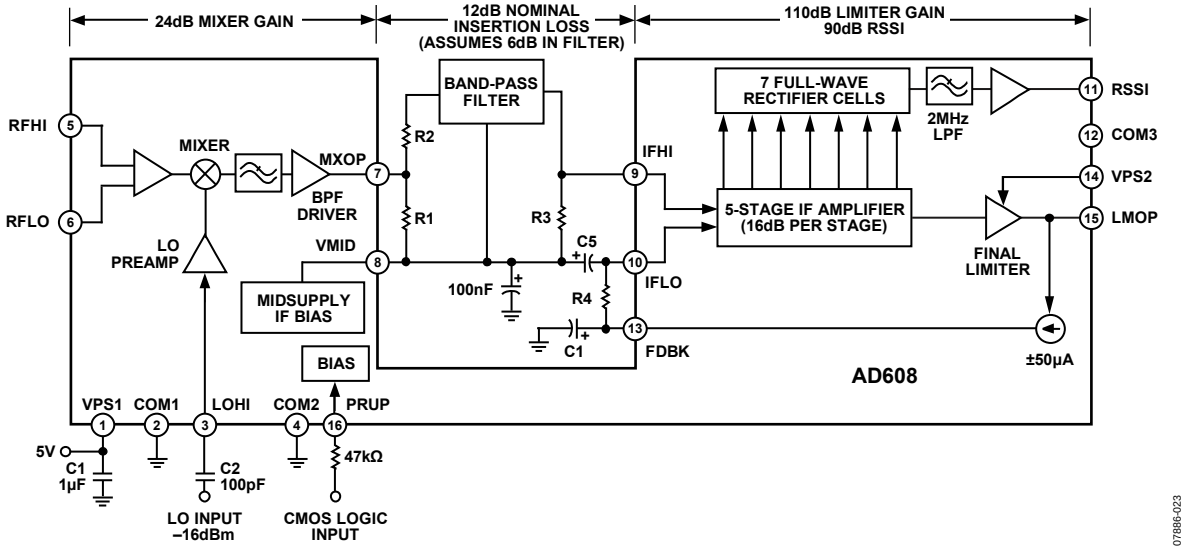


Figure 23. Applications Diagram for Common IFs and Filter Impedances

Table 6. AD608 Filter Termination and Offset-Null Feedback Loop Resistor and Capacitor Values for Common IFs

		Filter Termination Resistor Values[1] for 24 dB of Mixer Gain			Offset-Null Feedback Loop Values		
IF	Filter Impedance	R1	R2	R3	R4	C1	C5
450 kHz[2]	1500 Ω	174 Ω	1330 Ω	1500 Ω	1000 Ω	200 nF	100 nF
455 kHz	1500 Ω	174 Ω	1330 Ω	1500 Ω	1000 Ω	200 nF	100 nF
6.5 MHz	1000 Ω	178 Ω	825 Ω	1000 Ω	100 Ω	18 nF	10 nF
10.7 MHz	330 Ω	330 Ω	0 Ω	330 Ω	100 Ω	18 nF	10 nF

[1] Resistor values were calculated so that R1 + R2 = Z_{FILTER} and R1||(R2 + Z_{FILTER}) = 165 Ω.
[2] Operation at IFs of 450 kHz and 455 kHz requires use of an external low-pass filter with at least one pole at a cutoff frequency of 90 kHz (a decade below the ripple at 900 kHz).

RSSI OUTPUT

The logarithmic amplifier uses a successive-detection architecture. Each of the five stages has a full-wave detector; two additional high level detectors are driven by attenuators at the input to the limiting amplifiers, for a total of seven detector stages. Because each detector is a full-wave rectifier, the ripple component in the resulting dc is at twice the IF. The AD608 low-pass filter has a 2 MHz cutoff frequency, which is one decade below the 21.4 MHz ripple that results from a 10.7 MHz IF.

For operation at lower IFs, such as 450 kHz or 455 kHz, the AD608 requires an external low-pass filter with a single pole located at 90 kHz, a decade below the 900 kHz ripple frequency for these IFs. The RSSI range is from the noise level at approximately −80 dBm to overload at +15 dBm and is specified for ±1 dB accuracy from −75 dBm to +5 dBm. The +15 dBm maximum IF input is provided to accommodate band-pass filters of lower insertion loss than the nominal 4 dB for 10.7 MHz ceramic filters.

DIGITIZING THE RSSI

In typical cellular radio applications, the RSSI output of the AD608 is digitized by an analog-to-digital converter (ADC). The RSSI output of the AD608 is proportional to the power supply voltage, which not only allows the ADC to use the supply as a reference, but also causes the RSSI output and the ADC output to track over power supply variations, reducing system errors and component costs.

POWER CONSUMPTION

The total power supply current of the AD608 is a nominal 7.3 mA. The power is signal dependent, partly because the RSSI output increases (the current is increased by 200 µA at an RSSI output of +1.8 V), but mostly due to the IF consumption of the band-pass filter when driven to ±891 mV, assuming a 4 dB loss in this filter and a peak input of +5 dBm to the log-IF amp. In addition, the power is temperature dependent because the biasing system used in the AD608 is proportional to the absolute temperature (PTAT).

TROUBLESHOOTING

The most common causes of problems with the AD608 are incorrect component values for the offset feedback loop, poor board layout, and pickup of radio frequency interference (RFI), which all cause the AD608 to lose the low end (typically below −65 dBm) of its RSSI output and cause the limiter to swing randomly. Both poor board layout and incorrect component values in the offset feedback loop can cause low level oscillations. Pickup of RFI can be caused by improper layout and shielding of the circuit.

APPLICATIONS INFORMATION

Figure 24 shows the AD608 configured for operation in a digital system at a 10.7 MHz IF. The input and output impedance of the filter are parallel terminated using 330 Ω resistors, and the conversion gain is 24 dB. The RF port is terminated in 50 Ω; in a typical application, the input is matched to a SAW filter using the impedance data provided in Table 5.

Figure 25 shows the AD608 configured for narrow-band FM operation at a 450 kHz or 455 kHz with an external discriminator. The IF filter has 1500 Ω input and output impedances—the input is matched via a resistive divider, and the output is terminated in 1500 Ω. The discriminator requires a 1 V p-p drive from a 1 kΩ source impedance, which in Figure 25 is provided by a Class A amplifier with a gain of 2.5.

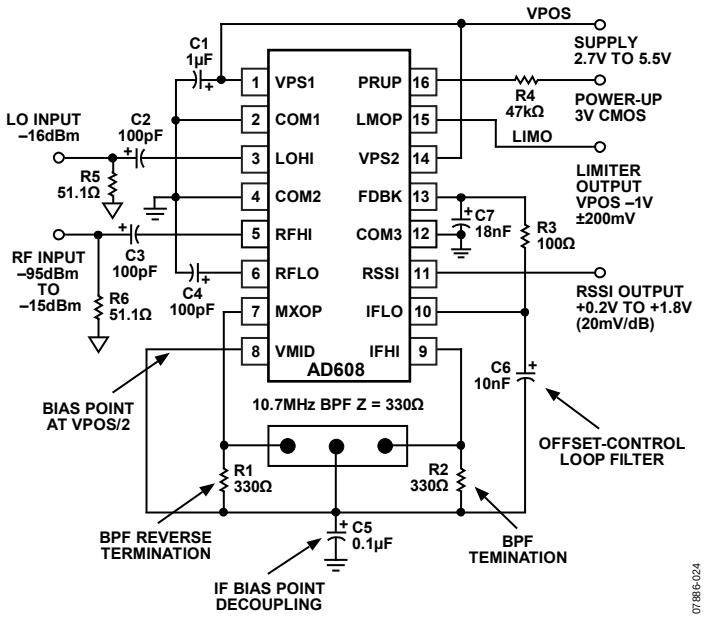


Figure 24. Application at 10.7 MHz (the Band-Pass Filter Can Be a Toko SK107 or Murata SFE10.7)

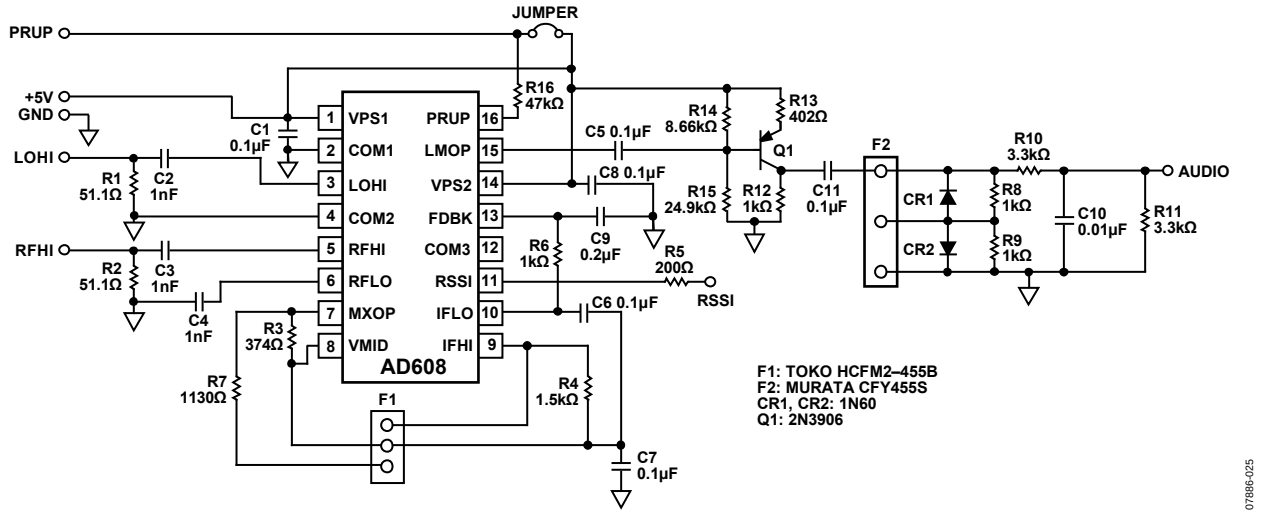
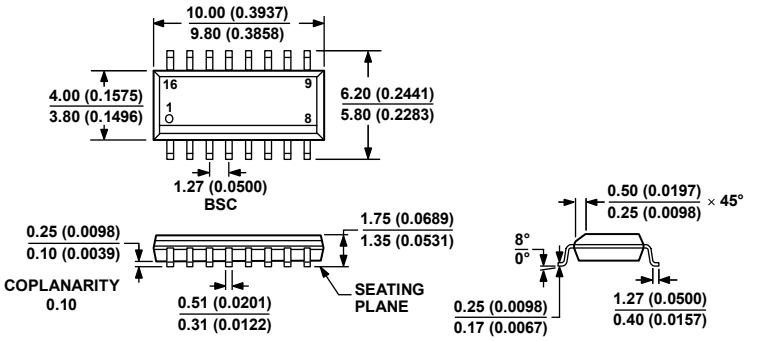


Figure 25. Narrow-Band FM Application at 450 kHz or 455 kHz

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 26. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD608AR	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
AD608AR-REEL	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
AD608ARZ[1]	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
AD608ARZ-RL[1]	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
EVAL-AD608EBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

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