DELIVERING HIGH-SPEED
CONNECTIVITY CAPABILITIES
ACROSS THE SERIAL SPECTRUM

CONNECTIVITY PLATFORMS FOR VIRTEX-6 / SPARTAN-6 FPGAS

Connectivity Design Challenges

- Scaling performance to meet changing requirements
- Building systems for smaller form factors and stringent power budgets, at lower costs
- Reducing design development time, accelerating market adoption

Xilinx Connectivity Platforms

- Support all popular serial protocols with Virtex®-6 FPGAs with built-in ultra-high speed >11Gb/s GTH transceivers and highly flexible 6.5Gb/s GTX transceivers
- Enable targeting smaller form factors with Spartan®-6 FPGAs with the low-power 3.125Gb/s GTP transceivers
- Address power considerations and enable low-cost solution deployment with built-in blocks for PCIe®, Ethernet, and Memory Controllers
- Accelerate development time with Targeted Reference Designs delivered with connectivity kits

Key Connectivity Challenges

Ever-increasing I/O bandwidth is needed to address higher silicon processing capabilities and to meet constantly changing market dynamics. Parallel to serial transition is almost complete and serial (≤ 3.125Gb/s) to higher speed serial (≥ 5Gb/s) is imminent. Designers must address lower power, lower system cost and shrink existing form-factors.

Xilinx Connectivity Platforms Simplify and Accelerate High-Speed Serial Deployment

The Connectivity Platforms enable efficient implementation and faster deployment of customer end-product systems across the serial spectrum. Key elements of these platforms are:

- FPGA silicon equipped development board with popular serial interfaces
- Tools and plug-and-play IP tailored for connectivity methodologies
- Targeted Reference Designs that integrate built-in blocks and soft IP both Xilinx and Alliance Partner IP
- Software interface to enable users to setup, evaluate settings and modify to understand different implementations

This complete and comprehensive approach accelerates development for experienced users and simplifies the adoption of FPGAs for new users.

Complete Tool Flow Reduces Time-to-Market

State-of-the-art serial connectivity tools are integrated in the ISE® Design Suite software to implement both established as well as new serial protocols. It also includes a comprehensive IP portfolio supporting industry leading serial protocols. In addition, Xilinx's scalable board strategy enabled by on-board FPGA Mezzanine Card (FMC) connectors empowers customers to focus on innovation by reusing the design elements of the targeted reference designs.

Target Market Applications

Xilinx Connectivity platforms accelerate a broad range of applications, including:

- Wired telecommunications and wireless infrastructure applications
- Audio, video, and broadcast solutions
- Industrial, automotive infotainment, and high-end consumer markets
- Aerospace and Defense (A&D) and high-performance computing
- Storage applications

XILINX®

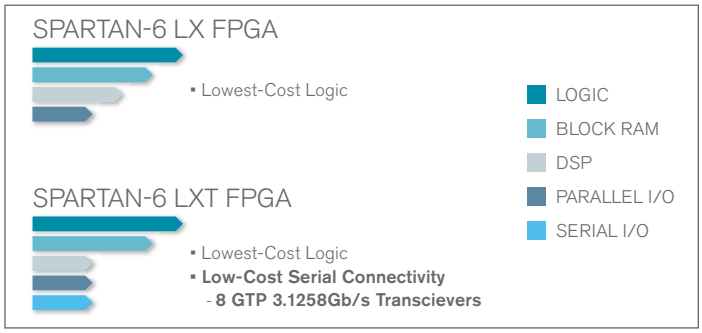
Silicon

High-Performance Connectivity Solutions for Virtex-6 FPGAs

- Virtex-6 LXT/SXT FPGAs serve applications that require high-performance logic, DSP, and serial connectivity, with up to 36 low-power GTX 6.5Gb/s serial transceivers
- Virtex-6 HXT FPGAs are optimized for communication, switching, and imaging systems that require the highest-speed serial connectivity, with up to 24 GTH 11.18Gb/s serial transceivers and 48 GTX 6.5Gb/s serial transceivers
- 1.4Gb/s SelectIO™ technology to build high-bandwidth parallel interfaces

Low-Cost, Easy-to-Use Connectivity Solutions for Spartan-6 FPGAs

- Spartan-6 LXT FPGAs are the first to provide the necessary logic capacity, performance, power consumption, and price points to enable mainstream designers to use FPGA-based serial technology with up to 8 GTP 3.125Gb/s transceivers
- 1.05Gb/s SelectIO technology to meet 3.3V to 1.2V parallel I/O standards and protocols along with hot swap compliance



Built-In Blocks and IP Portfolio

- Maximize scalability of Virtex-6 FPGAs supporting up to 4 PCIe blocks (x1-x8 Gen1/Gen2) Endpoint and Root port configuration, up to 4 Ethernet blocks supporting 10/100/1000Mb/s operation through multiple interfaces
- Simplified and optimized connectivity for Spartan-6 FPGAs using 1 PCIe block (x1 Gen1) Endpoint configuration and 4 Memory Interface controller blocks supporting DDR, DDR2, DDR3, and LP DDR interfaces
- Xilinx IP portfolio, available through the CORE Generator™ system enables design with multiple protocols, streamlines design process, and improves design quality
- Alliance Partner IP portfolio simplifies and maximizes design flexibility and reduces risk by supporting additional serial/parallel protocols and hardware acceleration functions

Support for Industry Standard AXI4™ Interface

The Xilinx Connectivity Targeted Design platforms now support the industry standard AXI interface for design creation and system integration. Users can now use a single interface specification that can be used to target the FPGA architectures to create high performance designs and simplify development & enhancement of these systems that include external memory and connectivity processing blocks.

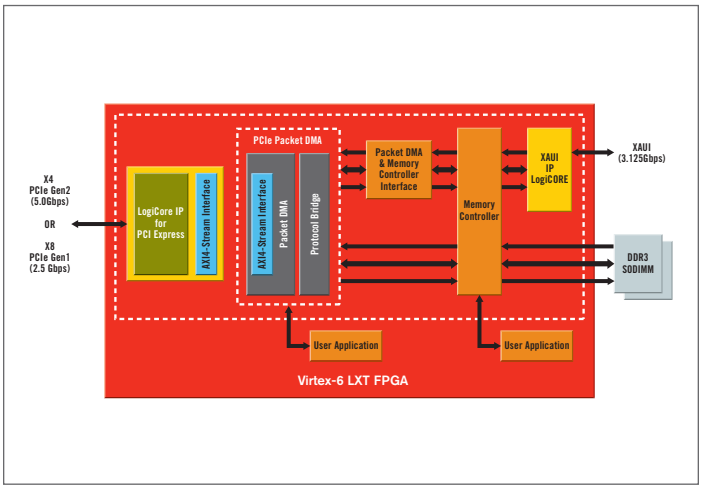
Tools and Design Flows Tailored for Connectivity Designs

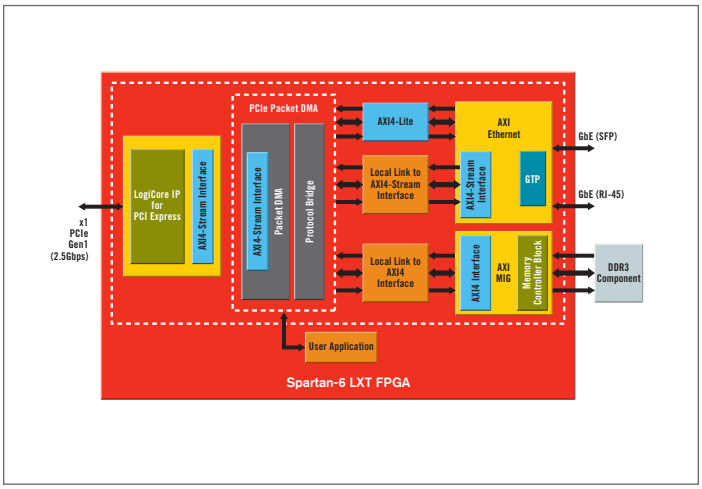
- Front-to-back design methodology with ISE Design Suite Logic/Embedded editions
- Architecture Wizards–Transceiver, Clocking, CRC Wizards
- Design analysis and synthesis–PlanAhead™ (floorplanning and PinLayout) and XST
- Implementation tool–MAP, Timing driven Place & Route (P&R), and SmartXplorer
- Debug tools–ChipScope™ Pro, SerialIO ToolKit, FPGA Editor
- Guidelines and reports:
  - Signal integrity considerations
  - Transceiver characterization: generic and protocol specific reports
  - PCB design guidelines

Targeted Reference Designs

Accelerate system design development by integrating critical components–transceivers, IP blocks, and memory controllers. The connectivity kit framework includes:

- Complete end-to-end system design enabling building block FPGA design architecture
- Design fully tested, validated, supported, maintained, and updated for every revision of the ISE software release
- Hardware Design Elements: RTL and IP files simulation environment, implementation scripts, and FPGA programming files
- Enabling System Design using the industry standard AXI4 Streaming, Memory Mapped, Lite Interfaces for interfacing different IP blocks
- Software Design Elements: source files including–device drivers, APIs, application, and GUI
- Demonstration and documentation: User Guides, Getting Started Guides, Hardware Setup Guides





Virtex-6 Connectivity Targeted Reference Design includes:

- GTX transceivers running at PCIe (5.0Gb/s) and XAUI (3.125Gb/s) line rates
- Xilinx IP LogiCORE for PCI Express Endpoint-x4 Gen2 or x8 Gen1
- Northwest Logic Packet DMA supporting >20G aggregate bandwidth
- Xilinx Virtual-FIFO memory controller design
- Xilinx IP LogiCORE for XAUI

Spartan-6 Connectivity Targeted Reference Design includes:

- GTP transceivers running at PCIe (2.5Gb/s) and GbE (1.25Gb/s) line rates
- Xilinx IP LogiCORE for PCI Express Endpoint–x1 Gen1
- Northwest Logic Packet DMA supporting >3G aggregate bandwidth
- Xilinx Virtual-FIFO memory controller design using built-in Memory Interface Controller Block
- Xilinx IP LogiCORE for Ethernet supporting GMII and SFP interfaces

CONNECTIVITY KIT DESIGN FLOW

1. GETTING STARTED

- Read the Getting Started Guide
- Connect the cables
- Power-up the board
- Load the reference designs
- Demo up and running

2. EVALUATE

- Evaluate reference design using interactive web-based user interface

3. CUSTOMIZE

- Open the design tools
- Customize the reference designs
- Generate a new design
- Download and run

Connectivity Kits

There are two Connectivity kits, each featuring either a Virtex-6 or Spartan-6 device. The kits are complete and easy-to-use right out of the box.

VIRTEX-6 FPGA CONNECTIVITY KIT

For more information, support, documents and reference designs, or to purchase, please visit **www.xilinx.com/v6connkit**

SPARTAN-6 FPGA CONNECTIVITY KIT

For more information, support, documents and reference designs, or to purchase, please visit **www.xilinx.com/s6connkit**

Each Virtex-6 FPGA Connectivity Kit for high-bandwidth and high-performance connectivity applications features:

- Xilinx ML605 Development Board including Virtex-6 LX240T FPGA
- FMC Connectivity Daughter Card (CX4, SMA, SATA interfaces)
- CX4 Loopback Module
- ISE Design Suite Embedded Edition (device-locked to Virtex-6 LX240T FPGA)
- Connectivity Targeted Reference Design: PCIe-10GDMA-DDR3-XAUI

Each Spartan-6 FPGA Connectivity Kit for easy-to-use connectivity applications features:

- Xilinx SP605 Development Board including Spartan-6 LX45T FPGA
- FULL seat of a Production Netlist of Northwest Logic x1 Packet DMA Back-end core (single seat node-locked license)
- ISE Design Suite Embedded Edition (device-locked to Spartan-6 LX45T FPGA)
- Connectivity Targeted Reference Design: PCIe-DMA-DDR3-GbE

Each kit also includes:

- Board design files
- Fedora 10 Live CD
- Cables and power supply
- Getting Started Demonstration
- Documentation: Hardware Setup Guide, Getting Started Guide, and User Guides
- Reference designs, demos, documentation, and applications delivered on USB memory stick to get started quickly

Take the NEXT STEP

Visit us online at **www.xilinx.com/connectivity**

Corporate Headquarters
Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
USA
Tel: 408-559-7778
www.xilinx.com

Europe
Xilinx Europe
One Logic Drive
Citywest Business Campus
Saggart, County Dublin
Ireland
Tel: +353-1-464-0311
www.xilinx.com

Japan
Xilinx K.K.
Art Village Osaki Central Tower 4F
1-2-2 Osaki, Shinagawa-ku
Tokyo 141-0032 Japan
Tel: +81-3-6744-7777
japan.xilinx.com

Asia Pacific
Xilinx, Asia Pacific Pte. Ltd.
5 Changi Business Park
Singapore 486040
Tel: +65-6407-3000
www.xilinx.com

Printed in the U.S.A. PN 2460