Freescale Semiconductor
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RoHS

An Energy-Efficient Solution from Freescale

MCF51JE256/128

MCF51JE256/128

The MCF51JE256 series devices are members of the low-cost, low-power, high-performance ColdFire® V1 family of 32-bit microcontrollers (MCUs).

Not all features are available in all devices or packages; see Table 2 for a comparison of features by device.


80-LQFP
12mm x 12mm


81-BGA
10mm x 10mm


100-LQFP
14mm x 14mm


104-BGA
10mm x 10mm

32-Bit ColdFire V1 Central Processor Unit (CPU)

- Up to 50.33-MHz ColdFire CPU above 2.4 V and 40 MHz CPU above 2.1 V and 20 MHz CPU above 1.8 V across temperature range of -40°C to 105°C.
- ColdFire Instruction Set Revision C (ISA_C).
- 32-bit multiply and accumulate (MAC) supports signed or unsigned integer or signed fractional inputs.

On-Chip Memory

- 256 K Flash comprised of two independent 128 K flash arrays; read/program/erase over full operating voltage and temperature; allows interrupt processing while programming.
- 32 Kbytes System Random-access memory (RAM).
- Security circuitry to prevent unauthorized access to RAM and Flash contents.

Power-Saving Modes

- Two ultra-low power stop modes. Peripheral clock enable register can disable clocks to unused modules to reduce currents.
- Time of Day (TOD) — Ultra low-power 1/4 sec counter with up to 64s timeout.
- Ultra-low power external oscillator that can be used in stop modes to provide accurate clock source to the TOD. 6 usec typical wake up time from stop3 mode.

Clock Source Options

- Oscillator (XOSC1) — Loop-control Pierce oscillator; 32.768 kHz crystal or ceramic resonator dedicated for TOD operation.
- Oscillator (XOSC2) for high frequency crystal input for MCG reference to be used for system clock and USB operations.
- Multipurpose Clock Generator (MCG) — PLL and FLL; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports CPU frequencies from 4 kHz to 50 MHz.

System Protection

- Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock.
- Low-voltage detection with reset or interrupt; selectable trip points; separate low voltage warning with optional interrupt; selectable trip points.
- Illegal opcode and illegal address detection with reset.
- Flash block protection for each array to prevent accidental write/erasure.
- Hardware CRC to support fast cyclic redundancy checks.

Development Support

- Integrated ColdFire DEBUG_Rev_B+ interface with single wire BDM connection supports same electrical interface used by the S08 family debug modules.
- Real-time debug with 6 hardware breakpoints (4 PC, 1 address and 1 data).
- On-chip trace buffer provides programmable start/stop recording conditions.

Peripherals

- USB — Dual-role USB On-The-Go (OTG) device, supports USB in either device, host or OTG configuration. On-chip transceiver and 3.3V regulator help save system cost, fully compliant with USB Specification 2.0. Allows control, bulk, interrupt and isochronous transfers.
- SCIx — Two serial communications interfaces with optional 13-bit break; option to connect Rx input to PRACMP output on SCI1 and SCI2; High current drive on Tx on SCI1 and SCI2; wake-up from stop3 on Rx edge.
- SPI1 — Serial peripheral interface with 64-bit FIFO buffer; 16-bit or 8-bit data transfers; full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting.
- SPI2 — Serial peripheral interface with full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting.
- IIC — Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 11-bit addressing.
- CMT — Carrier Modulator timer for remote control communications. Carrier generator, modulator and driver for dedicated infrared out (IRO). Can be used as an output compare timer.
- TPMx — Two 4-channel Timer/PWM Module; Selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel; external clock input/pulse accumulator.
- Mini-FlexBus — Multi-function external bus interface with user programmable chip selects and the option to multiplex address and data lines.
- PRACMP — Analog comparator with selectable interrupt; compare option to programmable internal reference voltage; operation in stop3.
- ADC12 — 12-bit Successive approximation ADC with 4 differential channels and up to12 single-ended channels; internal bandgap reference channel; operation in stop3; fully functional from 3.6V to 1.8V.
- PDB — Programmable delay block with 16-bit counter and modulus and prescale to set reference clock to bus divided by 1 to bus divided by 2048; 8 trigger outputs for ADC module provides periodic coordination of ADC sampling sequence with sequence completion interrupt; Back-to-Back mode and Timed mode.
- DAC — 12-bit resolution; 16-word data buffers with configurable watermark.

Input/Output

- Up to 68 GPIOs and 1 output-only pin.
- Voltage Reference output (VREFO).
- Dedicated infrared output pinwith high current sink capability.
- Up to 16 KBI pins with selectable polarity.
- Up to 16 pins of rapid general purpose I/O.

Energy Efficient Solutions optimized for low power

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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Preliminary — Subject to Change

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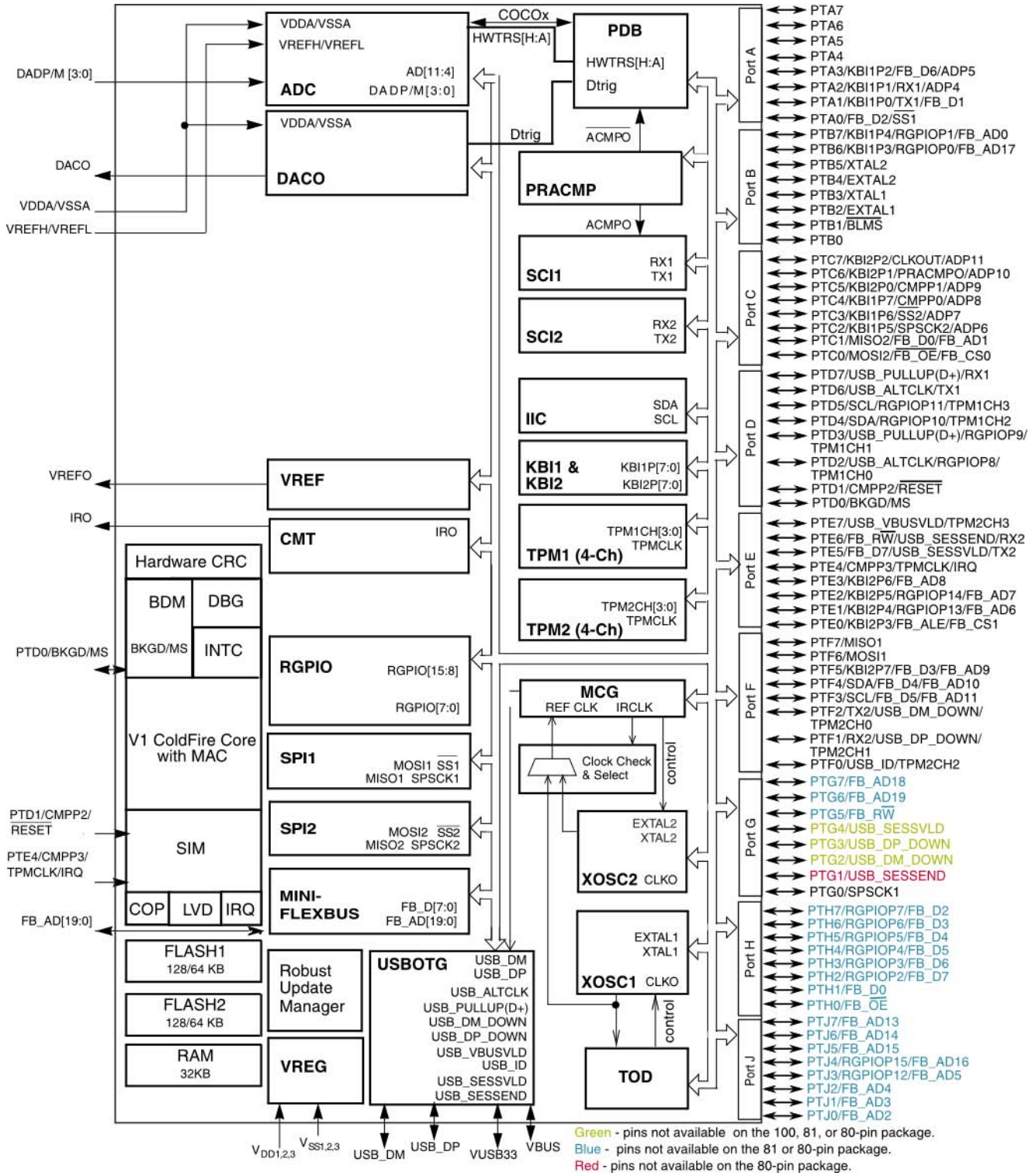


Figure 1. MCF51JE256/128 Block Diagram

1 Features

The following table provides a cross-comparison of the features of the MCF51JE256/128 according to package.

Table 1. MCF51JE256/128 Features by MCU and Package

Feature	MCF51JE256				MCF51JE128	
FLASH Size (bytes)	262144				131072	
RAM Size (bytes)	32K				32K	
Pin Quantity	104	100	81	80	81	80
Programmable Analog Comparator (PRACMP)	yes	yes	yes	yes	yes	yes
Debug Module (DBG)	yes	yes	yes	yes	yes	yes
Multipurpose Clock Generator (MCG)	yes	yes	yes	yes	yes	yes
Inter-Integrated Communication (IIC)	yes	yes	yes	yes	yes	yes
Interrupt Request Pin (IRQ)	yes	yes	yes	yes	yes	yes
Keyboard Interrupt (KBI)	16	16	16	16	16	16
Digital General Purpose I/O[1]	69	65	48	47	48	47
Power and Ground Pins	8	8	8	8	8	8
Time Of Day (TOD)	yes	yes	yes	yes	yes	yes
Serial Communications (SCI1)	yes	yes	yes	yes	yes	yes
Serial Communications (SCI2)	yes	yes	yes	yes	yes	yes
Serial Peripheral Interface (SPI1(FIFO))	yes	yes	yes	yes	yes	yes
Serial Peripheral Interface(SPI2)	yes	yes	yes	yes	yes	yes
Carrier Modulator Timer Pin (IRO)	yes	yes	yes	yes	yes	yes
TPM Input Clock Pin (TPMCLK)	yes	yes	yes	yes	yes	yes
TPM1 Channels	4	4	4	4	4	4
TPM2 Channels	4	4	4	4	4	4
XOSC1	yes	yes	yes	yes	yes	yes
XOSC2	yes	yes	yes	yes	yes	yes
USB On-the-Go	yes	yes	yes	yes	yes	yes
Mini-FlexBus	yes	yes	DATA	DATA	DATA	DATA
Rapid GPIO	16	16	9	9	9	9
Programmable Delay Block (PDB)	yes	yes	yes	yes	yes	yes
12-Bit SAR ADC Differential Channels[2]	4	4	4	4	4	4
12-Bit SAR ADC Single-Ended Channels	8	8	8	8	8	8
DAC Ouput Pin (DACO)	yes	yes	yes	yes	yes	yes
Voltage Reference Output Pin (VREFO)	yes	yes	yes	yes	yes	yes

1 Port I/O count does not include $\overline{\text{BLMS}}$, BKGD and IRQ. $\overline{\text{BLMS}}$ and BKGD are Output only, IRQ is input only.

2 Each differential channel is comprised of 2 pin inputs.

The following table describes the functional units of the MCF51JE256/128.

Table 2. MCF51JE256/128 Functional Units

Unit	Function
DAC (digital to analog converter)	Used to output voltage levels.
12-BIT SAR ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution. The ADC has up to 12 single-ended inputs.
PDB (Programmable Delay Block)	Precisely trigger the DAC FIFO buffer.
Mini-FlexBus	Provides expansion capability for off-chip memory and peripherals.
USB On-the-Go	Supports the USB On-the-Go dual-role controller.
CMT (Carrier Modulator Timer)	Infrared output used for the Remote Controller operation.
MCG (Multipurpose Clock Generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources.
BDM (Background Debug Module)	Provides single pin debugging interface (part of the V1 ColdFire core).
CF1 CORE (V1 ColdFire Core)	Executes programs and interrupt handlers.
PRACMP	Analog comparators for comparing external analog signals against each other, or a variety of reference levels.
COP (Computer Operating Properly)	Software Watchdog.
IRQ (Interrupt Request)	Single-pin high-priority interrupt (part of the V1 ColdFire core).
CRC (Cyclic Redundancy Check)	High-speed CRC calculation.
DBG (Debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire. core)
FLASH (Flash Memory)	Provides storage for program code, constants, and variables.
IIC (Inter-integrated Circuits)	Supports standard IIC communications protocol and SMBus.
INTC (Interrupt Controller)	Controls and prioritizes all device interrupts.
KBI1 & KBI2	Keyboard Interfaces 1 and 2.
LVD (Low-voltage Detect)	Provides an interrupt to theColdFire V1 CORE in the event that the supply voltage drops below a critical value. The LVD can also be programmed to reset the device upon a low voltage event.
VREF (Voltage Reference)	The Voltage Reference output is available for both on- and off-chip use.
RAM (Random-Access Memory)	Provides stack and variable storage.
RGPIO (Rapid General-purpose Input/output)	Allows for I/O port access at CPU clock speeds. RGPIO is used to implement GPIO functionality.
SCI1, SCI2 (Serial Communications Interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols.
SIM (system integration unit)	

Table 2. MCF51JE256/128 Functional Units (Continued)

Unit	Function
SPI1 (FIFO), SPI2 (Serial Peripheral Interfaces)	SPI1 and SPI2 provide standard master/slave capability. SPI contains a FIFO buffer in order to increase the throughput for this peripheral.
TPM1, TPM2 (Timer/PWM Module)	Timer/PWM module can be used for a variety of generic timer operations as well as pulse-width modulation.
VREG (Voltage Regulator)	Controls power management across the device.
XOSC1 and XOSC2 (Crystal Oscillators)	These devices incorporate redundant crystal oscillators. One is intended primarily for use by the TOD, and the other by the CPU and other peripherals.

2 Pinouts and Pin Assignments

2.1 104-Pin MAPBGA

The following figure shows the 104-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9	10	11	
A	PTF6	PTF7	USB_DP	USB_DM	VUSB33	PTF4	PTF3	FB_AD12	PTJ7	PTJ5	PTJ4	A
B	PTG0	PTA0	PTG3	VBUS	PTF5	PTJ6	PTH0	PTE5	PTF0	PTF1	PTF2	B
C	IRO	PTG4	PTA6	PTG2	PTG6	PTG5	PTG7	PTH1	PTE4	PTE6	PTE7	C
D	PTA5	PTA4	PTB1	VDD1		VDD2		VDD3	PTA1	PTE3	PTE2	D
E	VSSA	PTA7	PTB0						PTA2	PTJ3	PTE1	E
F	VREFL			PTG1				PTC7	PTJ2	PTJ0	PTJ1	F
G	DADP2								PTD5	PTD7	PTE0	G
H		DADM2	PTA3	VSS1		VSS2		VSS3	PTD4	PTD3	PTD2	H
J	DADP0	DADM0	PTH7	PTH6	PTH4	PTH3	PTH2	PTD6	PTC2	PTC0	PTC1	J
K		DADM3	DADP1	PTH5	PTB6	PTB7	PTC3	PTD1	PTC4	PTC5	PTC6	K
L	DADP3	DACO	DADM1	VREFO	VREFH	VDDA	PTB3	PTB2	PTD0	PTB5	PTB4	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 2. 104-Pin MAPBGA

2.2 100-Pin LQFP

The following figure shows the 100-pin LQFP pinout configuration.

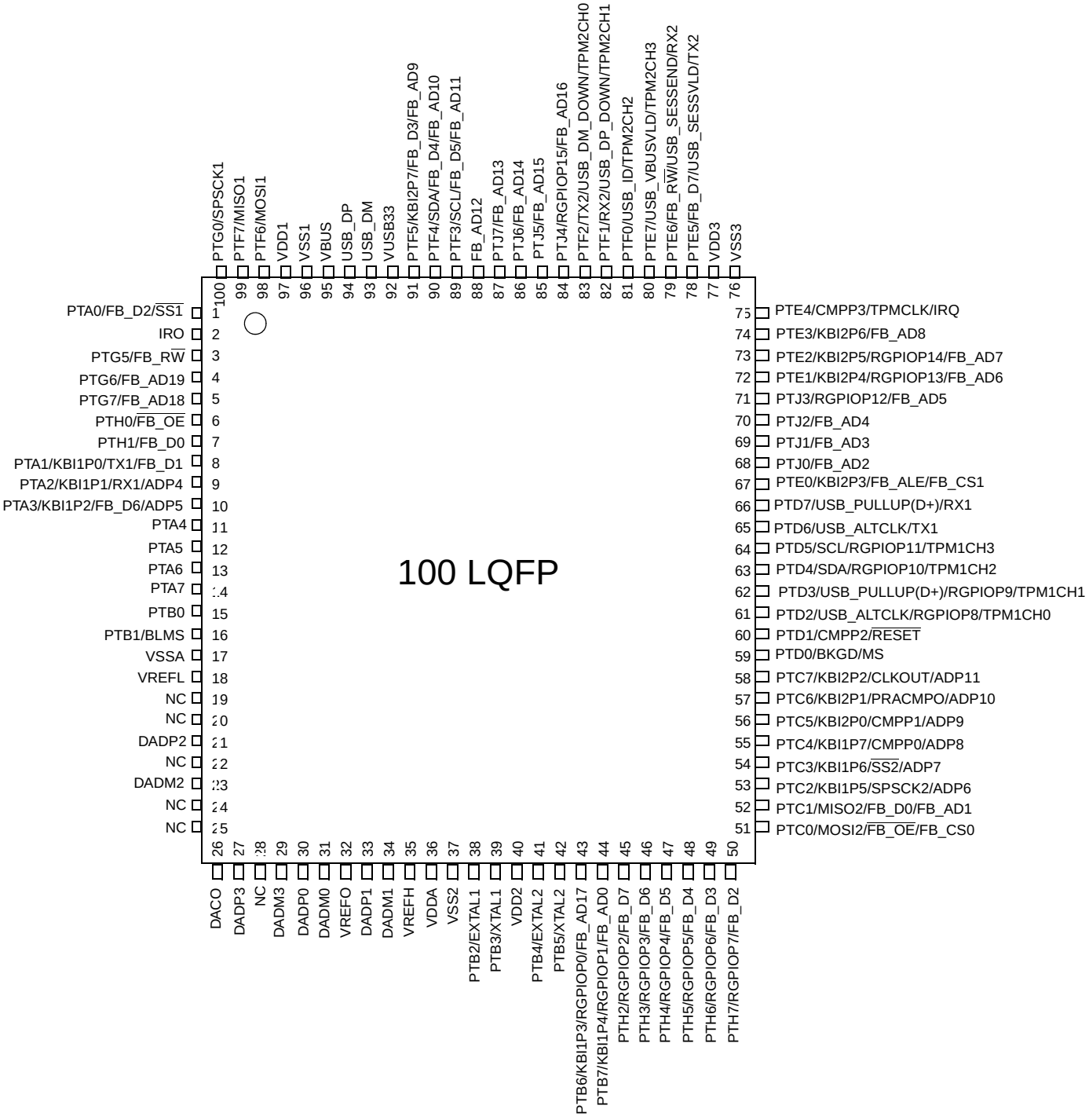


Figure 3. 100-Pin LQFP

2.3 81-Pin MAPBGA

The following figure shows the 81-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9	
A	IRO	PTG0	PTF6	USB_DP	VBUS	VUSB33	PTF4	PTF3	PTE4	A
B	PTF7	PTA0	PTG1	USB_DM	PTF5	PTE7	PTF1	PTF0	PTE3	B
C	PTA4	PTA5	PTA6	PTA1	PTF2	PTE6	PTE5	PTE2	PTE1	C
D		PTA7	PTB0	PTB1	PTA2	PTA3	PTD5	PTD7	PTE0	D
E		DADM2		VDD2	VDD3	VDD1	PTD2	PTD3	PTD6	E
F		DADP2		VSS2	VSS3	VSS1	PTB7	PTC7	PTD4	F
G	DADP0	DACO	DADP3	DADM3	VREFO	PTB6	PTC0	PTC1	PTC2	G
H	DADM0	DADM1	DADP1		PTC3	PTC4	PTD0	PTC5	PTC6	H
J	VSSA	VREFL	VREFH	VDDA	PTB2	PTB3	PTD1	PTB4	PTB5	J
	1	2	3	4	5	6	7	8	9	

Figure 4. 81-Pin MAPBGA

2.4 80-Pin LQFP

The following figure shows the 80-pin LQFP pinout configuration.

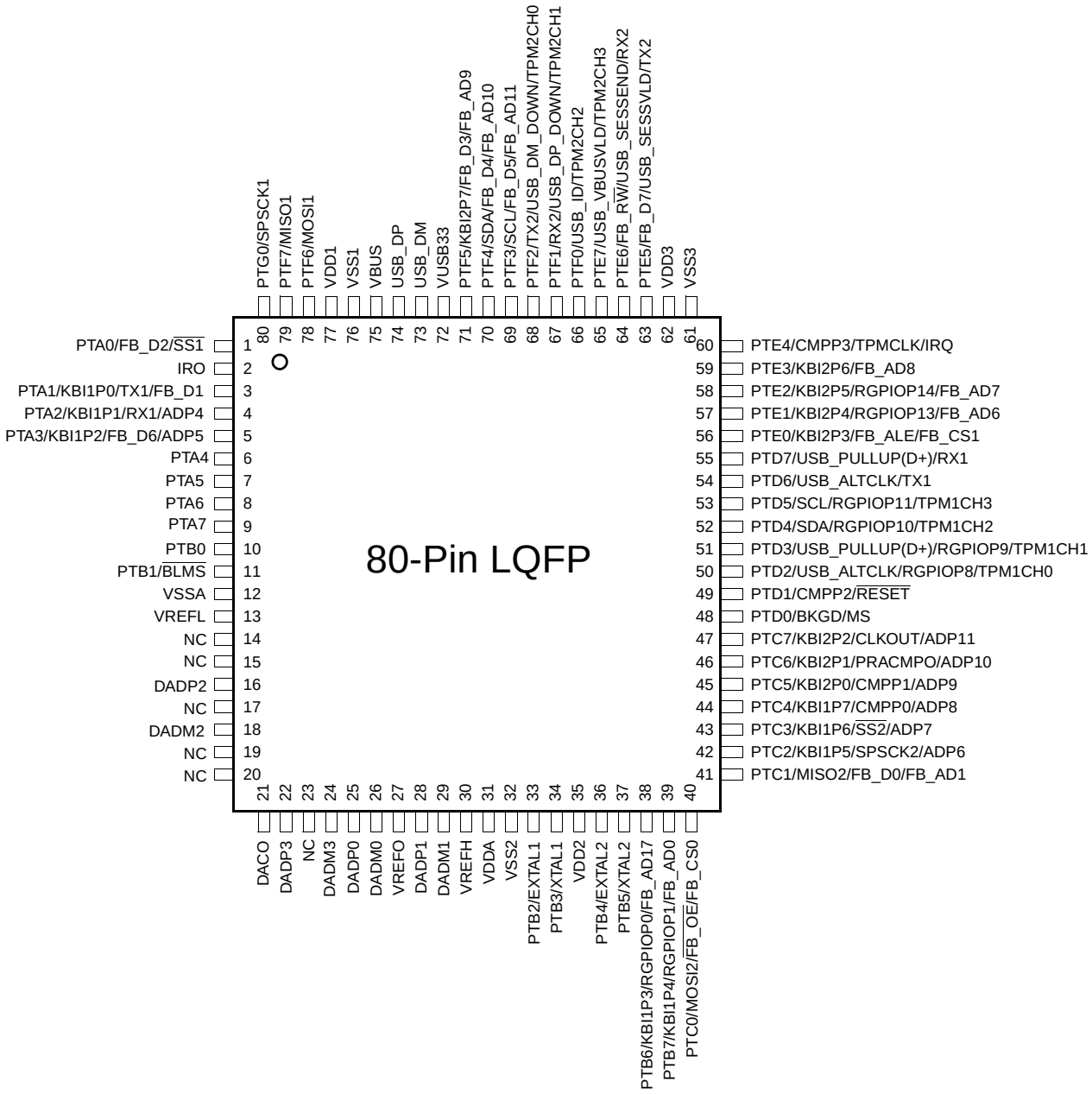


Figure 5. 80-Pin LQFP

2.5 Pin Assignments

Table 3. Package Pin Assignments

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
B2	1	B2	1	PTA0	FB_D2	$\overline{SS1}$	—	PTA0/FB_D2/$\overline{SS1}$
C1	2	A1	2	IRO	—	—	—	IRO
C6	3	—	—	PTG5	FB_$\overline{RW}$	—	—	PTG5/FB_$\overline{RW}$
C5	4	—	—	PTG6	FB_AD19	—	—	PTG6/FB_AD19
C7	5	—	—	PTG7	FB_AD18	—	—	PTG7/FB_AD18
B7	6	—	—	PTH0	$\overline{FB\_OE}$	—	—	PTH0/$\overline{FB\_OE}$
C8	7	—	—	PTH1	FB_D0	—	—	PTH1/FB_D0
D9	8	C4	3	PTA1	KBI1P0	TX1	FB_D1	PTA1/KBI1P0/TX1/FB_D1
E9	9	D5	4	PTA2	KBI1P1	RX1	ADP4	PTA2/KBI1P1/RX1/ADP4
H3	10	D6	5	PTA3	KBI1P2	FB_D6	ADP5	PTA3/KBI1P2/FB_D6/ADP5
D2	11	C1	6	PTA4	—	—	—	PTA4
D1	12	C2	7	PTA5	—	—	—	PTA5
C3	13	C3	8	PTA6	—	—	—	PTA6
E2	14	D2	9	PTA7	—	—	—	PTA7
E3	15	D3	10	PTB0	—	—	—	PTB0
D3	16	D4	11	PTB1	$\overline{BLMS}$	—	—	PTB1/$\overline{BLMS}$
E1	17	J1	12	VSSA	—	—	—	VSSA
F1	18	J2	13	VREFL	—	—	—	VREFL
F2	19	D1	14	—	—	—	—	NC
G2	20	E1	15	—	—	—	—	NC
G1	21	F2	16	DADP2		—	—	DADP2
H1	22	F1	17	—	—	—	—	NC
H2	23	E2	18	DADM2		—	—	DADM2
F3	24	F3	19	—	—	—	—	NC
G3	25	E3	20	—	—	—	—	NC
L2	26	G2	21	DACO	—	—	—	DACO
L1	27	G3	22	DADP3		—	—	DADP3
K1	28	H4	23	—	—	—	—	NC
K2	29	G4	24	DADM3		—	—	DADM3

Table 3. Package Pin Assignments

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
J1	30	G1	25	DADP0	—	—	—	DADP0
J2	31	H1	26	DADM0	—	—	—	DADM0
L4	32	G5	27	VREFO	—	—	—	VREFO
K3	33	H3	28	DADP1	—	—	—	DADP1
L3	34	H2	29	DADM1	—	—	—	DADM1
L5	35	J3	30	VREFH	—	—	—	VREFH
L6	36	J4	31	VDDA	—	—	—	VDDA
H6	37	F4	32	VSS2	—	—	—	VSS2
L8	38	J5	33	PTB2	EXTAL1	—	—	PTB2/EXTAL1
L7	39	J6	34	PTB3	XTAL1	—	—	PTB3/XTAL1
D6	40	E4	35	VDD2	—	—	—	VDD2
L11	41	J8	36	PTB4	EXTAL2	—	—	PTB4/EXTAL2
L10	42	J9	37	PTB5	XTAL2	—	—	PTB5/XTAL2
K5	43	G6	38	PTB6	KBI1P3	RGPIOP0	FB_AD17	PTB6/KBI1P3/RGPIOP0/FB_AD17
K6	44	F7	39	PTB7	KBI1P4	RGPIOP1	FB_AD0	PTB7/KBI1P4/RGPIOP1/FB_AD0
J7	45	—	—	PTH2	RGPIOP2	FB_D7	—	PTH2/RGPIOP2/FB_D7
J6	46	—	—	PTH3	RGPIOP3	FB_D6	—	PTH3/RGPIOP3/FB_D6
J5	47	—	—	PTH4	RGPIOP4	FB_D5	—	PTH4/RGPIOP4/FB_D5
K4	48	—	—	PTH5	RGPIOP5	FB_D4	—	PTH5/RGPIOP5/FB_D4
J4	49	—	—	PTH6	RGPIOP6	FB_D3	—	PTH6/RGPIOP6/FB_D3
J3	50	—	—	PTH7	RGPIOP7	FB_D2	—	PTH7/RGPIOP7/FB_D2
J10	51	G7	40	PTC0	MOSI2	$\overline{\text{FB\_OE}}$	FB_CS0	PTC0/MOSI2/$\overline{\text{FB\_OE}}$/FB_CS0
J11	52	G8	41	PTC1	MISO2	FB_D0	FB_AD1	PTC1/MISO2/FB_D0/FB_AD1
J9	53	G9	42	PTC2	KBI1P5	SPSCK2	ADP6	PTC2/KBI1P5/SPSCK2/ADP6
K7	54	H5	43	PTC3	KBI1P6	$\overline{\text{SS2}}$	ADP7	PTC3/KBI1P6/$\overline{\text{SS2}}$/ADP7
K9	55	H6	44	PTC4	KBI1P7	CMPP0	ADP8	PTC4/KBI1P7/CMPP0/ADP8
K10	56	H8	45	PTC5	KBI2P0	CMPP1	ADP9	PTC5/KBI2P0/CMPP1/ADP9
K11	57	H9	46	PTC6	KBI2P1	PRACMPO	ADP10	PTC6/KBI2P1/PRACMPO/ADP10
F8	58	F8	47	PTC7	KBI2P2	CLKOUT	ADP11	PTC7/KBI2P2/CLKOUT/ADP11
L9	59	H7	48	PTD0	BKGD	MS	—	PTD0/BKGD/MS
K8	60	J7	49	PTD1	CMPP2	$\overline{\text{RESET}}$	—	PTD1/CMPP2/$\overline{\text{RESET}}$

Table 3. Package Pin Assignments

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
H11	61	E7	50	PTD2	USB_ALTCLK	RGPIOP8	TPM1CH0	PTD2/USB_ALTCLK/RGPIOP8/TPM1CH0
H10	62	E8	51	PTD3	USB_PULLUP (D+)	RGPIOP9	TPM1CH1	PTD3/USB_PULLUP(D+)/RGPIOP9/TPM1CH1
H9	63	F9	52	PTD4	SDA	RGPIOP10	TPM1CH2	PTD4/SDA/RGPIOP10/TPM1CH2
G9	64	D7	53	PTD5	SCL	RGPIOP11	TPM1CH3	PTD5/SCL/RGPIOP11/TPM1CH3
J8	65	E9	54	PTD6	USB_ALTCLK	TX1	—	PTD6/USB_ALTCLK/TX1
G10	66	D8	55	PTD7	USB_PULLUP (D+)	RX1	—	PTD7/USB_PULLUP(D+) /RX1
G11	67	D9	56	PTE0	KBI2P3	FB_ALE	FB_CS1	PTE0/KBI2P3/FB_ALE/FB_CS1
F10	68	—	—	PTJ0	FB_AD2	—	—	PTJ0/FB_AD2
F11	69	—	—	PTJ1	FB_AD3	—	—	PTJ1/FB_AD3
F9	70	—	—	PTJ2	FB_AD4	—	—	PTJ2/FB_AD4
E10	71	—	—	PTJ3	RGPIOP12	FB_AD5	—	PTJ3/RGPIOP12/FB_AD5
E11	72	C9	57	PTE1	KBI2P4	RGPIOP13	FB_AD6	PTE1/KBI2P4/RGPIOP13/FB_AD6
D11	73	C8	58	PTE2	KBI2P5	RGPIOP14	FB_AD7	PTE2/KBI2P5/RGPIOP14/FB_AD7
D10	74	B9	59	PTE3	KBI2P6	FB_AD8	—	PTE3/KBI2P6/FB_AD8
C9	75	A9	60	PTE4	CMPP3	TPMCLK	IRQ	PTE4/CMPP3/TPMCLK/IRQ
H8	76	F5	61	VSS3	—	—	—	VSS3
D8	77	E5	62	VDD3	—	—	—	VDD3
B8	78	C7	63	PTE5	FB_D7	USB_ SESSVLD	TX2	PTE5/FB_D7/USB_SESSVLD/TX2
C10	79	C6	64	PTE6	FB_R$\overline{W}$	USB_ SESSEND	RX2	PTE6/FB_R$\overline{W}$/USB_SESSEND/RX2
C11	80	B6	65	PTE7	USB_ VBUSVLD	TPM2CH3	—	PTE7/USB_VBUSVLD/TPM2CH3
B9	81	B8	66	PTF0	USB_ID	TPM2CH2	—	PTF0/USB_ID/TPM2CH2
B10	82	B7	67	PTF1	RX2	USB_DP_D OWN	TPM2CH1	PTF1/RX2/USB_DP_DOWN/TPM2CH1
B11	83	C5	68	PTF2	TX2	USB_DM_ DOWN	TPM2CH0	PTF2/TX2/USB_DM_DOWN/TPM2CH0
A11	84	—	—	PTJ4	RGPIOP15	FB_AD16	—	PTJ4/RGPIOP15/FB_AD16
A10	85	—	—	PTJ5	FB_AD15	—	—	PTJ5/FB_AD15
B6	86	—	—	PTJ6	FB_AD14	—	—	PTJ6/FB_AD14
A9	87	—	—	PTJ7	FB_AD13	—	—	PTJ7/FB_AD13

Table 3. Package Pin Assignments

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
A8	88	—	—	FB_AD12	—	—	—	FB_AD12
A7	89	A8	69	PTF3	SCL	FB_D5	FB_AD11	PTF3/SCL/FB_D5/FB_AD11
A6	90	A7	70	PTF4	SDA	FB_D4	FB_AD10	PTF4/SDA/FB_D4/FB_AD10
B5	91	B5	71	PTF5	KBI2P7	FB_D3	FB_AD9	PTF5/KBI2P7/FB_D3/FB_AD9
A5	92	A6	72	VUSB33	—	—	—	VUSB33
A4	93	B4	73	USB_DM	—	—	—	USB_DM
A3	94	A4	74	USB_DP	—	—	—	USB_DP
B4	95	A5	75	VBUS	—	—	—	VBUS
H4	96	F6	76	VSS1	—	—	—	VSS1
D4	97	E6	77	VDD1	—	—	—	VDD1
A1	98	A3	78	PTF6	MOSI1	—	—	PTF6/MOSI1
A2	99	B1	79	PTF7	MISO1	—	—	PTF7/MISO1
B1	100	A2	80	PTG0	SPSCK1	—	—	PTG0/SPSCK1
F4	—	A1	—	PTG1	USB_ SESSEND	—	—	PTG1/USB_SESSEND
C4	—	—	—	PTG2	USB_DM_ DOWN	—	—	PTG2/USB_DM_DOWN
B3	—	—	—	PTG3	USB_DP_ DOWN	—	—	PTG3/USB_DP_DOWN
C2	—	—	—	PTG4	USB_SESSVLD	—	—	PTG4/USB_SESSVLD

3 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51JE256/128 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

3.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 4. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

Table 5. Absolute Maximum Ratings

#	Rating	Symbol	Value	Unit
1	Supply voltage	V_{DD}	–0.3 to + 3.8	V
2	Maximum current into V_{DD}	I_{DD}	120	mA
3	Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
4	Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
5	Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{In} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 6. Thermal Characteristics

#	Symbol	Rating	Value	Unit
1	T_A	Operating temperature range (packaged):		°C
		MCF51JE256	–40 to 105	
		MCF51JE128	–40 to 105	
2	T_{JMAX}	Maximum junction temperature	135	°C
3	θ_{JA}	Thermal resistance[1,2,3,4] Single-layer board — 1s		°C/W
		104-pin MBGA	67	
		100-pin LQFP	53	
		81-pin MBGA	67	
		80-pin LQFP	53	
4	θ_{JA}	Thermal resistance[1, 2, 3, 4] Four-layer board — 2s2p		°C/W
		104-pin MBGA	39	
		100-pin LQFP	41	
		81-pin MBGA	39	
		80-pin LQFP	39	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2 Junction to Ambient Natural Convection
3 1s — Single layer board, one signal layer
4 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.4 ESD Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 8. ESD and Latch-Up Protection Characteristics

#	Rating	Symbol	Min	Max	Unit	C
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V	T
2	Machine Model (MM)	V_{MM}	±200	—	V	T
3	Charge Device Model (CDM)	V_{CDM}	±500	—	V	T
4	Latch-up Current at T_A = 125°C	I_{LAT}	±100	—	mA	T

3.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 9. DC Characteristics

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
1	—	Operating Voltage	—	1.8[2]	—	3.6	V	—
2	V_{OH}	Output high voltage	All I/O pins, low-drive strength					
			1.8 V, I_{Load} = –600 µA	V_{DD} – 0.5	—	—	V	C
			All I/O pins, high-drive strength					
			2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	V	P
			2.3 V, I_{Load} = –6 mA	V_{DD} – 0.5	—	—	V	T
			1.8V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	V	C
3	I_{OHT}	Output high current	Max total I_{OH} for all ports					
			—	—	—	100	mA	D
4	V_{OL}	Output low voltage	All I/O pins, low-drive strength					
			1.8 V, I_{Load} = 600 µA	—	—	0.5	V	C
			All I/O pins, high-drive strength					
			2.7 V, I_{Load} = 10 mA	—	—	0.5	V	P
			2.3 V, I_{Load} = 6 mA	—	—	0.5	V	T
			1.8 V, I_{Load} = 3 mA	—	—	0.5	V	C
5	I_{OLT}	Output low current	Max total I_{OL} for all ports	—	—	—	100	mA	D

Table 9. DC Characteristics (Continued)

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
6	V_{IH}	Input high voltage all digital inputs						
			V_{DD} > 2.7 V	0.70 x V_{DD}	—	—	V	P
			V_{DD} > 1.8 V	0.85 x V_{DD}	—	—	V	C
7	V_{IL}	Input low voltage all digital inputs						
			V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	V	P
			V_{DD} >1.8 V	—	—	0.30 x V_{DD}	V	C
8	V_{hys}	Input hysteresis all digital inputs	—	0.06 x V_{DD}	—	—	mV	C
9	$\|I_{In}\|$	Input leakage current all input only pins (Per pin)	V_{In} = V_{DD} or V_{SS}	—	—	0.25 (TBD)	µA	P
10	$\|I_{OZ}\|$	Hi-Z (off-state) leakage current all input/output (per pin)	V_{In} = V_{DD} or V_{SS}	—	—	0.25	µA	P
11	$\|I_{OZ}\|$	Leakage current for analog output pins (DACO, VREFO) all input/output (per pin)	V_{In} = V_{DD} or V_{SS}	—	—	0.5	µA	P
12	R_{PU}	Pull-up resistors all digital inputs, when enabled	—	17.5	—	52.5	kΩ	P
13	R_{PD}	Internal pull-down resistors[3]	—	17.5	—	52.5	kΩ	P
14	I_{IC}	DC injection current [4, 5, 6] Single pin limit						
			V_{SS} > V_{IN} > V_{DD}	–0.2	—	0.2	mA	D
		Total MCU limit, includes sum of all stressed pins						
			V_{SS} > V_{IN} > V_{DD}	–5	—	5	mA	D
15	C_{In}	Input Capacitance, all pins	—	—	—	8	pF	C
16	V_{RAM}	RAM retention voltage	—	—	0.6	1.0	V	C
17	V_{POR}	POR re-arm voltage[7]	—	0.9	1.4	1.79	V	C
18	t_{POR}	POR re-arm time	—	10	—	—	µs	D

Table 9. DC Characteristics (Continued)

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
19	V_{LVDH}[8]	Low-voltage detection threshold — high range	V_{DD} falling					
			—	2.11	2.16	2.22	V	P
			V_{DD} rising					
			—	2.16	2.21	2.27	V	P
20	V_{LVDL}	Low-voltage detection threshold — low range[8]	V_{DD} falling					
			—	1.80	1.82	1.91	V	P
			V_{DD} rising					
			—	1.86	1.90	1.99	V	P
21	V_{LVWH}	Low-voltage warning threshold — high range[8]	V_{DD} falling					
			—	2.36	2.46	2.56	V	P
			V_{DD} rising					
			—	2.36	2.46	2.56	V	P
22	V_{LVWL}	Low-voltage warning threshold — low range[8]	V_{DD} falling					
			—	2.11	2.16	2.22	V	P
			V_{DD} rising					
			—	2.16	2.21	2.27	V	P
23	V_{hys}	Low-voltage inhibit reset/recoverhysteresis[9]	—	—	50	—	mV	C
24	V_{BG}	Bandgap Voltage Reference[10]	—	1.145	1.17	1.195	V	P

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 Measured with $V_{In} = V_{DD}$.

4 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

5 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

6 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

7 Maximum is highest voltage that POR is guaranteed.

[8] Run at 1 MHz bus frequency
[9] Low voltage detection and warning limits measured at 1 MHz bus frequency.
[10] Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

3.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
1	RI_{DD}	Run supply current FEI mode All modules ON							
			25.165 MHz	3	43	48	mA	–40 to 25	P
			25.165 MHz	3	43	48	mA	105	P
			20 MHz	3	31.6	—	mA	–40 to 105	T
			8 MHz	3	15.4	—	mA	–40 to 105	T
			1 MHz	3	2.9	—	mA	–40 to 105	T
2	RI_{DD}	Run supply current FEI mode; All modules OFF							
			25.165 MHz	3	28.1	29.6	mA	–40 to 105	C
			20 MHz	3	23.2	—	mA	–40 to 105	T
			8 MHz	3	12.3	—	mA	–40 to 105	T
			1 MHz	3	2.4	—	mA	–40 to 105	T
3	RI_{DD}	Run supply current LPS=0; All modules OFF							
			16 kHz FBILP	3	TBD	—	µA	–40 to 105	T
			16 kHz FBELP	3	TBD	—	µA	–40 to 105	T
4	RI_{DD}	Run supply current LPS=1, all modules OFF							
			16 kHz FBELP	3	TBD	—	µA	0 to 70	T
			16 kHz FBELP	3	TBD	—	µA	–40 to 105	T

Table 10. Supply Current Characteristics (Continued)

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
5	WI_{DD}	Wait mode supply current — FEI mode, all modules OFF							
			25.165 MHz	3	5	—	mA	–40 to 105	C
			20 MHz	3	TBD	—	mA	–40 to 105	T
			8 MHz	3	TBD	—	mA	–40 to 105	T
			1 MHz	3	TBD	—	mA	–40 to 105	T
6	$S2I_{DD}$	Stop2 mode supply current							
			N/A	3	0.410	0.640	µA	–40 to 25	P
			N/A	3	3.5	10	µA	70	C
			N/A	3	10	20	µA	85	C
			N/A	3	21	31.5	µA	105	P
			N/A	2	0.410	0.640	µA	–40 to 25	C
			N/A	2	3.4	9	µA	70	C
			N/A	2	9.5	18	µA	85	C
			N/A	2	20	30	µA	105	C
7	$S3I_{DD}$	Stop3 mode supply current — No clocks active							
			N/A	3	0.650	1.2	µA	–40 to 25	P
			N/A	3	7.1	18	µA	70	C
			N/A	3	20	28	µA	85	C
			N/A	3	37	63	µA	105	P
			N/A	2	0.400	0.900	µA	–40 to 25	C
			N/A	2	7.1	16	µA	70	C
			N/A	2	18	26	µA	85	C
			N/A	2	33	59	µA	105	C

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

Table 11. Typical Stop Mode Adders

#	Parameter	Condition	Temperature (°C)					Units	C
			-40	25	70	85	105		
1	LPO	—	50	75	100	150	250	nA	D
2	EREFSTEN	RANGE = HGO = 0	600 (TBD)	650 (TBD)	750 (TBD)	850 (TBD)	1000 (TBD)	nA	D
3	IREFSTEN[1]	—	68	70	77	86	120	µA	T
4	TOD	Does not include clock source current	50	75	100	150	250	nA	D
5	LVD[1]	LVDSE = 1	114	115	123	135	170	µA	T
6	ACMP[1]	Not using the bandgap (BGBE = 0)	18	20	23	33	65	µA	T
7	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	75	85	100	115	165	µA	T
8	DAC[1]	High power mode; no load on DACO	500	500	500	500	500	µA	T

1 Not available in stop2 mode.

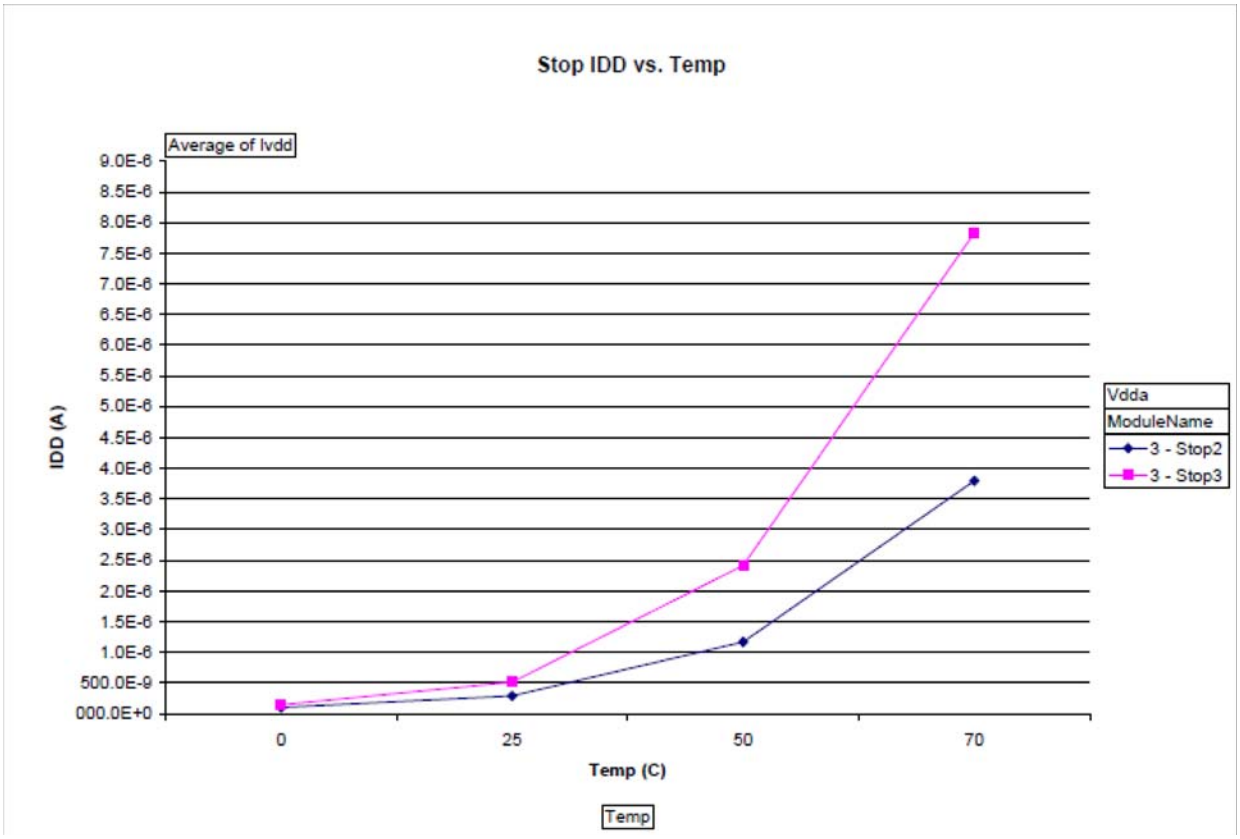


Figure 6. Stop IDD versus Temperature

3.7 PRACMP Electricals

Table 12. PRACMP Electrical Specifications

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage	V_{PWR}	1.8	—	3.6	V	P
2	Supply current (active) (PRG enabled)	I_{DDACT1}	—	—	60	µA	C
3	Supply current (active) (PRG disabled)	I_{DDACT2}	—	—	40	µA	C
4	Supply current (ACMP and PRG all disabled)	I_{DDDIS}	—	—	2	nA	D
5	Analog input voltage	VAIN	V_{SS} – 0.3	—	V_{DD}	V	—
6	Analog input offset voltage	VAIO	—	5	40	mV	T
7	Analog comparator hysteresis	V_H	3.0	—	20.0	mV	T
8	Analog input leakage current	I_{ALKG}	—	—	1	nA	D
9	Analog comparator initialization delay	tAINIT	—	—	1.0	µs	T

Table 12. PRACMP Electrical Specifications

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
10	Programmable reference generator inputs	$V_{In2}(V_{DD25})$	1.8	—	2.75	V	—
11	Programmable reference generator setup delay	t_{PRGST}	—	1	—	µs	D
12	Programmable reference generator step size	Vstep	–0.25	1	0.25	LSB	D
13	Programmable reference generator voltage range	Vprgout	$V_{In}/32$	—	V_{in}	V	P

3.8 12-bit DAC Electricals

Table 13. DAC 12LV Operating Requirements

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Supply voltage	V_{DDA}	1.8	3.6	V	P	
2	Reference voltage	V_{DACR}	1.15	3.6	V	C	
3	Temperature	T_A	–40	105	°C	C	
4	Output load capacitance	C_L	—	100	pF	C	A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.
5	Output load current	I_L	—	1	mA	C	

Table 14. DAC 12-Bit Operating Behaviors

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Resolution	N	12	12	bit	C	
2	Supply current low-power mode	I_{DDA_DACLP}	50	100	µA	C	
3	Supply current high-power mode	I_{DDA_DACHP}	120	500 (TBD)	µA	C	
4	Full-scale Settling time (±0.5 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) low-power mode	$Ts_{FS}LP$	—	200 (TBD)	µs	C	
5	Full-scale Settling time (±0.5 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) high-power mode	$Ts_{FS}HP$	—	30	µs	C	
6	Code-to-code Settling time (±0.5 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) low-power mode	$Ts_{C-C}LP$	—	5	µs	C	
7	Code-to-code Settling time (±0.5 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) high-power mode	$Ts_{C-C}HP$	—	1(TBD)	µs	C	
8	DAC output voltage range low (high-power mode, no load, DAC set to 0)	$V_{dacoutl}$	—	100 (TBD)	mV	C	
9	DAC output voltage range high (high-power mode, no load, DAC set to 0x0FFF)	$V_{dacouth}$	V_{DACR}-100	—	mV	C	
10	Integral non-linearity error	INL	—	± 8	LSB	C	
11	Differential non-linearity error VDACR is > 2.4 V	DNL	—	± 1	LSB	C	
12	Offset error	E_O	—	± 0.5	%FSR	C	
13	Gain error	E_G	—	± 0.5 (TBD)	%FSR	C	
14	Power supply rejection ratio $V_{DD} \geq 2.4$ V	PSRR	60	—	dB	C	
15	Temperature drift of offset voltage (DAC set to 0x0800)	T_{co}	—	2 (TBD)	mV	C	See Typical Drift figure that follows.
16	Offset aging coefficient	A_c	—	TBD	µV/yr	C	

Figure 7. Offset at Half Scale vs Temperature

3.9 ADC Characteristics

Table 15. 12-bit ADC Operating Conditions

#	Symb	Characteristic	Conditions	Min	Typ[1]	Max	Unit	C	Comment
1	V_{DDAD}	Supply voltage	Absolute	1.8	—	3.6	V	D	
2	ΔV_{DDAD}		Delta to V_{DD} (V_{DD}-V_{DDAD})[2]	-100	0	+100	mV	D	
3	ΔV_{SSAD}	Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSAD})[2]	-100	0	+100	mV	D	
4	V_{REFH}	Ref Voltage High		1.13	V_{DDAD}	V_{DDAD}	V	D	
5	V_{REFL}	Ref Voltage Low		V_{SSAD}	V_{SSAD}	V_{SSAD}	V	D	
6	V_{ADIN}	Input Voltage		V_{REFL}	—	V_{REFH}	V	D	
7	C_{ADIN}	Input Capacitance		—	4	5	pF	C	
8	R_{ADIN}	Input Resistance		—	2	5	kΩ	C	
9	R_{AS}	Analog Source Resistance							External to MCU Assumes ADLSMP=0
			12-bit mode f_{ADCK} > 4 MHz	—	—	2	kΩ	C	
			f_{ADCK} < 4 MHz	—	—	5	kΩ	C	
			11/10-bit mode f_{ADCK} > 8 MHz	—	—	2	kΩ	C	
			4 MHz < f_{ADCK} < 8 MHz	—	—	5	kΩ	C	
			f_{ADCK} < 4 MHz	—	—	10	kΩ	C	
			9/8-bit mode f_{ADCK} > 4 MHz	—	—	5	kΩ	C	
			f_{ADCK} < 4 MHz	—	—	10	kΩ	C	
10	f_{ADCK}	ADC Conversion Clock Freq.	High Speed (ADLPC=0, ADHSC=1)	1.0	—	8.0	MHz	D	
			High Speed (ADLPC=0, ADHSC=0)	1.0	—	5.0	MHz	D	
			Low Power (ADLPC=1, ADHSC=1)	1.0	—	2.5	MHz	D	

1 Typical values assume V_{DDAD} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

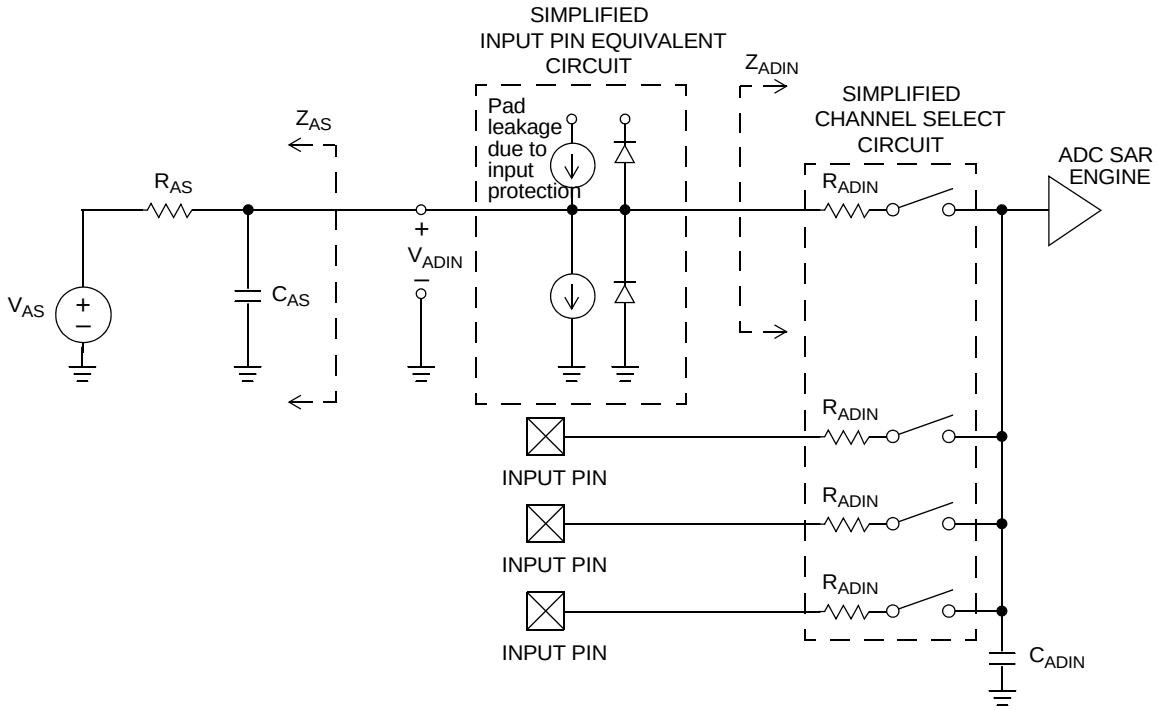


Figure 8. ADC Input Impedance Equivalency Diagram

Table 16. 12-bit SAR ADC Characteristics full operating range (V_{REFH} = V_{DDAD}, > 1.8, V_{REFL} = V_{SSAD} ≤ 8 MHz)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}	—	215	—	μA	T	ADLSMP=0 ADCO=1
	ADLPC=0, ADHSC=0		—	470	—			
	ADLPC=0, ADHSC=1		—	610	—			
Supply Current	Stop, Reset, Module Off	I_{DDAD}	—	0.01	—	μA	C	
ADC Asynchronous Clock Source	ADLPC=1, ADHSC=0	f_{ADACK}	—	2.4	—	MHz	P	t_{ADACK} = $1/f_{ADACK}$
	ADLPC=0, ADHSC=0		—	5.2	—			
	ADLPC=0, ADHSC=1		—	6.2	—			
Sample Time	See Block Guide for sample times							
Conversion Time	See Block Guide for conversion times							
Total Unadjusted Error	12-bit single-ended mode	TUE	—	±1.75	±3.5	LSB[3]	T	32x Hardware Averaging (AVGE = %1 AVGS = %11)
	11-bit differential mode 10-bit single-ended mode		— —	±0.7 ±0.8	±1.5 ±1.5		T	
	9-bit differential mode 8-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
Differential Non-Linearity	12-bit single-ended mode	DNL	—	±0.7	±1	LSB[2]	T	
	11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±0.75 ±0.75		T	
	9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
Integral Non-Linearity	12-bit single-ended mode	INL	—	±1.0	±2.5	LSB[2]	T	
	11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
	9-bit differential mode 8-bit single-ended mode		— —	±0.3 ±0.3	±0.5 ±0.5		T	

Table 16. 12-bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDAD}$, > 1.8, $V_{REFL} = V_{SSAD} \leq 8$ MHz) (Continued)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
Zero-Scale Error	12-bit single-ended mode	E_{ZS}	—	±0.7	±2.0	LSB[2]	T	$V_{ADIN} = V_{SSAD}$
	11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
	9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
Full-Scale Error	12-bit single-ended mode	E_{FS}	—	±1.0	±3.5	LSB[2]	T	$V_{ADIN} = V_{DDAD}$
	11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.5 ±1.5		T	
	9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
Quantization Error	All modes	E_Q	—	—	±0.5	LSB[2]	D	
Input Leakage Error	all modes	E_{IL}	$I_{In} * R_{AS}$			mV	D	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	–40°C – 25°C	m	—	1.646	—	mV/×C	C	
	25°C – 125°C		—	1.769	—			
Temp Sensor Voltage	25°C	V_{TEMP25}	—	701.2	—	mV	C	

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}

2 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3.10 MCG and External Oscillator (XOSC) Characteristics

Table 17. MCG (Temperature Range = –40 to 105°C Ambient)

#	Rating		Symbol	Min	Typical	Max	Unit	C
1	Internal reference startup time		t_{irefst}	—	55	100	µs	D
2	Average internal reference frequency	factory trimmed at VDD=3.0 V and temp=25°C	f_{int_ft}	—	31.25	—	kHz	C
		user trimmed		31.25	—	39.0625		C
3	DCO output frequency range - trimmed	Low range (DRS=00)	f_{dco_t}	16	—	20	MHz	C
		Mid range (DRS=01)		32	—	40		C
		High range[1] (DRS=10)		40	—	60		C
4	Resolution of trimmed DCO output frequency at fixed voltage and temperature	with FTRIM	$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$	C
		without FTRIM		—	± 0.2	± 0.4		C
5	Total deviation of trimmed DCO output frequency over voltage and temperature	over voltage and temperature	Δf_{dco_t}	—	±1.0	± 2	$\%f_{dco}$	p
		over fixed voltage and temp range of 0 - 70 °C		—	± 0.5	± 1		C
6	Acquisition time	FLL[2]	$t_{fll\_acquire}$	—	—	1	ms	C
		PLL[3]	$t_{pll\_acquire}$	—	—	1		D
7	Long term Jitter of DCO output clock (averaged over 2mS interval) [4]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$	C
8	VCO operating frequency		f_{vco}	7.0	—	55.0	MHz	D
9	PLL reference frequency range		f_{pll_ref}	1.0	—	2.0	MHz	D
10	Jitter of PLL output clock measured over 625ns [5]	Long term	$f_{pll\_jitter\_625\ ns}$	—	0.566[4]	—	$\%f_{pll}$	D
11	Lock frequency tolerance	Entry[6]	D_{lock}	± 1.49	—	± 2.98	%	D
		Exit[7]	D_{unl}	± 4.47	—	± 5.97		D
12	Lock time	FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s	D
		PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})		D
13	Loss of external clock minimum frequency - RANGE = 0		f_{loc_low}	(3/5) x f_{int_t}	—	—	kHz	D
14	Loss of external clock minimum frequency - RANGE = 1		f_{loc_high}	(16/5) x f_{int_t}	—	—	kHz	D

[1] This should not exceed the maximum CPU frequency for this device.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

5 625 ns represents 5 time quanta for CAN applications, under worst-case conditions of 8 MHz CAN bus clock, 1 Mbps CAN Bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

6 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

7 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

Table 18. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)	• Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		• High range (RANGE = 1), • FEE or FBE mode [2]	fhi	1	—	5	MHz
		• High range (RANGE = 1), • High gain (HGO = 1), • FBELP mode	fhi	1	—	16	MHz
		• High range (RANGE = 1), • Low power (HGO = 0), • FBELP mode	fhi	1	—	8	MHz
2	Load capacitors		C_1 C_2	See Note [3]			
3	Feedback resistor	Low range (32 kHz to 38.4 kHz)	R_F	—	10	—	MΩ
		High range (1 MHz to 16 MHz)	—	—	1	—	
4	Series resistor — Low range	Low Gain (HGO = 0)	R_S	—	0	—	kΩ
		High Gain (HGO = 1)		—	100	—	
5	Series resistor — High range	• Low Gain (HGO = 0) • High Gain (HGO = 1)					kΩ
		≥ 8 MHz	R_S	—	0	0	
		4 MHz		—	0	10	
		1 MHz		—	0	20	

Table 18. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Min	Typ[1]	Max	Unit
6	Crystal start-up time [4, 5]	Low range, low gain (RANGE = 0, HGO = 0)	t_{CSTL}	—	200	—	ms
		Low range, high gain (RANGE = 0, HGO = 1)		—	400	—	
		High range, low gain (RANGE = 1, HGO = 0)	t_{CSTH}	—	5	—	
		High range, high gain (RANGE = 1, HGO = 1)		—	15	—	

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 See crystal or resonator manufacturer's recommendation.

4 This parameter is characterized and not tested on each device.

5 Proper PC board layout procedures must be followed to achieve specifications.

3.11 Mini-FlexBus Timing Specifications

A multi-function external bus interface called Mini-FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 25.1666 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used.

All processor bus timings are synchronous; that is, input setup/hold and output delay are given in respect to the rising edge of a reference clock, MB_CLK. The MB_CLK frequency is half the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Mini-FlexBus output clock (MB_CLK). All other timing relationships can be derived from these values.

Table 19. Mini-FlexBus AC Timing Specifications

Num	C	Characteristic	Min	Max	Unit	Notes
—	—	Frequency of Operation	—	25.1666	MHz	—
MB1	D	Clock Period	39.73	—	ns	—
MB2	T	Output Valid	—	20	ns	1
MB3	D	Output Hold	1.0	—	ns	1
MB4	T	Input Setup	22	—	ns	2
MB5	D	Input Hold	10	—	ns	2

1 Specification is valid for all MB_A[19:0], MB_D[7:0], $\overline{\text{MB\_CS}}$[1:0], $\overline{\text{MB\_OE}}$, MB_R/$\overline{\text{W}}$, and MB_ALE.

2 Specification is valid for all MB_D[7:0].

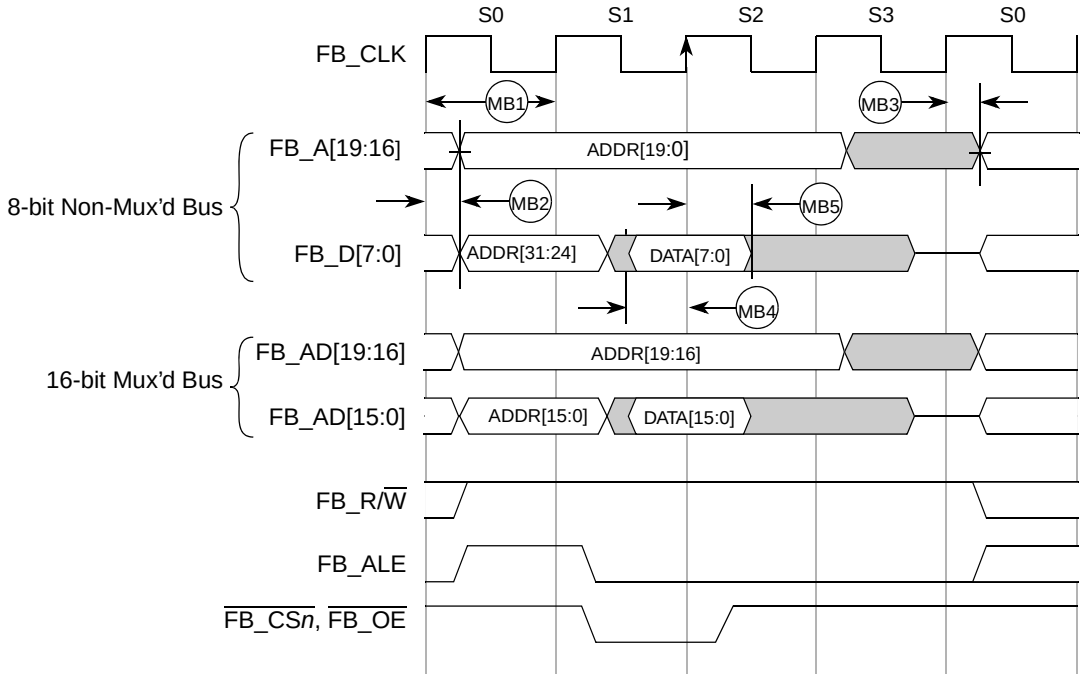


Figure 9. Mini-FlexBus Read Timing

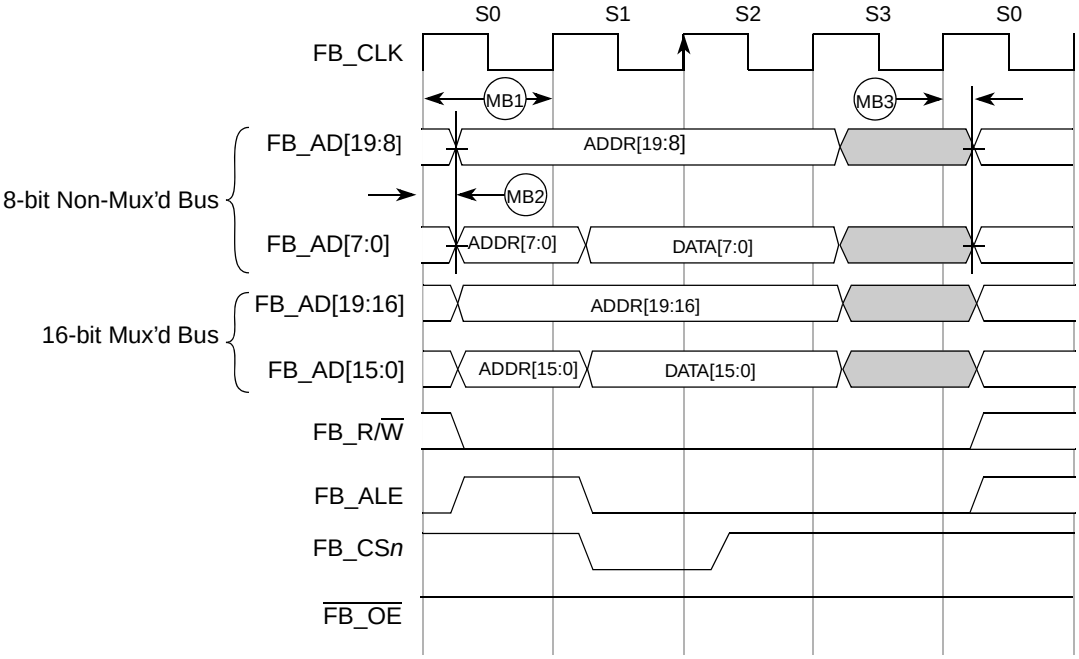


Figure 10. Mini-FlexBus Write Timing

3.12 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

3.12.1 Control Timing

Table 20. Control Timing

#	Symbol	Parameter		Min	Typical[1]	Max	C	Unit
1	f_{Bus}	Bus frequency ($t_{cyc} = 1/f_{Bus}$)						MHz
			$V_{DD} \geq 1.8$ V	dc	—	10	D	
			$V_{DD} > 2.1$ V	dc	—	20	D	
			$V_{DD} > 2.4$ V	dc	—	25.165	D	
2	t_{LPO}	Internal low-power oscillator period		800	990 (TBD)	1500	D	µs
3	t_{extrst}	External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)		100	—	—	D	ns
4	t_{rstdrv}	Reset low drive		66 x t_{cyc}	—	—	D	ns
5	t_{MSSU}	Active background debug mode latch setup time		500	—	—	D	ns
6	t_{MSH}	Active background debug mode latch hold time		100	—	—	D	ns
7	t_{ILIH}, t_{IHIL}	IRQ pulse width • Asynchronous path[2] • Synchronous path[3]		100 1.5 x t_{cyc}	—	—	D	ns
8	t_{ILIH}, t_{IHIL}	KBIPx pulse width • Asynchronous path[2] • Synchronous path[3]		100 1.5 x t_{cyc}	—	—	D	ns

Table 20. Control Timing

#	Symbol	Parameter	Min	Typical[1]	Max	C	Unit
9	t_{Rise}, t_{Fall}	Port rise and fall time (load = 50 pF)[4], Low Drive					ns
		Slew rate control disabled (PTxSE = 0)	—	11	—	D	
		Slew rate control enabled (PTxSE = 1)	—	35	—	D	
		Slew rate control disabled (PTxSE = 0)	—	40	—	D	
		Slew rate control enabled (PTxSE = 1)	—	75	—	D	

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

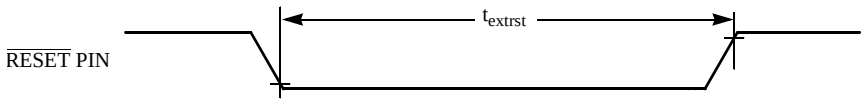


Figure 11. Reset Timing

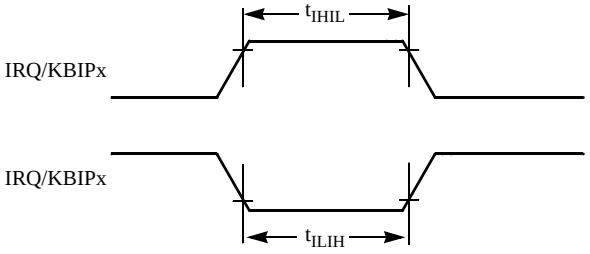


Figure 12. IRQ/KBIPx Timing

3.12.2 TPM Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 21. TPM Input Timing

#	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

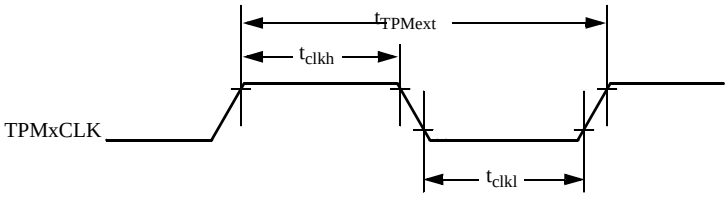


Figure 13. Timer External Clock

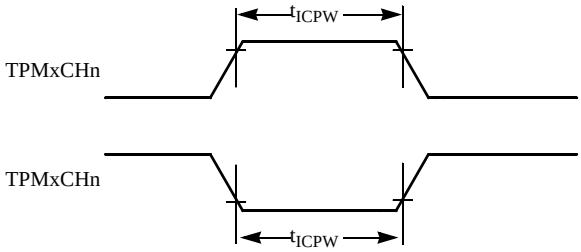


Figure 14. Timer Input Capture Pulse

3.13 SPI Characteristics

Table 22 and Figure 15 through Figure 18 describe the timing requirements for the SPI system.

Table 22. SPI Timing

No.[1]	Characteristic[2]	Symbol	Min	Max	Unit	C
1	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz Hz	D
2	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}	D
3	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}	D
4	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}	D
5	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns	D
6	Data setup time (inputs) Master Slave	t_{SU} t_{SU}	15 15	— —	ns ns	D
7	Data hold time (inputs) Master Slave	t_{HI} t_{HI}	0 25	— —	ns ns	D
8	Slave access time[3]	t_a	—	1	t_{cyc}	D
9	Slave MISO disable time[4]	t_{dis}	—	1	t_{cyc}	D
10	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns	D
11	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns	D
12	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ 25	ns ns	D
13	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ 25	ns ns	D

1 Numbers in this column identify elements in Figure 15 through Figure 18.

2 All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

3 Time to data active from high-impedance state.

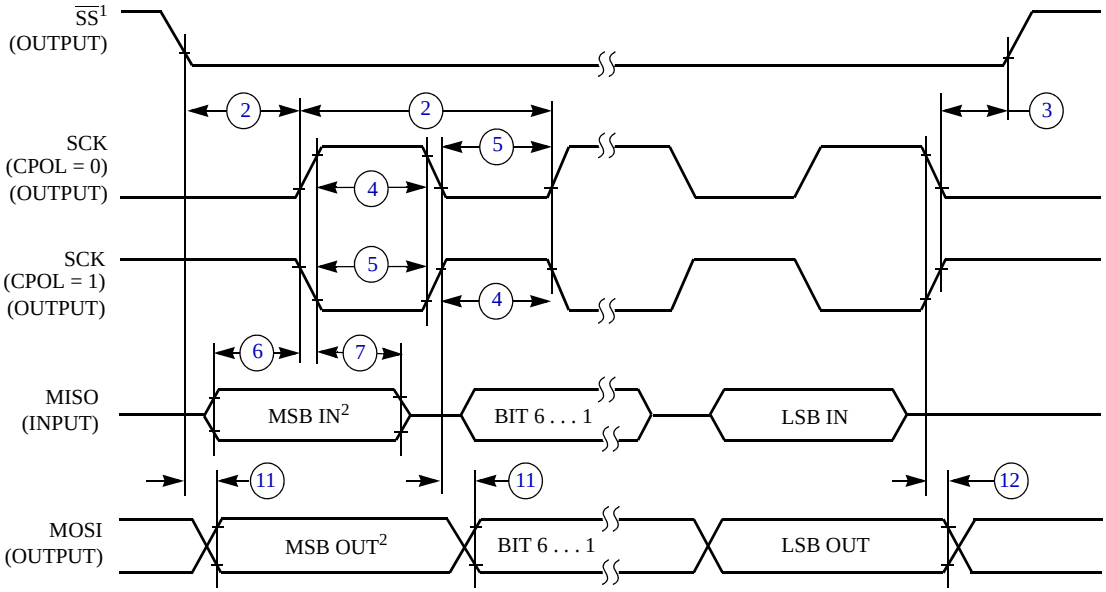
4 Hold time to high-impedance state.

Table 23. SPI Electrical Characteristic

Num[1]	Characteristic[2]	Symbol	Min	Max	Unit	C
1	Operating frequency Master Slave	 f_{op} f_{op}	 $f_{Bus}/2048$ dc	 $f_{Bus}/2$ $f_{Bus}/4$	Hz	D
2	Cycle time Master Slave	 t_{SCK} t_{SCK}	 2 4	 2048 —	t_{cyc}	D
3	Enable lead time Master Slave	 t_{Lead} t_{Lead}	 — 1/2	 1/2 —	t_{SCK}	D
4	Enable lag time Master Slave	 t_{Lag} t_{Lag}	 — 1/2	 1/2 —	t_{SCK}	D
5	Clock (SPSCK) high time Master and Slave	t_{SCKH}	1/2 t_{SCK} – 25	—	ns	D
6	Clock (SPSCK) low time Master and Slave	t_{SCKL}	1/2 t_{SCK} – 25	—	ns	D
7	Data setup time (inputs) Master Slave	 $t_{SI(M)}$ $t_{SI(S)}$	 30 30	 — —	ns	D
8	Data hold time (inputs) Master Slave	 $t_{HI(M)}$ $t_{HI(S)}$	 30 30	 — —	ns	D
9	Access time, slave	t_A	0	40	ns	D
10	Disable time, slave	t_{dis}	—	40	ns	D
11	Data setup time (outputs) Master Slave	 t_{SO} t_{SO}	 25 25	 — —	ns	D
12	Data hold time (outputs) Master Slave	 t_{HO} t_{HO}	 –10 –10	 — —	ns	D

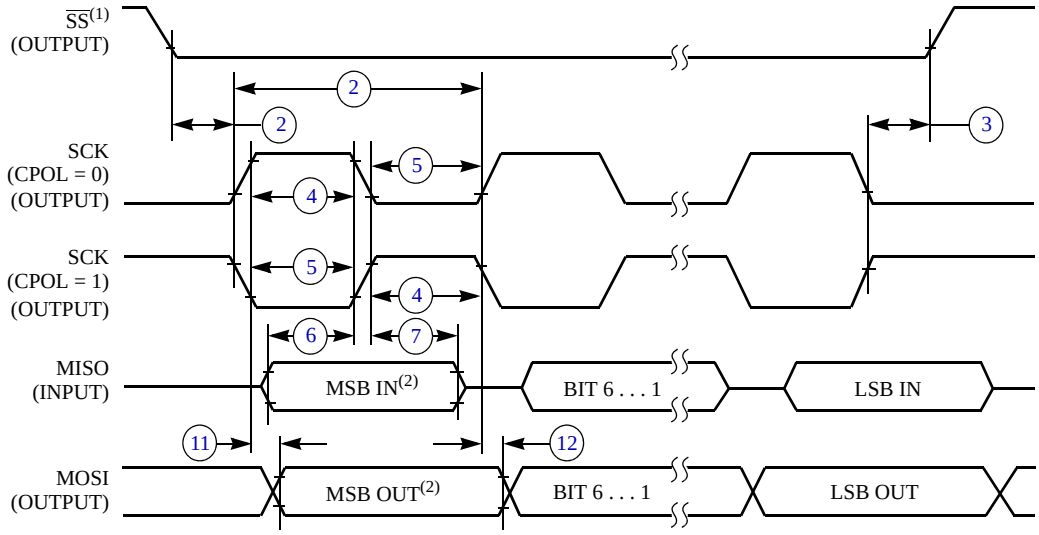
1 Refer to Figure 15 through Figure 18.

2 All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.



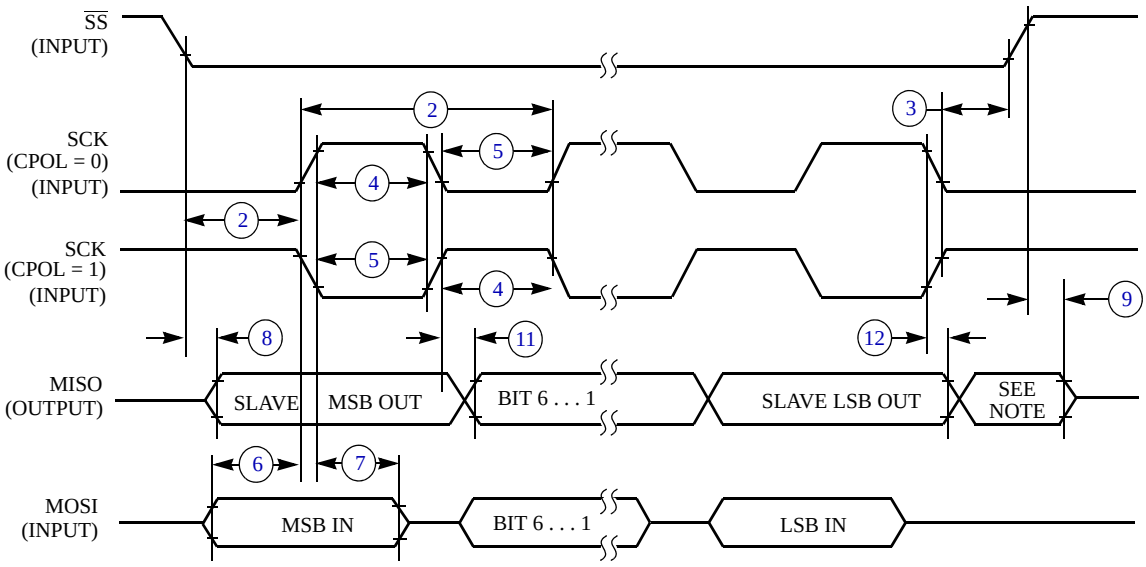
NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

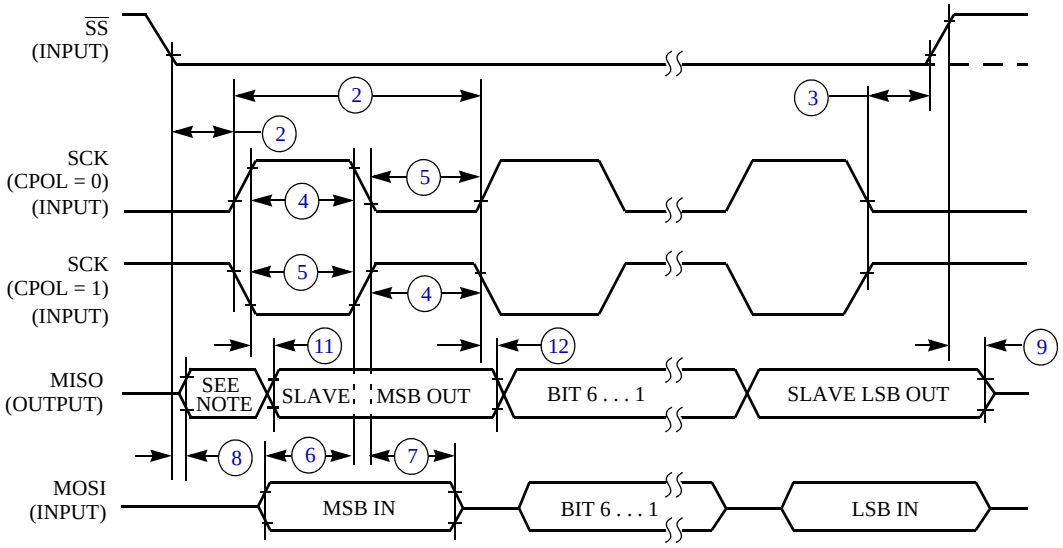
Figure 16. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined, but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined, but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

3.14 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter in the Reference Manual for this device (MCF51JE256RM).

Table 24. Flash Characteristics

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage for program/erase -40°C to 105°C	$V_{prog/erase}$	1.8	—	3.6	V	D
2	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V	D
3	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz	D
4	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs	D
5	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}	P
6	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}	P
7	Page erase time[2]	t_{Page}	4000			t_{Fcyc}	P
8	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}	P
9	Program/erase endurance[3] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles	C
10	Data retention[4]	t_{D_ret}	15	100	—	years	C

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

3.15 USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

Table 25. Internal USB 3.3 V Voltage Regulator Characteristics

#	Characteristic	Symbol	Min	Typ	Max	Unit	C
1	Regulator operating voltage	V_{regin}	3.9	—	5.5	V	C
2	VREG output	V_{regout}	3	3.3	3.6	V	P
3	V_{USB33} input with internal VREG disabled	$V_{usb33in}$	3	3.3	3.6	V	C
4	VREG Quiescent Current	I_{VRQ}	—	0.5	—	mA	C

3.16 VREF Electrical Specifications

Table 26. VREF Electrical Specifications

Num	Characteristic	Symbol	Min	Max	Unit	C
1	Supply voltage	V_{DDA}	1.80	3.6	V	C
2	Temperature	T_A	–40	105	°C	C
3	Output Load Capacitance	C_L	—	100	nf	D
4	Maximum Load	—	—	10	mA	—
5	Voltage Reference Output with Factory Trim. V_{DD} = 3 V.	Vout	1.148	1.152	V	P
6	Temperature Drift (Vmin - Vmax across the full temperature range)	Tdrift	—	10 (TBD)	mV[1]	T
7	Aging Coefficient	Ac	—	TBD	ppm/year	C
8	Powered down Current (Off Mode, VREFEN=0, VRSTEN=0)	I	—	0.10	µA	C
9	Bandgap only (MODE_LV[1:0] = 00)	I	—	75	µA	T
10	Low-Power buffer (MODE_LV[1:0] = 01)	I	—	125	µA	T
11	Tight-Regulation buffer (MODE_LV[1:0] = 10)	I	—	1.1	mA	T
12	Load Regulation MODE_LV = 10	—	—	100	µV/mA	C
13	Line Regulation (Power Supply Rejection)	DC	—	TBD	mV	C
14		AC	TBD	—	dB	

1 See typical chart below.

Table 27. VREF Limited Range Operating Requirements

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Temperature	T_A	0	50	°C	C	

Table 28. VREF Limited Range Operating Behaviors

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Voltage Reference Output with Factory Trim	Vout	TBD	TBD	µA	C	

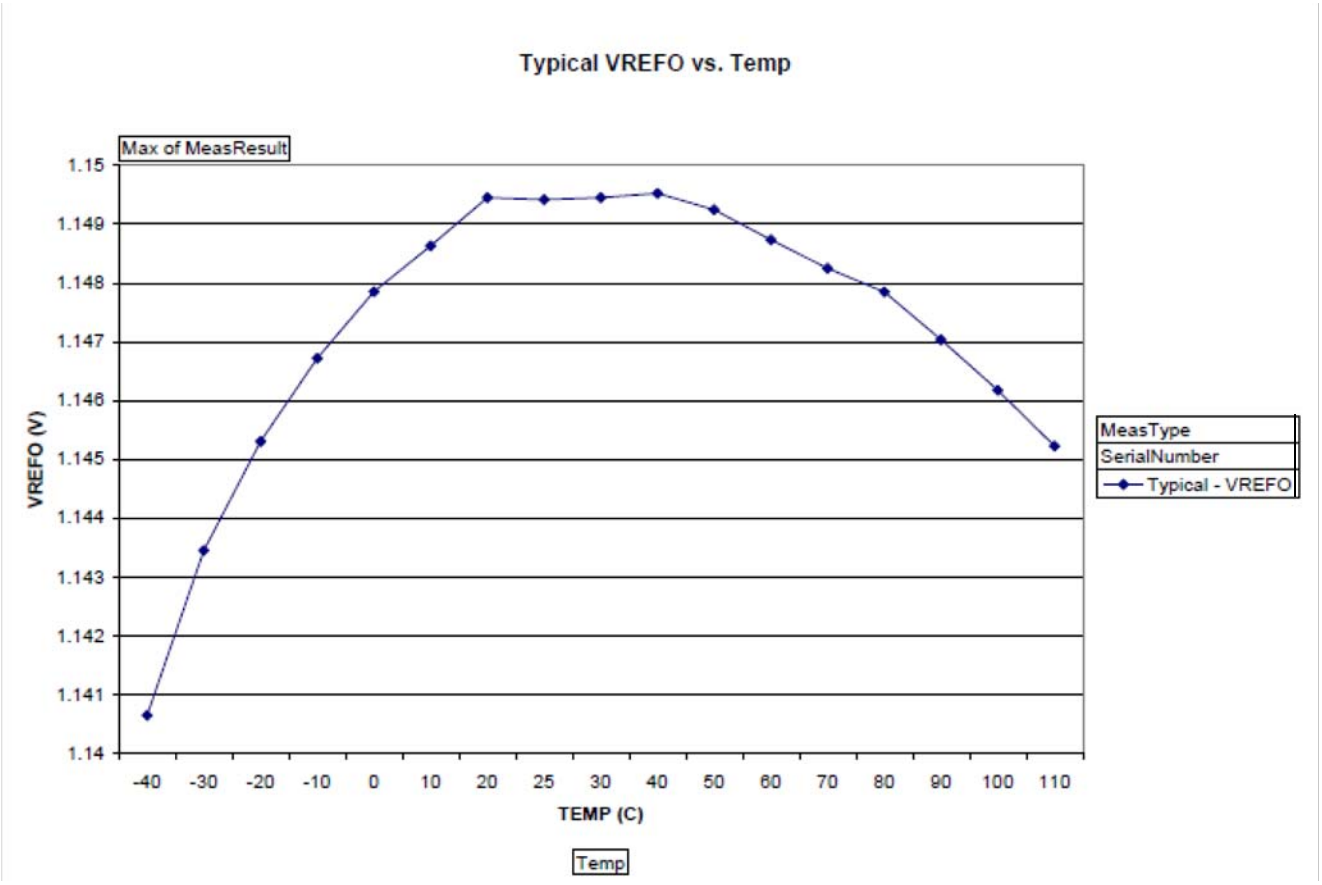


Figure 19. Typical Output vs. Temperature

TBD

Figure 20. Typical Output vs. V_{DD}

4 Ordering Information

This section contains ordering information for the device numbering system. See Table 2 for feature summary by package information.

4.1 Part Numbers

Table 29. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (Kbytes)	Package	Temperature
MCF51JE256VML	MCF51JE256 ColdFire Microcontroller	256K/32K	104 MAPBGA	–40 to 105 °C
MCF51JE256VLL	MCF51JE256 ColdFire Microcontroller	256K/32K	100 LQFP	–40 to 105 °C
MCF51JE256VMB	MCF51JE256 ColdFire Microcontroller	256K/32K	81 MAPBGA	–40 to 105 °C
MCF51JE256VLK	MCF51JE256 ColdFire Microcontroller	256K/32K	80 LQFP	–40 to 105 °C
MCF51JE128VMB	MCF51JE128 ColdFire Microcontroller	128K/32K	81 MAPBGA	–40 to 105 °C
MCF51JE256CML	MCF51JE256 ColdFire Microcontroller	256K/32K	104 MAPBGA	–40 to 85 °C
MCF51JE256CLL	MCF51JE256 ColdFire Microcontroller	256K/32K	100 LQFP	–40 to 85 °C
MCF51JE256CMB	MCF51JE256 ColdFire Microcontroller	256K/32K	81 MAPBGA	–40 to 85 °C
MCF51JE256CLK	MCF51JE256 ColdFire Microcontroller	256K/32K	80 LQFP	–40 to 85 °C
MCF51JE128CMB	MCF51JE128 ColdFire Microcontroller	128K/32K	81 MAPBGA	–40 to 85 °C
MCF51JE128CLK	MCF51JE128 ColdFire Microcontroller	128K/32K	80 LQFP	–40 to 85 °C

4.2 Package Information

Table 30. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
100	Low Quad Flat Package	LQFP	LL	983-03	98ASS23308W
80	Low Quad Flat Package	LQFP	LK	1418	98ASS23174W
104	MAPBGA Package	MAPBGA	ML	1285-02	98ARH98267A
81	MAPBGA Package	MAPBGA	MB	1662-01	98ASA10670D

4.3 Mechanical Drawings

Table 30 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MCF51JE256/128 Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 30, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 30) in the "Enter Keyword" search box at the top of the page.

5 Revision History

This section lists major changes between versions of the MCF51JE256 Data Sheet.

Table 31. Revision History

Revision	Date	Description
0	March/April 09	Initial Draft
1	July 09	• Revised to follow standard template. • Removed extraneous headings from the TOC. • Corrected units for Monotoncity to be blank in for the DAC specification. • Updated ADC characteristic tables to include 16-Bit SAR in headings.
2	July 09	• Changed MCG (XOSC) Electricals Table - Row 2, Average Internal Reference Frequency typical value from 32.768 to 31.25.
3	April 10	• Updated Thermal Characteristics table. Reinserted the 81 and 104 MapBGA devices. • Revised the ESD and Latch-Up Protection Characeristic description to read: Latch-up Current at T_A = 125°C. • Changed Table . DC Characteristics rows 2 and 4, to 1.8 V, ILoad = -600 mA conditions to 1.8 V, ILoad = 600μA respectively. • Corrected the 16-bit SAR ADC Operating Condition table Ref Voltage High Min value to be 1.13 instead of 1.15. • Updated the ADC electricals. • Inserted the Mini-FlexBus Timing Specifications. • Added a Temp Drift parameter to the VREF Electrical Specifications. • Removed the S08 Naming Convention diagram. • Updated the Orderable Part Number Summary to include the Freescale Part Number suffixes. • Completed the Package Description table values. • Changed the 80LQFP package drawing from 98ARL10530D to 98ASS23174W. Updated electrical characteristic data.

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