TERIDIAN SEMICONDUCTOR CORP.

Simplifying System Integration™

73M1903C
Evaluation Board User Manual

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Table of Contents

Figures

Tables

1 Introduction

The Teridian Semiconductor Corporation (TSC) 73M1903C Evaluation Board is a Modem Analog Front End Evaluation Board with an on-board DAA for evaluating the 73M1903C device. This device can support up to V.90 modulation and demodulation on typical DSP or CPU systems available in the market.

The 73M1903C Evaluation Board incorporates a 73M1903C integrated circuit, a US, CTR21 or World Wide DAA circuit for interfacing with the telephone line and an audio amplifier and speaker for line monitoring during the call progress period. The Evaluation Board supports the evaluation of the 73M1903C Modem Analog Front End device for universal modem applications and interfaces to a general purpose DSP or CPU system.

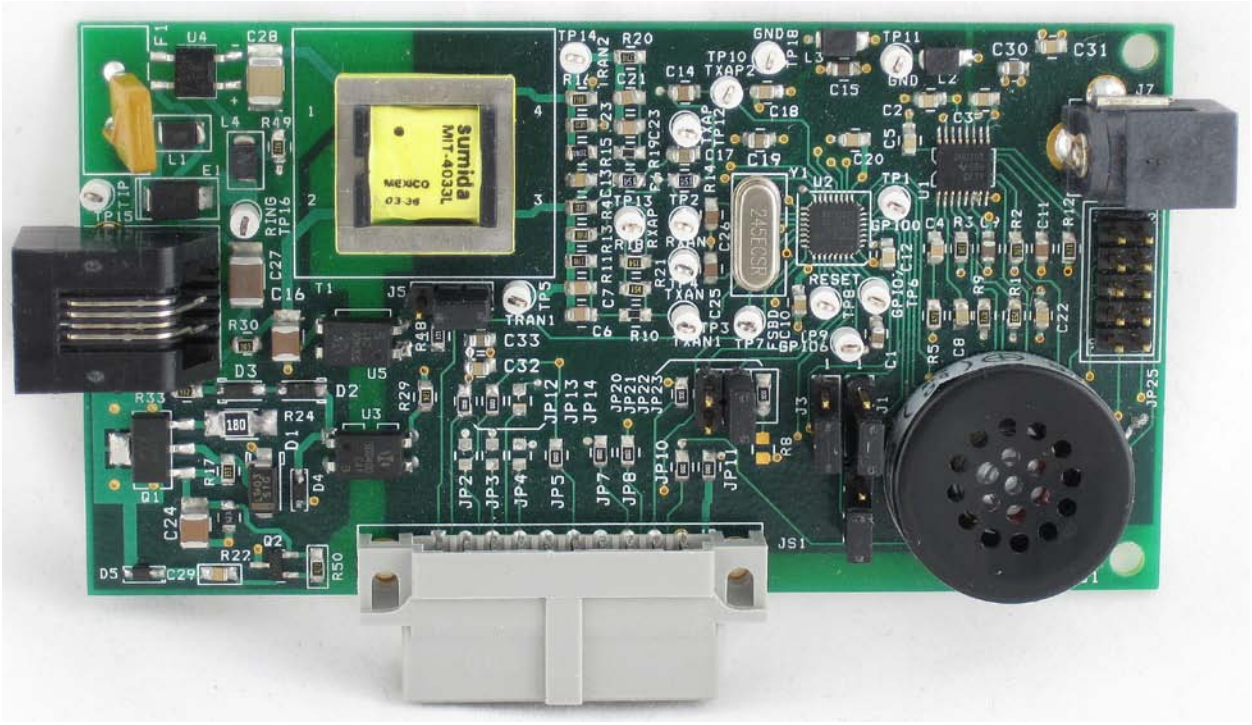

Figure 1: 73M1903C Evaluation Board

1.1 Safety and ESD Notes

THE 73M1903C EVALUATION BOARD IS ESD SENSITIVE! ESD PRECAUTIONS SHOULD BE TAKEN WHEN HANDLING THE EVALUATION BOARD!

1.2 Evaluation Board Host Interfaces

The 73M1903C Evaluation Board includes a Modem Analog Front End (MAFE) Interface with a 20-pin right angle connector to connect to a target DSP or CPU system. The Evaluation Board also includes a 3.3 V power receptacle for powering the on board circuits from either the target system or an external power supply.

2 System Description

Figure 2 shows a block diagram of the 73M1903C Evaluation Board. This section includes descriptions of:

- Modem Analog Front End (MAFE) Host System Interface
- 73M1903C Register Map
- System Initialization

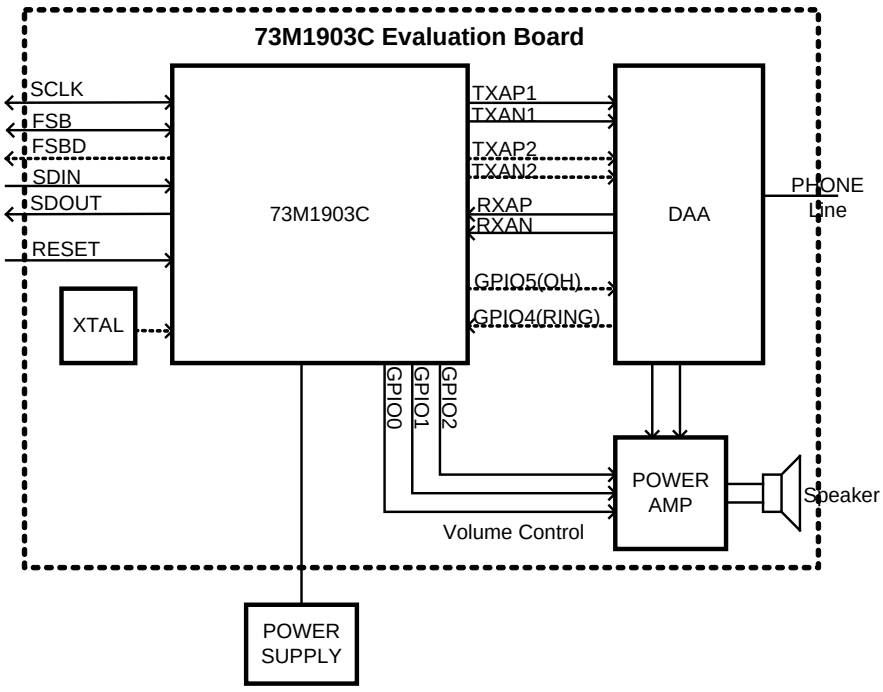

Figure 2: 73M1903C Evaluation Board Block Diagram

2.1 MAFE Interface

The Modem Analog Front End (MAFE) Interface is a serial port integrated into the 73M1903C device to interface to a host controller or a DSP. This serial data port is a bi-directional port that is supported by most DSPs available in the market.

The MAFE interface requires one end to act as a master and the other as a slave. The 73M1903C device can be configured either as a master or as a slave (refer to Figure 3). Multiple 73M1903C devices can also be daisy chained in a single master and multiple slave configuration (refer to Figure 4).

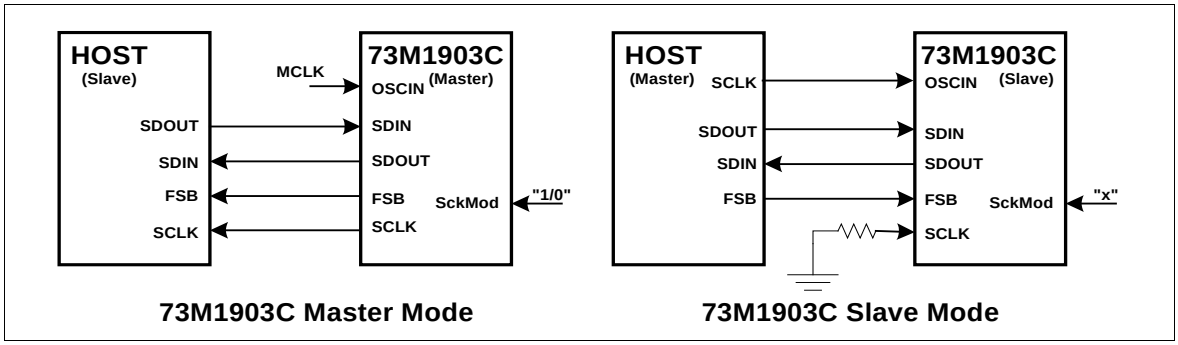

Figure 3: 73M1903C in Master or Slave Configuration

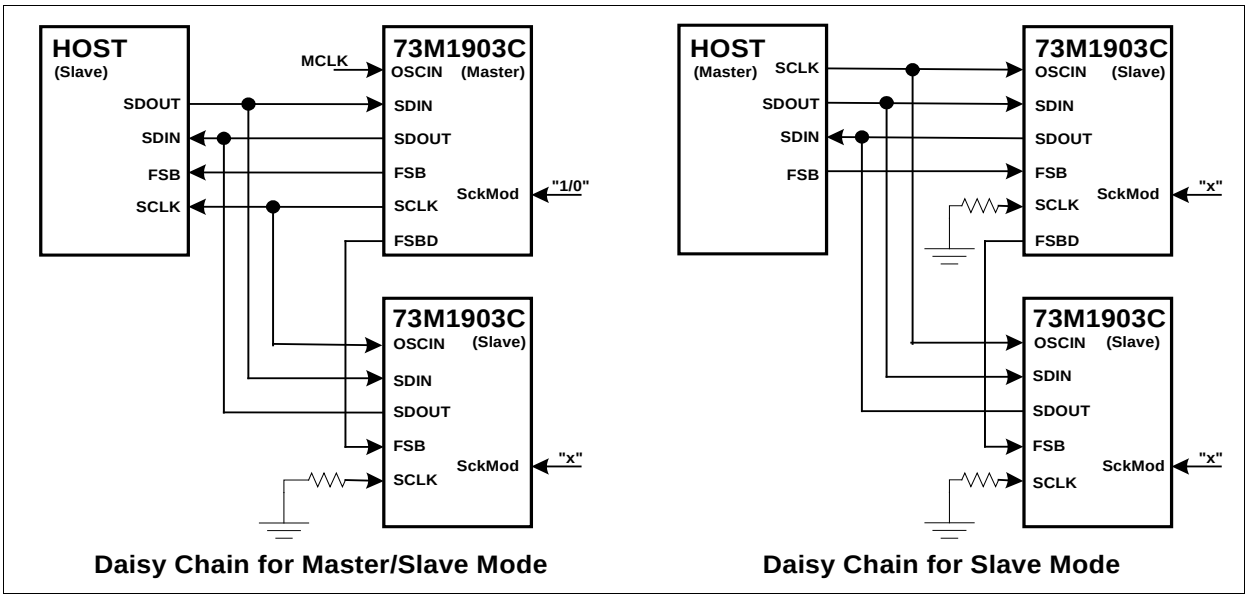

Figure 4: 73M1903C Daisy Chain Configurations

Figure 5 and Figure 6 show the MAFE and serial data timing diagrams.

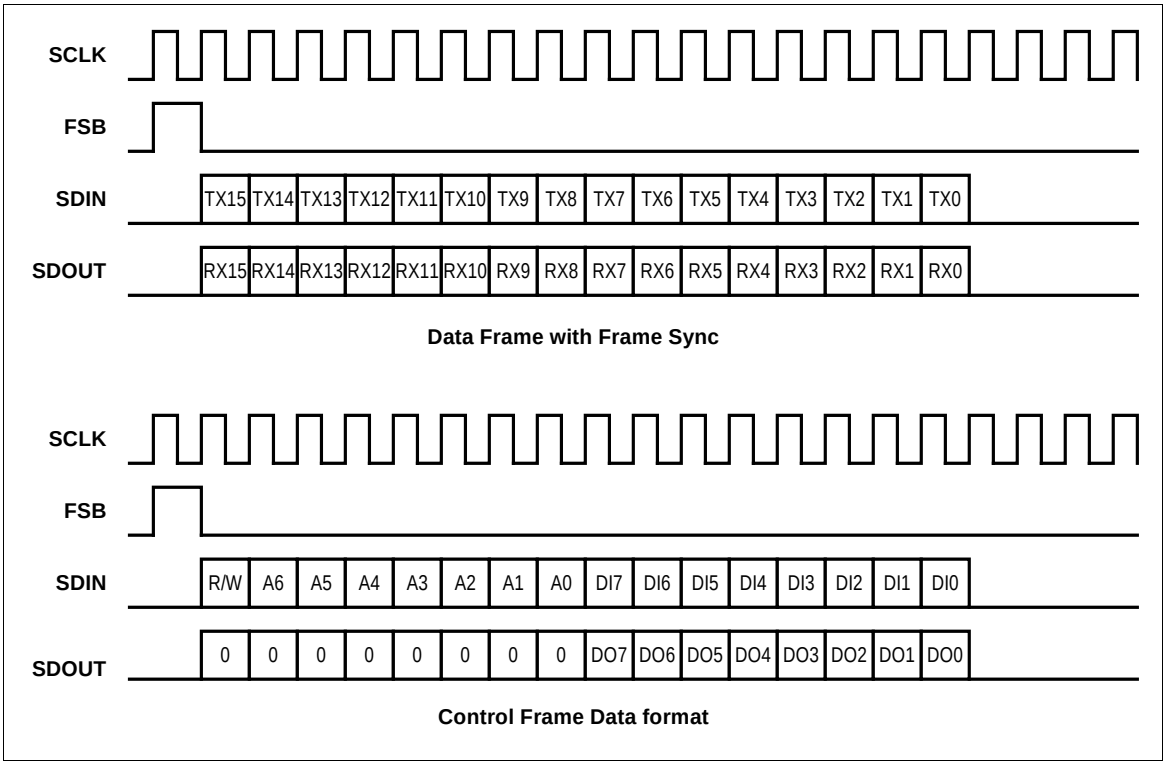

Figure 5: MAFE Timing Diagram

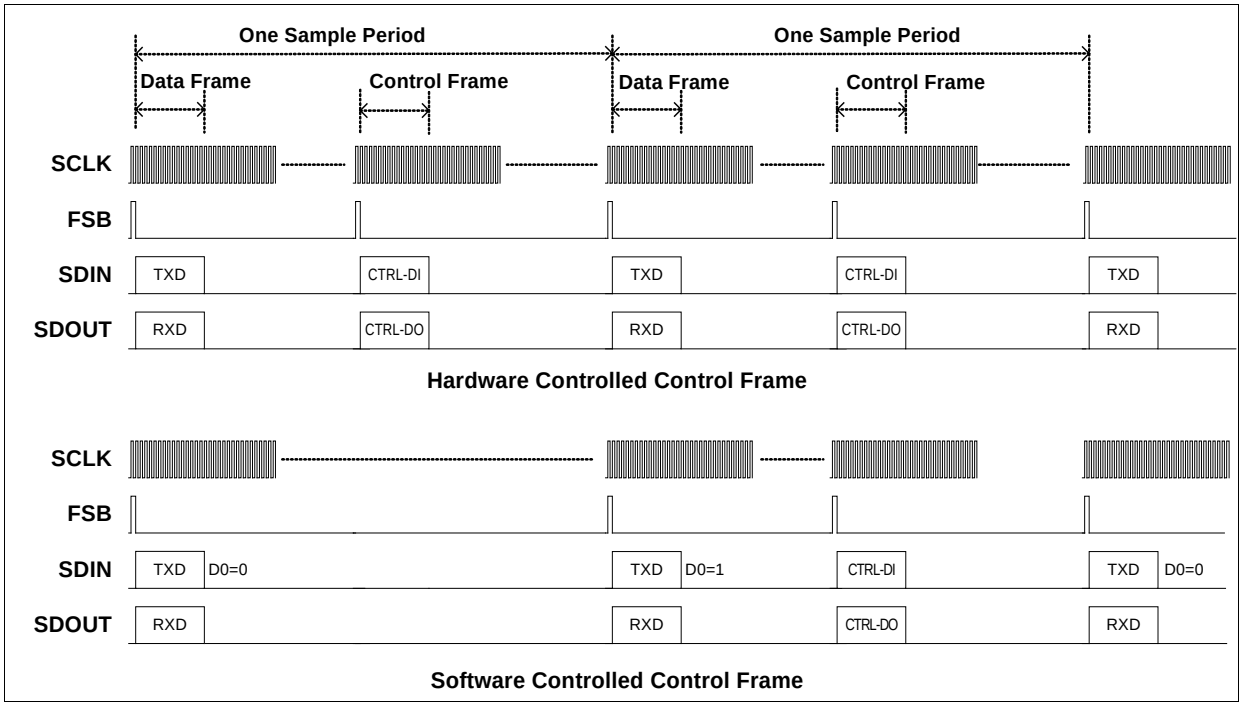

Figure 6: Serial Data Timing

2.2 73M1903C Register Map

Table 1 shows the memory map of the addressable registers in the 73M1903C. Each register can be read or written by a host controller or a DSP using the MAFE interface control frame format.

All registers and their bits are described in detail in the *73M1903C Data Sheet*.

Table 1: 73M1903C Register Memory Map

Address	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	0x08	ENFE	SelTX2	TXBST1	TXBST0	TXDIS	RXG1	RXG0	RXGAIN
0x01	0x00	TMEN	DIGLB	ANALB	INTLB	CkoutEn	RXPULL	SPOS	HC
0x02	0xFF	GPIO7	GPIO 6	GPIO 5	GPIO 4	GPIO 3	GPIO 2	GPIO 1	GPIO 0
0x03	0xFF	DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
0x04	0x00	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
0x05	0x00	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
0x06	0x50	Rev3	Rev2	Rev1	Rev0	FSBDEn	Trim(2)	Trim(1)	Trim(0)
0x07	0x00	Unused	TestPll	Tclksel1	Tclksel0	ATX	DTX	ARX	DRX
0x08	0x00	Pseq7	Pseq6	Pseq5	Pseq4	Pseq3	Pseq2	Pseq1	Pseq0
0x09	0x0A	Prst2	Prst1	Prst0	Pdvsr4	Pdvsr3	Pdvsr2	Pdvsr1	Pdvsr0
0x0A	0x22	Ichp3	Ichp2	Ichp1	Ichp0	FL	Kvco2	Kvco1	Kvco0
0x0B	0x12	Unused	Ndvsr6	Ndvsr5	Ndvsr4	Ndvsr3	Ndvsr2	Ndvsr1	Ndvsr0
0x0C	0x00	Nseq7	Nseq6	Nseq5	Nseq4	Nseq3	Nseq2	Nseq1	Nseq0
0x0D	0xC0	Xtal1	Xtal0	LokdetEn	ThLk0	Unused	Nrst2	Nrst1	Nrst0
0x0E	0x00	Frcvco	PwdnPLL	Lokdet	Unused	Unused	Unused	Unused	Unused

2.3 73M1903C System Initialization

The following example shows the sequence to follow to bring the 73M1903C device out of reset and to start up after power up.

The 73M1903C device does not have a power on reset circuit. For proper operation, a reset signal must be asserted from the host by pulling the 73M1903C reset pin low for approximately 100 ns or longer after the power is stabilized. The 73M1903C device will be ready to use within 100 µs after the removal of the reset pulse from the reset pin.

RESET the 73M1903 Device

1. Power up the system.
2. Wait for the 3.3 V power to become stable.
3. Hold the 73M1903C RESET pin low for 100 ns or longer then let it go high.
4. Wait for 100 µs for the PLL and OSC to be stabilized.

INITIALIZE the 73M1903 Device

There are control operating modes; Hardware Control and Software control. In the Hardware Control mode, the serial interface will alternate between data frames and control frames. If synchronization is lost and it is not known whether a data or control frame is being sent, it is necessary to reinitialize the HC mode. Since there isn't way to initially tell the difference between whether a control frame or data frame is being sent, it is necessary to send a reset of this bit in two consecutive frames, and the procedure for this is as follows:

A. Frame Synchronization
   1. Reset the HC bit (Register 0x01 bit 0) in a frame sequence.

2. Reset the HC bit (Register 0x01 bit 0) in next frame sequence.

At this point, the 73M1903C is guaranteed to be in the software controlled control frame mode. All the MAFE serial data will be data only unless the host requests a control frame by setting the LSB of the TX data to a one by setting bit 0 of data frame. The following frame will then be a control frame.

B. Control Frame Generation

- Software Controlled Control Frame
  1. Mask TXD Bit 0 as 1 to request a subsequent control frame.
  2. Write or read the 73M1903C register using the MAFE control data format.
  3. Make sure to Mask TXD bit 0 as 0 if the control frame is not needed.

- Hardware Controlled Control Frame
  1. Mask TXD Bit 0 as 1 to request a subsequent control frame.
  2. Set the HC bit (Register 0x01 bit 0) using the MAFE control data format in the next frame.

  From this point on, there will be alternating data and control frames. Make sure not to miss this sequence. This is needed to initialize the HC mode.

Example 1: Using the Software Controlled Control Frame:

```
static const U16 init_afe_config[] =        // MUST HAVE Data(LSB=1), Control, Data(LSB=1), Control,.. FRAMES
{
  CTRL2|0x00, CTRL2|0x00,                   // Force to Software controlled control frame
  CTRL_FRAME, CTRL13|0x00,                  // Force to Xtal clock
  CTRL_FRAME, CTRL1|ENFE,                   // Enable Analog
  CTRL_FRAME, CTRL2|0x00,                   //
  CTRL_FRAME, GPIO|0x00,                    //
  CTRL_FRAME, GDIR|0xD0,                    // GPIO 7,6,4=in 5,3,2,1,0=output
  CTRL_FRAME, GIE|0x00,
  CTRL_FRAME, GIP|0x00,
  CTRL_FRAME, BGTRIM|0x00,
  CTRL_FRAME, TEST|0x00,
  CTRL_FRAME, CTRL08|AFE_CTRL08,            // Timing chain set up
  CTRL_FRAME, CTRL09|AFE_CTRL09,
  CTRL_FRAME, CTRL10|AFE_CTRL10,
  CTRL_FRAME, CTRL11|AFE_CTRL11,
  CTRL_FRAME, CTRL12H|AFE_CTRL12H,
  CTRL_FRAME, CTRL12L|AFE_CTRL12L,
  CTRL_FRAME, RWB|GPIO,                     // Delay for 2 sample cycle time to
  CTRL_FRAME, RWB|GPIO,                     // let PLL settle before Lockdet
  CTRL_FRAME, CTRL13|AFE_CTRL13
};
note: CTRL_FRAME = 0x0001
```

Example 2: Using the Automatic Control Frame (Hardware Controlled Control Frame)

```
static const U16 init_afe_config[] =        // MUST HAVE Dummy Data, Control, Dummy Data, Control,..
FRAMES
{
  CTRL2|0x00, CTRL2|0x00,                   // Force to Software controlled control frame
  CTRL_FRAME, CTRL13|0x00,                  // Force to Xtal clock
  CTRL_FRAME, CTRL1|ENFE|HC,                // Enable Analog
  0x0000, GPIO|0x00,                        // Forces DATA to be 0x0000
  0x0000, GDIR|0xD0,                        // GPIO 7,6,4=in 5,3,2,1,0=output
```

```
  0x0000, GIE|0x00,
  0x0000, GIP|0x00,
  0x0000, BGTRIM|0x00,
  0x0000, TEST|0x00,
  0x0000, CTRL08|AFE_CTRL08,          // Timing chain set up
  0x0000, CTRL09|AFE_CTRL09,
  0x0000, CTRL10|AFE_CTRL10,
  0x0000, CTRL11|AFE_CTRL11,
  0x0000, CTRL12H|AFE_CTRL12H,
  0x0000, CTRL12L|AFE_CTRL12L,
  0x0000, RWB|GPIO,                   // Delay for 2 sample cycle time to
  0x0000, RWB|GPIO,                   // let PLL settle before Lockdet
  0x0000, CTRL13|AFE_CTRL13
};
```

2.4 Typical Sample Rate Settings

Table 2 shows the register values to set up for each example sample rate using a 24.576 MHz crystal.

Table 2: Control Register Settings for Example Sample Rates

Register (Addr)	Sample Rate				
	7.2 kHz	**8 kHz**	**9.6 kHz**	**14.4 kHz**	**16 kHz**
CTRL08 (0x08)	0x00	0x00	0x00	0x00	0x00
CTRL09 (0x09)	0x0A	0x0A	0x0A	0x0A	0x08
CTRL10 (0x0A)	0x10	0x11	0x22	0x26	0x17
CTRL11 (0x0B)	0x0D	0x0F	0x12	0x1B	0x18
CTRL12H (0x0C)	0x02	0x00	0x00	0x00	0x00
CTRL12L (0x0D)	0xC1	0xC0	0xC0	0xC0	0xC0

3 Hardware Description

3.1 Board Settings: Jumpers and Connectors

Figure 7 shows all the connectors and jumpers available on 73M1903C Evaluation Board.

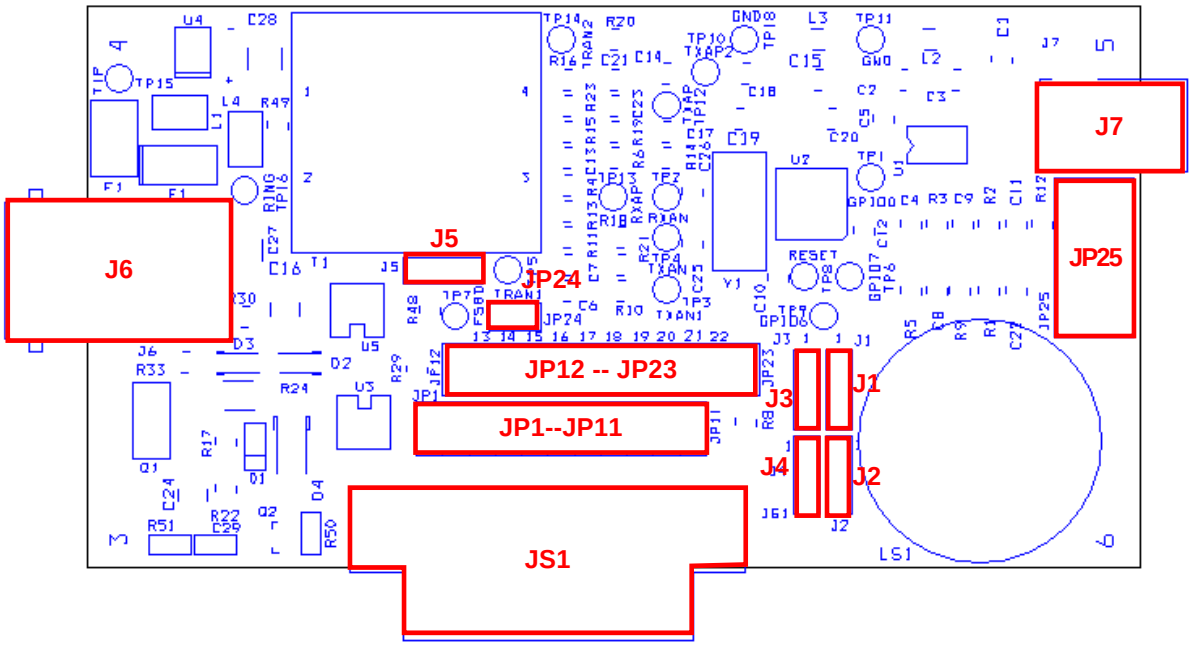

Figure 7: 73M1903C Evaluation Board Jumpers and Connectors

Table 3 lists the Evaluation Board connectors. JS1 is the main connector for interfacing to a host processor or DSP board. The pins of this connector are configurable by jumper settings (JP1 to JP24). Table 5 describes the details of the jumper settings.

J6 is a modular connector for connection to the telephone line and J7 is for power connection from the main board or from an external power supply.

JP25 is an alternative MAFE interface connector whose pin assignments are show in Table 4.

Table 3: 73M1903C Evaluation Board Connectors

Schematic and PCB Reference	Name	Description
JS1	CONN SOCKET 10X2	20-pin connector to interface the 73M1903C Evaluation Board to a host controller main board.
J6	RJ-11	Telephone line connector.
J7	3.3V external supply	Plug for connecting external 3.3 V DC power supply.
JP25	HEADER 5X2	10 pin interface connector / MAFE test points.

Table 4: JP25 Pin Assignments

Pin#	Name	Pin#	Name
1	NC (SCLK in slave mode)	6	SCLK
2	RINGD	7	AFEIN
3	HOOK	8	AFEOUT
4	FSB	9	RESET
5	FSBD	10	GND

Table 5: 73M1903C Evaluation Board Jumper Description

Schematic and PCB Reference	Name	Description
JP1	Jumper Strap	Two-pin header that allows JS1 pin 1 to be assigned as FSBD. SHUNT: JS1 pin1 = FSBD OPEN: JS1 pin 1 is floating
JP2	Jumper Strap	Two-pin header that allows JS1 pin 4 to be assigned as AFEIN. SHUNT: JS1 pin4 = AFEIN OPEN: JS1 pin 4 is controlled by JP13
JP3	Jumper Strap	Two-pin header that allows JS1 pin 5 to be assigned as AFEOUT. SHUNT: JS1 pin 5 = AFEOUT OPEN: JS1 pin 5 is floating
JP4	Jumper Strap	Two-pin header that allows JS1 pin 7 to be assigned as FS. SHUNT: JS1 pin 7 = FS OPEN: JS1 pin 7 is controlled by JP15
JP5	Jumper Strap	Two-pin header that allows JS1 pin 9 to be assigned as FS. SHUNT: JS1 pin 9 = FS OPEN: JS1 pin 9 is controlled by JP16
JP6	Jumper Strap	Two-pin header that allows JS1 pin 11 to be assigned as AFEOUT. SHUNT: JS1 pin11 = AFEOUT OPEN: JS1 pin 11 is floating
JP7	Jumper Strap	Two-pin header that allows JS1 pin 15 to be assigned as AFEIN. SHUNT: JS1 pin 15 = AFEIN OPEN: JS1 pin 15 is controlled by JP19
JP8	Jumper Strap	Two-pin header that allows JS1 pin 16 to be assigned as AFEOUT. SHUNT: JS1 pin 16 = AFEOUT OPEN: JS1 pin 16 is floating
JP9	Jumper Strap	Two-pin header that allows JS1 pin 17 to be assigned as AFEIN. SHUNT: JS1 pin 17 = AFEIN OPEN: JS1 pin 17is controlled by JP20
JP10	Jumper Strap	Two-pin header that allows JS1 pin 18 to be assigned as FS. SHUNT: JS1 pin 18 = FS OPEN: JS1 pin 18 is floating
JP11	Jumper Strap	Two-pin header that allows JS1 pin 20 to be assigned as digital signal ground. SHUNT: JS1 pin 20 =GND OPEN: JS1 pin 20 is floating
JP12	Jumper Strap	Two-pin header that allows JS1 pin 2 to be assigned as VCCD (3.3 V Digital supply). SHUNT: JS1 pin 2 = VCCD OPEN: JS1 pin 2 is floating

<table>
<tr><th>Schematic and PCB Reference</th><th>Name</th><th>Description</th></tr>
<tr><td>JP13</td><td>Jumper Strap</td><td>Two-pin header that allows JS1 pin 4 to be assigned as RESET.
SHUNT: JS1 pin 4 = RESET
OPEN: JS1 pin 4 is controlled by JP2</td></tr>
<tr><td>JP14</td><td>Jumper Strap</td><td>Two-pin header that allows JS1 pin 6 to be assigned as SCLK.
SHUNT: JS1 pin 6 = SCLK
OPEN: JS1 pin 6 is floating</td></tr>
<tr><td>JP15</td><td>Jumper Strap</td><td>Two-pin header that allows JS1 pin 7 to be assigned as RESET.
SHUNT: JS1 pin 7 = SCLK
OPEN: JS1 pin 7 is controlled by JP4</td></tr>
<tr><td>JP16</td><td>Jumper Strap</td><td>Two-pin header that allows JS1 pin 9 to be assigned as RINGD.
SHUNT: JS1 pin 9 = RINGD
OPEN: JS1 pin 9 is controlled by JP5</td></tr>
<tr><td>JP17</td><td>Jumper Strap</td><td>Two-pin header that allows JS1 pin 10 to be assigned as HOOK.
SHUNT: JS1 pin 10 = HOOK
OPEN: JS1 pin 10 is floating</td></tr>
<tr><td>JP18</td><td>Jumper Strap</td><td>Two-pin header that allows JS1 pin 13 to be assigned as HOOK.
SHUNT: JS1 pin 13 = HOOK
OPEN: JS1 pin 13 is floating</td></tr>
<tr><td>JP19</td><td>Jumper Strap</td><td>Two-pin header that allows JS1 pin15 to be assigned as RINGD.
SHUNT: JS1 pin 15 = RINGD
OPEN: JS1 pin 15 is controlled by JP7</td></tr>
<tr><td>JP20</td><td>Jumper Strap</td><td>Two-pin header that allows JS1 pin 17 to be assigned as SCLK.
SHUNT: JS1 pin 17 = SCLK
OPEN: JS1 pin 17 is controlled by JP9</td></tr>
<tr><td>JP21</td><td>TESTB</td><td>Two-pin header that selects factory test. This pin must be left open for normal operation.</td></tr>
<tr><td>JP22</td><td>CLKMODE</td><td>Two-pin header that selects the 73M1903C Clock Mode.
SHUNT: 73M1903C 32 clock per frame
OPEN: 73M1903C continuous clock mode</td></tr>
<tr><td>JP23</td><td>Jumper Strap</td><td>Two-pin header to select Slave mode.
SHUNT: 73M1903C MASTER configuration. (R8 must be depopulated)
OPEN: 73M1903C SLAVE configuration (R8 must be populated)</td></tr>
<tr><td>JP24</td><td>Jumper Strap</td><td>Two-pin header to enable Daisy Chaining.
SHUNT: 72M1903C FSBD signal is connected to JP25 pin3 and JS1 pin through JP1 (Daisy Chain enable)
OPEN: 73M1903C FSBD pin is isolated (No Daisy Chain)</td></tr>
<tr><td>J1, J2, J3</td><td>Speaker Volume control</td><td>Three-pin header for selecting the line monitor speaker volume.
Manual volume control:
<table>
<tr><th>J1</th><th>J2</th><th>J3</th><th>Volume Control</th></tr>
<tr><td>1-2</td><td>don’t care</td><td>don’t care</td><td>Shutdown (MUTE)</td></tr>
<tr><td>open</td><td>1-2</td><td>1-2</td><td>6 db Amp gain</td></tr>
<tr><td>open</td><td>1-2</td><td>open</td><td>12 db Amp gain</td></tr>
<tr><td>open</td><td>open</td><td>1-2</td><td>18 db Amp gain</td></tr>
<tr><td>open</td><td>open</td><td>open</td><td>23.4 db Amp gain</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Schematic and PCB Reference</th><th>Name</th><th>Description</th></tr>
<tr><td></td><td></td><td>Software volume control by the 73M1903C GPIO:
The 73M1903C GPIO 0, 1 and 2 must be configured as output).
J1(2-3), J2(2-3), J3(2-3)

<table>
<tr><th>GPIO2</th><th>GPIO1</th><th>GPIO0</th><th>Volume Control</th></tr>
<tr><td>Low</td><td>don’t care</td><td>don’t care</td><td>Shutdown (MUTE)</td></tr>
<tr><td>High</td><td>Low</td><td>Low</td><td>6 db Amp gain</td></tr>
<tr><td>High</td><td>Low</td><td>High</td><td>12 db Amp gain</td></tr>
<tr><td>High</td><td>High</td><td>Low</td><td>18 db Amp gain</td></tr>
<tr><td>High</td><td>High</td><td>High</td><td>23.4 db Amp gain</td></tr>
</table>
</td></tr>
<tr><td>J4</td><td>Ring Detector Output</td><td>Three-pin header that selects the Ring Detector output to connect to either GPIO4 of the 73M1903C or to a Host CPU GPIO through JS1 or JP25.
1-2: Ring Detector output is fed to 73M1903C GPIO4 (GPIO4 must be configured as an input).
2-3: Ring detector output is directed to a host controller through either JS1 or JP25.</td></tr>
<tr><td>J5</td><td>Off-hook Control</td><td>Three-pin header that selects the Off-hook control by either 73M1903C GPIO5 or by a Host CPU GPIO through JS1 or JP25.
1-2: Off-hook is controlled by 73M1903C GPIO5 (GPIO5 must be configured as an output).
2-3: Off-hook is controlled by a host output through either JS1 or JP25.</td></tr>
</table>

3.2 Board Physical and Operating Information

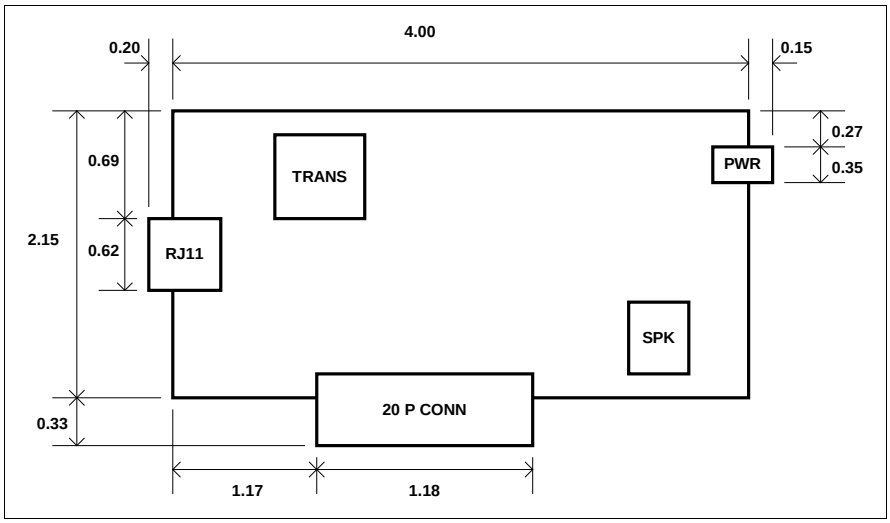

Figure 8: 73M1903C Evaluation Board PCB Dimensions

PCB Dimensions

- Size 4.00 x 2.15” (101.60 x 54.60 mm)
- Height with components and solder 0.65” (16.5 mm)

Environmental

- Operating Temperature -40 °C to +85 °C
  (crystal oscillator function is affected outside –10 °C to +60 °C range)
- Storage Temperature -65 °C to 150 °C

Power Supply

- DC Input Voltage (powered from DC supply) 3.3 VDC ± 0.5 V
- Supply Current 25 mA (off-hook at room temperature) typical

4 73M1903C Evaluation Board Schematics, PCB Layouts and Bill of Materials

4.1 Schematic

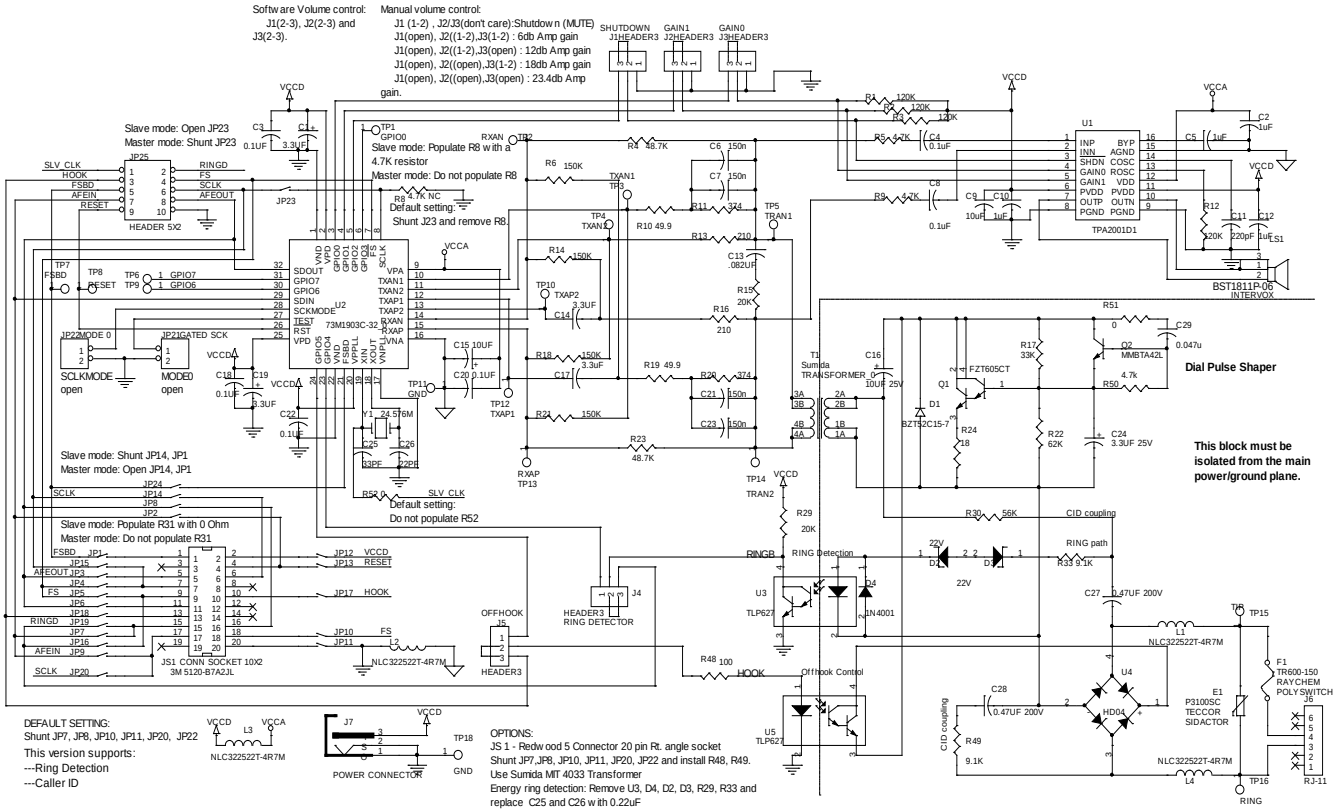

Figure 9: 73M1903C Evaluation Board Electrical Schematic

4.2 PCB Layouts

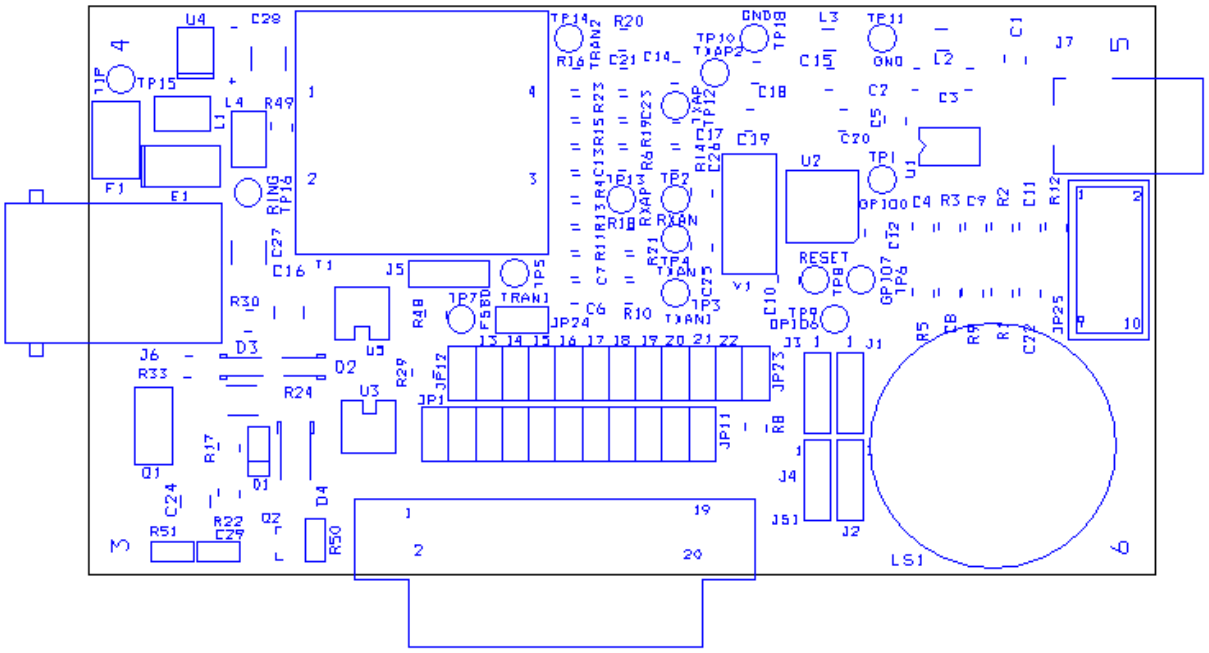

Figure 10: 73M1903C Evaluation Board Silk Screen Top

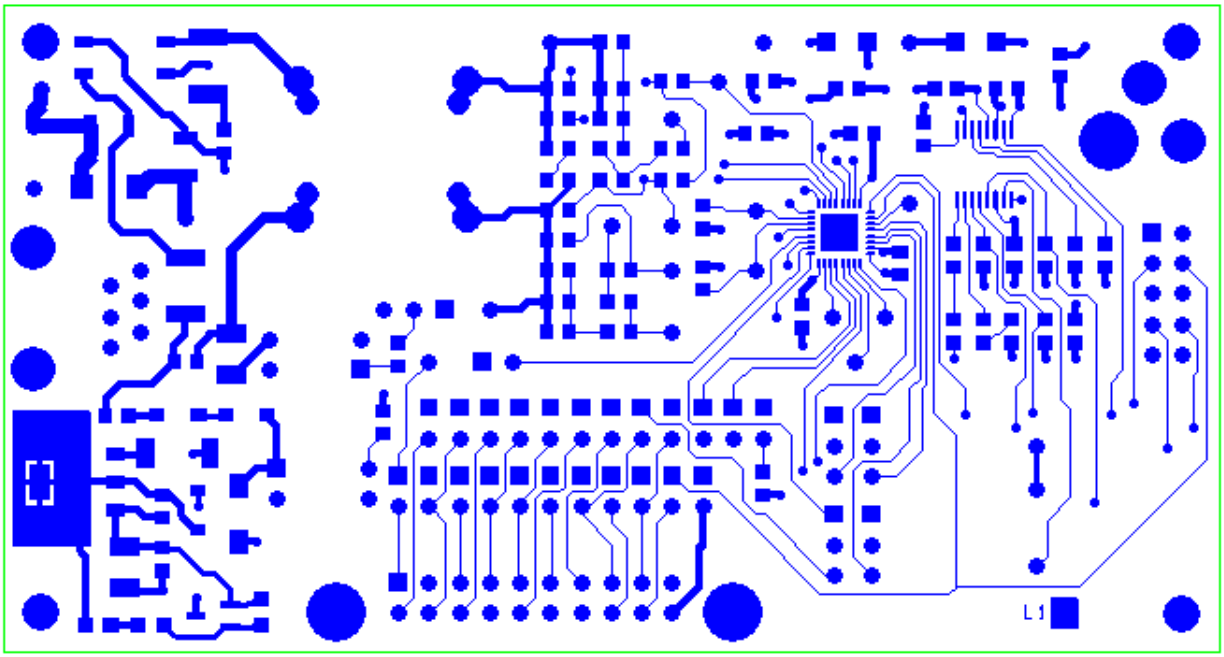

Figure 11: 73M1903C Evaluation Board Top Signal Layer

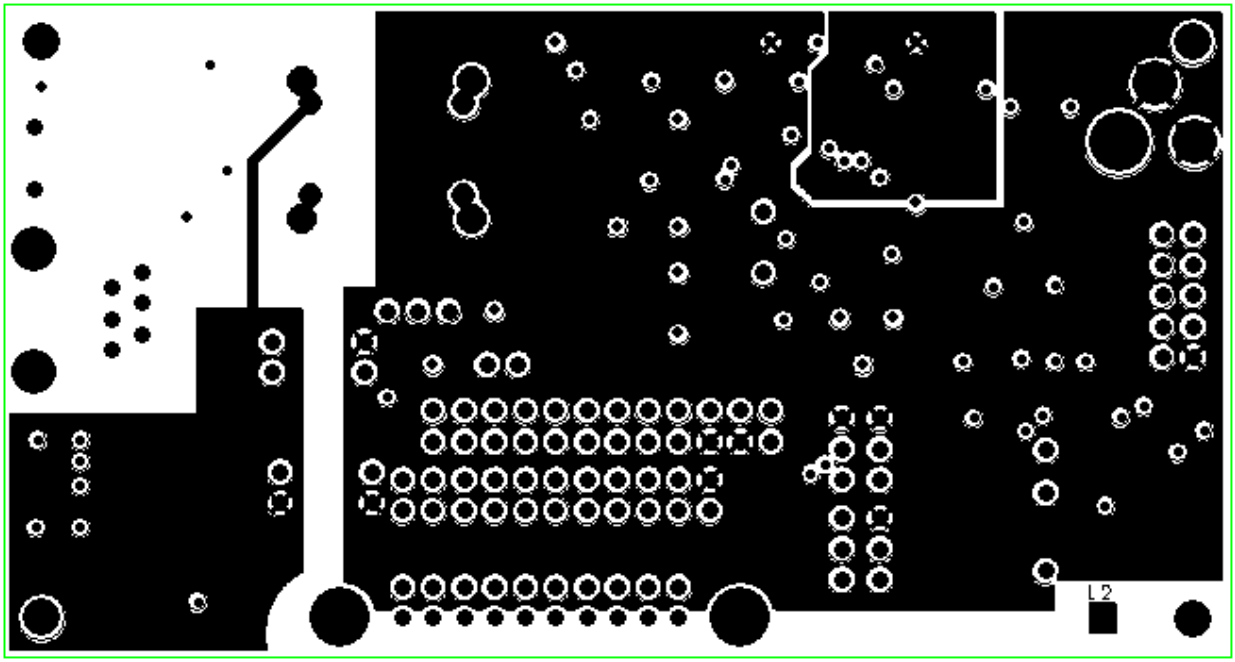

Figure 12: 73M1903C Evaluation Board Layer 2 – Ground Plane

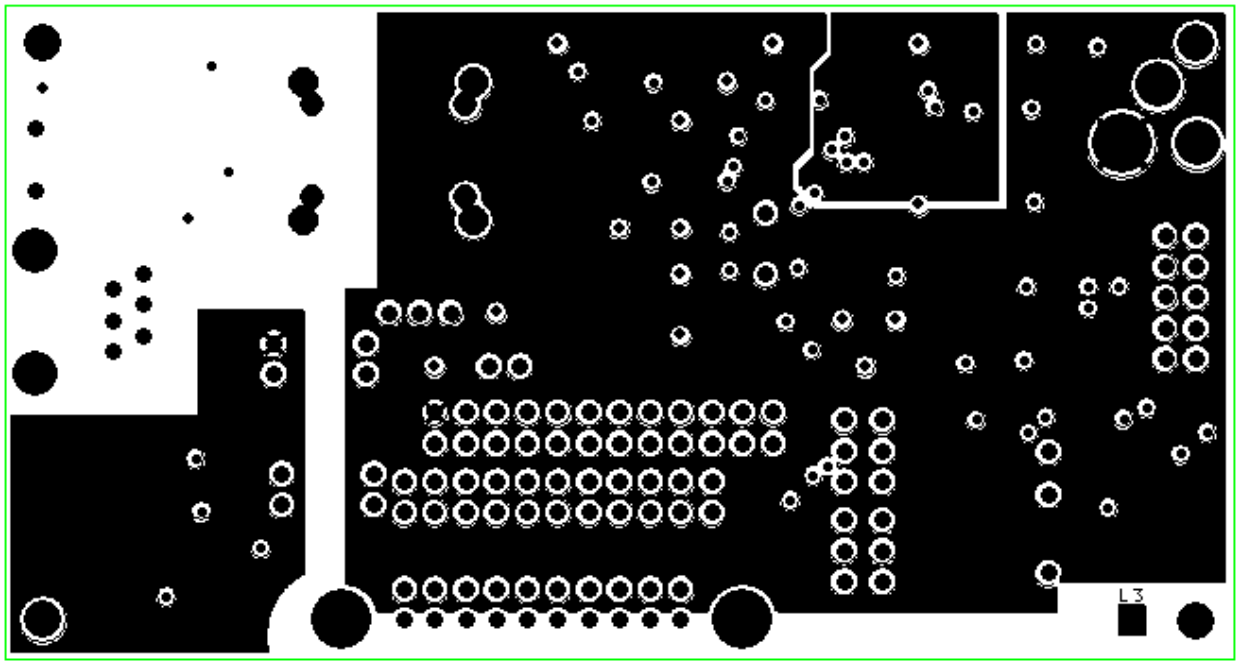

Figure 13: 73M1903C Evaluation Board Layer 3 – Supply Plane

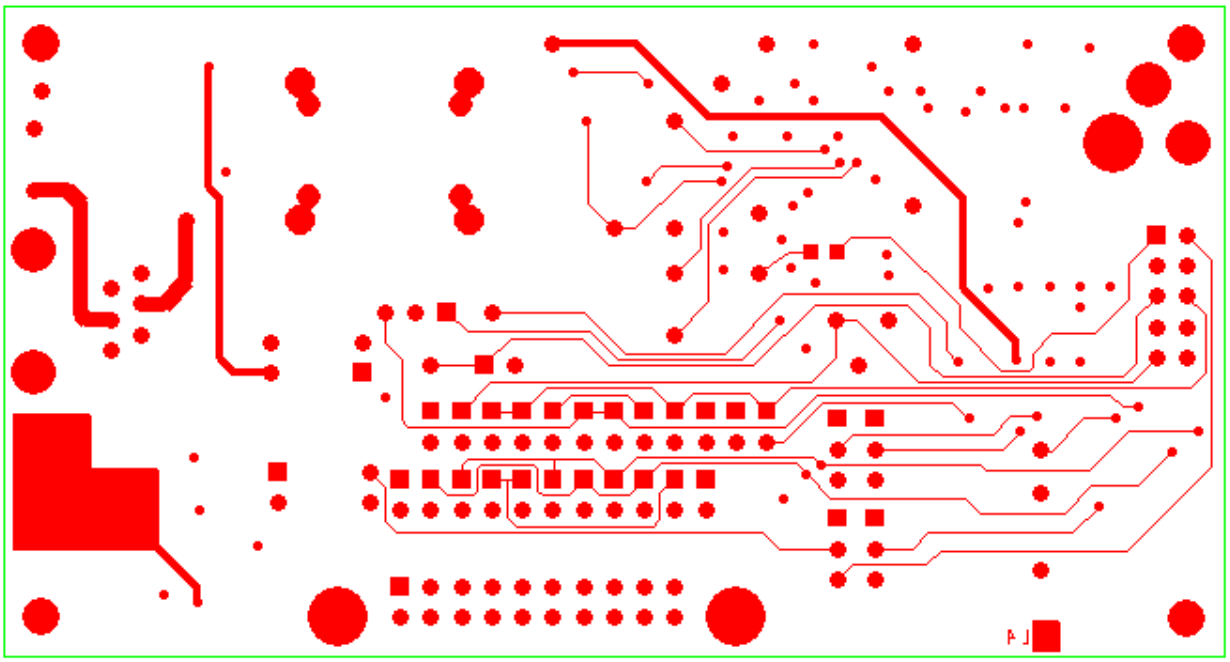

Figure 14: 73M1903C Evaluation Board Bottom Signal Layer

4.3 Bill of Materials

Table 6 provides the bill of materials for the 73M1903C Evaluation Board schematic provided in Figure 9.

Table 6: 73M1903C Evaluation Board Bill of Materials

Item	Qty.	Reference	Part	Manufacturer
1	4	C1, C14, C17, C19	3.3 µF	Panasonic
2	4	C2, C5, C10, C12	1 µF	Panasonic
3	6	C3, C4, C8, C18, C20, C22	0.1 µF	Panasonic
4	4	C6, C7, C21, C23	150 nF (0.15 µF)	Panasonic
5	2	C9,C15	10 µF	Panasonic
6	1	C11	2 nF (0.002 µF)	Panasonic
7	1	C13	0.082 µF	Panasonic
8	1	C16	3.3 µF 16 V / 25 V	Kemet
9	1	C24	10 µF 16 V / 25 V	Panasonic
10	1	C25	33 pF	Panasonic
11	1	C26	22 pF	Panasonic
12	2	C27, C28	0.47 µF 250 V	UTC
13	1	C29	0.047 µF 50 V	Panasonic
14	2	D1	15 V / MMSZ15T1	On Semiconductor
15	2	D3, D2	22 V/ MMSZ5251BDICT	Diodes
16	1	D4	S1G	Diodes
17	1	E1	P3100SC	Teccor
18	1	F1	TR600-150	Raychem
19	24	JP1 – JP24	2 pin HEADER	Sullin
20	1	JP25	HEADER 5X2	Sullin
21	1	JS1	CONN SOCKET 10x2	3M
22	5	J1, J2, J3, J4, J5	3 pin HEADER	Sullin
23	1	J6	RJ-11	AMP/Tyco
24	1	J7	power connector	Switchcraft
25	1	LS1	Speaker/AT-2308	Intervox
26	4	L1, L2, L3, L4	NLC322522T-4R7M	TDK
27	1	Q1	FZT605	Zetex Ind.
28	1	Q2	MMBTA42	On Semiconductor
29	4	R1, R2, R3, R12,	120 kΩ	Panasonic
30	2	R23, R4	48.7 kΩ	Panasonic
31	3	R5, R9, R50	4.7 kΩ	Panasonic
32	4	R6, R14, R18, R21	150 kΩ	Panasonic
33	2	R19, R10	49.9 Ω	Panasonic
34	2	R11, R20	374 Ω	Panasonic
35	2	R13, R16	210 Ω	Panasonic
36	2	R15,R29	20 kΩ	Panasonic
37	1	R17	33 kΩ	Panasonic
38	1	R22	62 kΩ	Panasonic
39	1	R24	18 Ω ½ W	Panasonic
40	2	R33, R49	9.1 kΩ	Panasonic
41	1	R30	56 kΩ	Panasonic
42	1	R48	100 Ω	Panasonic

Item	Qty.	Reference	Part	Manufacturer
44	1	R51, R52	0 Ω	Panasonic
45	17	TP1 – TP18	Test point	Sullin
46	1	T1	EMIT4033L	Sumita
47	1	U1	TPA2001D1	TI
48	1	U2	73M1903C-32	Teridian
49	2	U3, U5	TLP627	Toshiba
50	1	U4	H04	Diodes
51	1	Y1	24.576 MHz	ECS inc

5 Ordering Information

Part Description	Order Number
73M1903C Evaluation Board with worldwide and 600 Ω termination	73M1903C-EVM

6 Related Documentation

The following 73M1903C documents are available from Teridian Semiconductor Corporation:

73M1903C Data Sheet

7 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73M1903C contact us at:

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For a complete list of worldwide sales offices, go to http://www.teridian.com.

Revision History

Revision	Date	Description
1.0	11/12/2004	First release.
2.0	6/12/2009	Revised in new format.