# Rugged 20Mbps, 8 Channel Multi-Protocol Transceiver with Programmable DCE/DTE and Termination Resistors

## FEATURES

- 20Mbps Differential Transmission Rates
- 15kV ESD Tolerance for Analog I/Os
- Internal Transceiver Termination Resistors for V.11/V.35
- Interface Modes:
  - RS-232 (V.28)
  - X.21 (V.11)
  - RS-449/V.36 (V.10 & V.11)
  - EIA-530 (V.10 & V.11)
  - EIA-530A (V.10 & V.11)
  - V.35
- Software Selectable Protocols with 3-Bit Word
- Eight Drivers and Eight Receivers
- V.35/V.11 Receiver Termination Network Disable Option
- Internal Line or Digital Loopback Testing
- Adheres to NET1/NET2 and TBR-2 Requirements

*Now Available in Lead Free Packaging*

Refer to page 7 for pinout

- Easy Flow-Through Pinout
- +5V Only Operation
- Individual Driver/Receiver Enable/Disable Controls
- Operates in DTE or DCE Mode

## APPLICATIONS

- Router
- Frame Relay
- CSU
- DSU
- PBX
- Secure Communication Terminals

## DESCRIPTION

The SP508 is a monolithic device that supports eight (8) popular serial interface standards for Wide Area Network (WAN) connectivity. The SP508 is fabricated using a low power BiCMOS process technology, and incorporates an Exar regulated charge pump allowing +5V only operation. Exar's patented charge pump provides a regulated output of ±5.8V, which will provide enough voltage for compliant operation in all modes. Eight (8) drivers and eight (8) receivers can be configured via software for any of the above interface modes at any time. The SP508 requires no additional external components for compliant operation for all of the eight (8) modes of operation other than four capacitors used for the internal charge pump. All necessary termination is integrated within the SP508 and is switchable when V.35 drivers and V.35 receivers, or when V.11 receivers are used. The SP508 provides the controls and transceiver availability for operating as either a DTE or DCE.

Additional features with the SP508 include internal loopback that can be initiated in any of the operating modes by use of the $\overline{\text{LOOPBACK}}$ pin. While in loopback mode, receiver outputs are internally connected to driver inputs creating an internal signal path bypassing the serial communications controller for diagnostic testing. The SP508 also includes a latch enable pin with the driver and receiver address decoder. The internal V.11 or V.35 receiver termination can be switched off using a control pin (TERM_OFF) for monitoring applications. All eight (8) drivers and receivers in the SP508 include separate enable pins for added convenience. The SP508 is ideal for WAN serial ports in networking equipment such as routers, access concentrators, network muxes, DSU/CSU's, networking test equipment, and other access devices.

Applicable U.S. Patents-5,306,954; and others patents pending

## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

$V_{CC}$ .....+7V
Input Voltages:
Logic ..... -0.3V to ($V_{CC}$+0.5V)
Drivers..... -0.3V to ($V_{CC}$+0.5V)
Receivers .....±15.5V
Output Voltages:
Logic ..... -0.3V to ($V_{CC}$+0.5V)
Drivers.....±12V
Receivers ..... -0.3V to ($V_{CC}$+0.5V)
Storage Temperature.....-65°C to +150°C
Power Dissipation.....1520mW

(derate 19.0mW/°C above +70°C)

Package Derating:

$ø_{JA}$ .....52.7 °C/W
$ø_{JC}$ .....6.5 °C/W

## STORAGE CONSIDERATIONS

Due to the relatively large package size, storage in a low humidity environment is preferred. Large high density plastic packages are moisture sensitive and should be stored in Dry Vapor Barrier Bags. Prior to usage, the parts should remain bagged and stored below 40°C and 60%RH. If the parts are removed from the bag, they should be used within 48 hours or stored in an environment at or below 20%RH. If the above conditions cannot be followed, the parts should be baked for four hours at 125°C in order to remove moisture prior to soldering. Exar ships the 100-pin LQFP in Dry Vapor Barrier Bags with a humidity indicator card and desiccant pack. The humidity indicator should be below 30%RH.

## ELECTRICAL SPECIFICATIONS

$T_A$ = 0°C to +70°C and $V_{CC}$ = +4.75V to +5.25V unless otherwise noted. The ♦ denotes the specifications which applies to full temperature range of -40°C to =+85°C, unless otherwise specified.

| PARAMETER | MIN. | TYP. | MAX. | UNITS | | CONDITIONS |
|---|---|---|---|---|---|---|
| **LOGIC INPUTS** | | | | | | |
| $V_{IL}$ | | | 0.8 | Volts | ♦ | |
| $V_{IH}$ | 2.0 | | | Volts | ♦ | |
| **LOGIC OUTPUTS** | | | | | | |
| $V_{OL}$ | | | 0.4 | Volts | ♦ | $I_{OUT}$= –3.2mA |
| $V_{OH}$ | | 2.4 | | Volts | ♦ | $I_{OUT}$= 1.0mA |
| **V.28 DRIVER** | | | | | | |
| **DC Parameters** | | | | | | |
| Outputs | | | | | | |
| Open Circuit Voltage | | | ±15 | Volts | ♦ | per Figure 1 |
| Loaded Voltage | ±5.0 | | ±15 | Volts | ♦ | per Figure 2 |
| Short-Circuit Current | | | ±100 | mA | ♦ | per Figure 4, $V_{OUT}$=0V |
| Power-Off Impedance | 300 | | | Ω | ♦ | per Figure 5 |
| **AC Parameters** | | | | | | **$V_{cc}$ = +5V for AC parameters** |
| Outputs | | | | | | |
| Transition Time | | | 1.5 | µs | ♦ | per Figure 6; +3V to -3V |
| Instantaneous Slew Rate | | | 30 | V/µs | | per Figure 3 |
| Propagation Delay | | | | | | |
| $t_{PHL}$ | 0.5 | 1 | 5 | µs | ♦ | |
| $t_{PLH}$ | 0.5 | 1 | 5 | µs | ♦ | |
| Max.Transmission Rate | 120 | 230 | | kbps | ♦ | |
| **V.28 RECEIVER** | | | | | | |
| **DC Parameters** | | | | | | |
| Inputs | | | | | | |
| Input Impedance | 3 | | 7 | kΩ | ♦ | per Figure 7 |
| Open-Circuit Bias | | | +2.0 | Volts | ♦ | per Figure 8 |
| HIGH Threshold | | 1.7 | 3.0 | Volts | ♦ | |
| LOW Threshold | 0.8 | 1.2 | | Volts | ♦ | |
| **AC Parameters** | | | | | | **$V_{cc}$ = +5V for AC parameters** |
| Propagation Delay | | | | | | |
| $t_{PHL}$ | 50 | 100 | 500 | ns | ♦ | |
| $t_{PLH}$ | 50 | 100 | 500 | ns | ♦ | |

$T_A$ = 0°C to +70°C and $V_{CC}$ = +4.75V to +5.25V unless otherwise noted. The ♦ denotes the specifications which applies to full temperature range of -40°C to =+85°C, unless otherwise specified.

| PARAMETER | MIN. | TYP. | MAX. | UNITS | | CONDITIONS |
|---|---|---|---|---|---|---|
| **V.28 RECEIVER (cont)** | | | | | | |
| **AC Parameters (cont.)** | | | | | | |
| Max.Transmission Rate | 120 | 235 | | kbps | | |
| **V.10 DRIVER** | | | | | | |
| **DC Parameters** | | | | | | |
| Outputs | | | | | | |
| Open Circuit Voltage | ±4.0 | | ±6.0 | Volts | ♦ | per Figure 9 |
| Test-Terminated Voltage | $0.9V_{OC}$ | | | Volts | ♦ | per Figure 10 |
| Short-Circuit Current | | | ±150 | mA | ♦ | per Figure 11 |
| Power-Off Current | | | ±100 | µA | ♦ | per Figure 12 |
| **AC Parameters** | | | | | | **$V_{cc}$ = +5V for AC parameters** |
| Outputs | | | | | | |
| Transition Time | | | 200 | ns | ♦ | per Figure 13; 10% to 90% |
| Propagation Delay | | | | | | |
| $t_{PHL}$ | 30 | 100 | 500 | ns | ♦ | |
| $t_{PLH}$ | 30 | 100 | 500 | ns | ♦ | |
| Max.Transmission Rate | 120 | | | kbps | ♦ | |
| **V.10 RECEIVER** | | | | | | |
| **DC Parameters** | | | | | | |
| Inputs | | | | | | |
| Input Current | –3.25 | | +3.25 | mA | ♦ | per Figures 14 and 15 |
| Input Impedance | 4 | | | kΩ | ♦ | |
| Sensitivity | | | ±0.3 | Volts | ♦ | |
| **AC Parameters** | | | | | | **$V_{cc}$ = +5V for AC parameters** |
| Propagation Delay | | | | | | |
| $t_{PHL}$ | | | 60 | ns | ♦ | |
| $t_{PLH}$ | | | 60 | ns | ♦ | |
| Max.Transmission Rate | 120 | | | kbps | ♦ | |
| **V.11 DRIVER** | | | | | | |
| **DC Parameters** | | | | | | |
| Outputs | | | | | | |
| Open Circuit Voltage | | | ±6.0 | Volts | ♦ | per Figure 16 |
| Test Terminated Voltage | ±2.0 | | | Volts | ♦ | per Figure 17 |
| | $0.5V_{OC}$ | | $0.67V_{OC}$ | Volts | ♦ | |
| Balance | | | ±0.4 | Volts | ♦ | per Figure 17 |
| Offset | | | +3.0 | Volts | ♦ | per Figure 17 |
| Short-Circuit Current | | | ±150 | mA | ♦ | per Figure 18 |
| Power-Off Current | | | ±100 | µA | ♦ | per Figure 19 |
| **AC Parameters** | | | | | | **$V_{cc}$ = +5V for AC parameters** |
| Outputs | | | | | | |
| Transition Time | | | 10 | ns | ♦ | per Fig. 21 and 36; 10% to 90% |
| Propagation Delay | | | | | | Using $C_L$ = 50pF; |
| $t_{PHL}$ | | 30 | 85 | ns | ♦ | per Figures 33 and 36 |
| $t_{PLH}$ | | 30 | 85 | ns | ♦ | per Figures 33 and 36 |
| Differential Skew ($\|t_{phl} - t_{plh}\|$) | | 5 | 10 | ns | ♦ | per Figures 33 and 36 |
| Max.Transmission Rate | 20 | | | Mbps | ♦ | |
| Channel to Channel Skew | | 2 | | ns | | |
| **V.11 RECEIVER** | | | | | | |
| **DC Parameters** | | | | | | |
| Inputs | | | | | | |
| Common Mode Range | –7 | | +7 | Volts | ♦ | |
| Sensitivity | | | ±0.2 | Volts | ♦ | |

## ELECTRICAL SPECIFICATIONS

$T_A$ = 0°C to +70°C and $V_{CC}$ = +4.75V to +5.25V unless otherwise noted. The ♦ denotes the specifications which applies to full temperature range of -40°C to =+85°C, unless otherwise specified.

| PARAMETER | MIN. | TYP. | MAX. | UNITS | | CONDITIONS |
|---|---|---|---|---|---|---|
| **V.11 RECEIVER (cont)** | | | | | | |
| **DC Parameters (cont.)** | | | | | | |
| Input Current | –3.25 | | ±3.25 | mA | ♦ | per Figure 20 and 22; power on or off |
| Current w/ 100Ω Termination | | | ±60.75 | mA | ♦ | per Figure 23 and 24 |
| Input Impedance | 4 | | | kΩ | ♦ | |
| **AC Parameters** | | | | | | **$V_{cc}$ = +5V for AC parameters** |
| Propagation Delay | | | | | | Using $C_L$ = 50pF; |
| $t_{PHL}$ | | 30 | 85 | ns | ♦ | per Figures 33 and 38 |
| $t_{PLH}$ | | 30 | 85 | ns | ♦ | per Figures 33 and 38 |
| Skew($\lvert t_{phl}-t_{plh}\rvert$) | | 5 | 10 | ns | ♦ | per Figure 33 |
| Max.Transmission Rate | 20 | | | Mbps | ♦ | |
| Channel to Channel Skew | | 2 | | ns | | |
| **V.35 DRIVER** | | | | | | |
| **DC Parameters** | | | | | | |
| Outputs | | | | | | |
| Test Terminated Voltage | ±0.44 | | ±0.66 | Volts | | per Figure 25 |
| Offset | | | ±0.6 | Volts | ♦ | per Figure 25 |
| Output Overshoot | -0.2$V_{ST}$ | | +0.2$V_{ST}$ | Volts | ♦ | per Figure 25; $V_{ST}$ = Steady state value |
| Source Impedance | 50 | | 150 | Ω | ♦ | per Figure 27; $Z_S = V_2/V_1$ x 50 |
| Short-Circuit Impedance | 135 | | 165 | Ω | ♦ | per Figure 28 |
| **AC Parameters** | | | | | | **$V_{cc}$ = +5V for AC parameters** |
| Outputs | | | | | | |
| Transition Time | | 7 | 20 | ns | ♦ | per Figure 29; 10% to 90% |
| Propagation Delay | | | | | | |
| $t_{PHL}$ | | 30 | 85 | ns | ♦ | per Figure 33 and 36; $C_L$ = 20pF |
| $t_{PLH}$ | | 30 | 85 | ns | ♦ | per Figure 33 and 36; $C_L$ = 20pF |
| Differential Skew ($\lvert t_{phl}-t_{plh}\rvert$) | | 5 | 10 | ns | ♦ | per Figure 33 and 36; $C_L$ = 20pF |
| Max.Transmission Rate | 20 | | | Mbps | ♦ | |
| Channel to Channel Skew | | 5 | | ns | | |
| **V.35 RECEIVER** | | | | | | |
| **DC Parameters** | | | | | | |
| Inputs | | | | | | |
| Sensitivity | | ±50 | ±200 | mV | ♦ | |
| Source Impedance | 90 | | 110 | Ω | ♦ | per Figure 30; $Z_S = V_2/V_1$ x 50Ω |
| Short-Circuit Impedance | 135 | | 165 | Ω | ♦ | per Figure 31 |
| **AC Parameters** | | | | | | **$V_{cc}$ = +5V for AC parameters** |
| Propagation Delay | | | | | | |
| $t_{PHL}$ | | 30 | 85 | ns | ♦ | per Figure 33 and 38; $C_L$ = 20pF |
| $t_{PLH}$ | | 30 | 85 | ns | ♦ | per Figure 33 and 38; $C_L$ = 20pF |
| Skew($\lvert t_{phl}-t_{plh}\rvert$) | | 5 | 10 | ns | ♦ | per Figure 33; $C_L$ = 20pF |
| Max.Transmission Rate | 20 | | | Mbps | ♦ | |
| Channel to Channel Skew | | 2 | | ns | | |
| **TRANSCEIVER LEAKAGE CURRENT** | | | | | | |
| Driver Output 3-State Current | | 500 | | µA | | per Figure 32; Drivers disabled |
| Rcvr Output 3-State Current | | 1 | 10 | µA | | $T_X$ & $R_X$ disabled, 0.4V - $V_O$ - 2.4V |
| **POWER REQUIREMENTS** | | | | | | |
| $V_{CC}$ | 4.75 | 5.00 | 5.25 | Volts | | |
| $I_{CC}$ (Shutdown Mode) | | 1 | | µA | | All $I_{CC}$ values are with $V_{CC}$ = +5V |
| (V.28/RS-232) | | 95 | | mA | | $f_{IN}$ = 120kbps; Drivers active & loaded |
| (V.11/RS-422) | | 230 | | mA | | $f_{IN}$ = 10Mbps; Drivers active & loaded |
| (EIA-530 & RS-449) | | 270 | | mA | | $f_{IN}$ = 10Mbps; Drivers active & loade |
| (V.35) | | 170 | | mA | | V.35 @ $f_{IN}$ = 10Mbps, V.28 @ 20kbps |
| (EIA-530A) | | 200 | | mA | | $f_{IN}$ = 10Mbps; Drivers active & loaded |

## OTHER AC CHARACTERISTICS

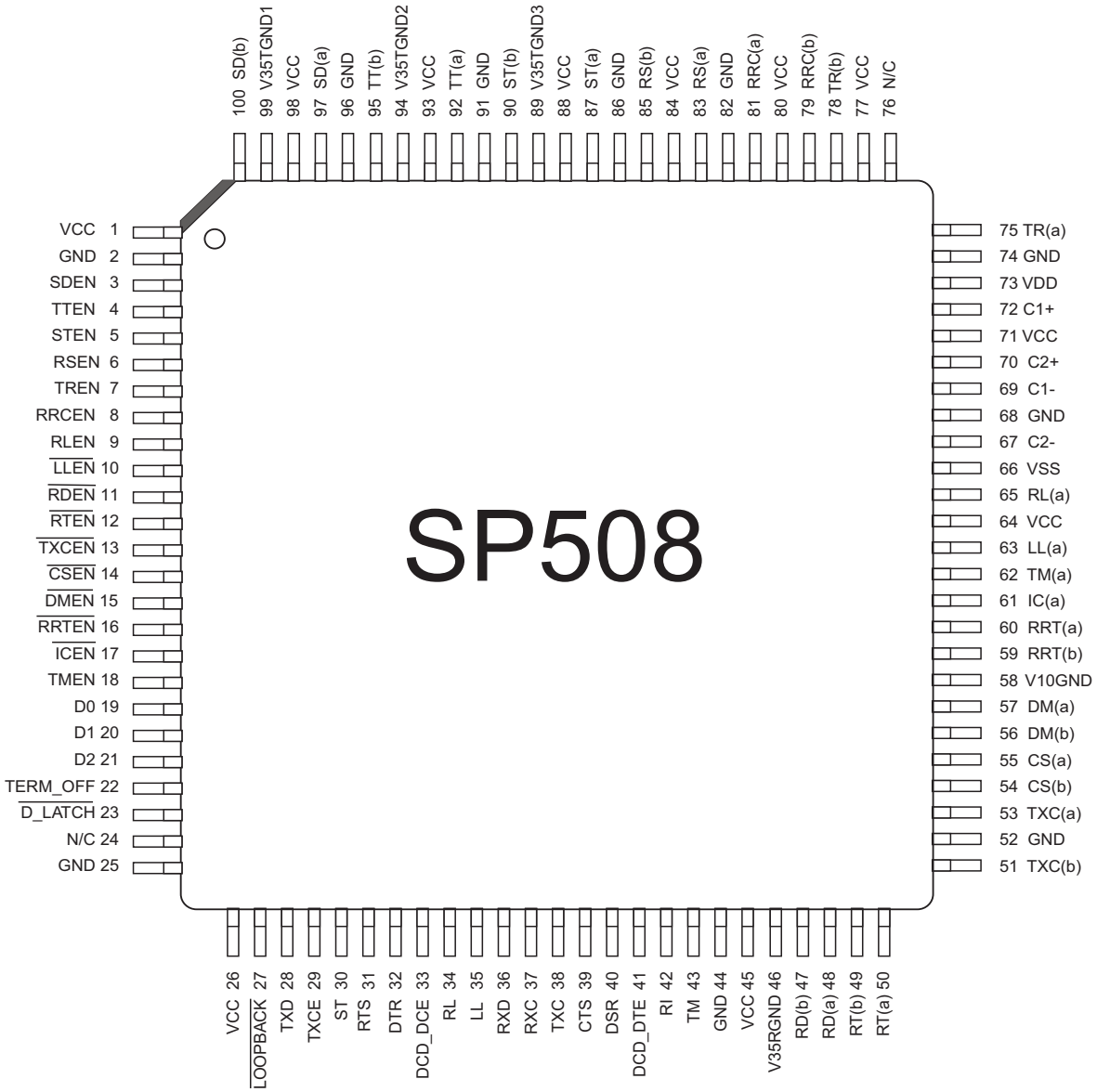
$T_A$ = +25°C and $V_{CC}$ = +5.0V unless otherwise noted.

| PARAMETER | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| **DRIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE** | | | | | |
| **RS-232/V.28** | | | | | |
| $t_{PZL}$; Tri-state to Output LOW | | 0.11 | 5.0 | µs | $C_L$ = 100pF, Fig. 34 & 40; $S_2$ closed |
| $t_{PZH}$; Tri-state to Output HIGH | | 0.11 | 2.0 | µs | $C_L$ = 100pF, Fig. 34 & 40; $S_2$ closed |
| $t_{PLZ}$; Output LOW to Tri-state | | 0.05 | 2.0 | µs | $C_L$ = 100pF, Fig. 34 & 40; $S_2$ closed |
| $t_{PHZ}$; Output HIGH to Tri-state | | 0.05 | 2.0 | µs | $C_L$ = 100pF, Fig. 34 & 40; $S_2$ closed |
| **RS-423/V.10** | | | | | |
| $t_{PZL}$; Tri-state to Output LOW | | 0.07 | 2.0 | µs | $C_L$ = 100pF, Fig. 34 & 40; $S_2$ closed |
| $t_{PZH}$; Tri-state to Output HIGH | | 0.05 | 2.0 | µs | $C_L$ = 100pF, Fig. 34 & 40; $S_2$ closed |
| $t_{PLZ}$; Output LOW to Tri-state | | 0.55 | 2.0 | µs | $C_L$ = 100pF, Fig. 34 & 40; $S_2$ closed |
| $t_{PHZ}$; Output HIGH to Tri-state | | 0.12 | 2.0 | µs | $C_L$ = 100pF, Fig. 34 & 40; $S_2$ closed |
| **RS-422/V.11** | | | | | |
| $t_{PZL}$; Tri-state to Output LOW | | 0.04 | 10.0 | µs | $C_L$ = 100pF, Fig. 34 & 37; $S_1$ closed |
| $t_{PZH}$; Tri-state to Output HIGH | | 0.05 | 2.0 | µs | $C_L$ = 100pF, Fig. 34 & 37; $S_2$ closed |
| $t_{PLZ}$; Output LOW to Tri-state | | 0.03 | 2.0 | µs | $C_L$ = 15pF, Fig. 34 & 37; $S_1$ closed |
| $t_{PHZ}$; Output HIGH to Tri-state | | 0.11 | 2.0 | µs | $C_L$ = 15pF, Fig. 34 & 37; $S_2$ closed |
| **V.35** | | | | | |
| $t_{PZL}$; Tri-state to Output LOW | | 0.85 | 10.0 | µs | $C_L$ = 100pF, Fig. 34 & 37; $S_1$ closed |
| $t_{PZH}$; Tri-state to Output HIGH | | 0.36 | 2.0 | µs | $C_L$ = 100pF, Fig. 34 & 37; $S_2$ closed |
| $t_{PLZ}$; Output LOW to Tri-state | | 0.06 | 2.0 | µs | $C_L$ = 15pF, Fig. 34 & 37; $S_1$ closed |
| $t_{PHZ}$; Output HIGH to Tri-state | | 0.05 | 2.0 | µs | $C_L$ = 15pF, Fig. 34 & 37; $S_2$ closed |
| **RECEIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE** | | | | | |
| **RS-232/V.28** | | | | | |
| $t_{PZL}$; Tri-state to Output LOW | | 0.05 | 2.0 | µs | $C_L$ = 100pF, Fig. 35 & 40; $S_1$ closed |
| $t_{PZH}$; Tri-state to Output HIGH | | 0.05 | 2.0 | µs | $C_L$ = 100pF, Fig. 35 & 40; $S_2$ closed |
| $t_{PLZ}$; Output LOW to Tri-state | | 0.65 | 2.0 | µs | $C_L$ = 100pF, Fig. 35 & 40; $S_1$ closed |
| $t_{PHZ}$; Output HIGH to Tri-state | | 0.65 | 2.0 | µs | $C_L$ = 100pF, Fig. 35 & 40; $S_2$ closed |
| **RS-423/V.10** | | | | | |
| $t_{PZL}$; Tri-state to Output LOW | | 0.04 | 2.0 | µs | $C_L$ = 100pF, Fig. 35 & 40; $S_1$ closed |
| $t_{PZH}$; Tri-state to Output HIGH | | 0.03 | 2.0 | µs | $C_L$ = 100pF, Fig. 35 & 40; $S_2$ closed |
| $t_{PLZ}$; Output LOW to Tri-state | | 0.03 | 2.0 | µs | $C_L$ = 100pF, Fig. 35 & 40; $S_1$ closed |
| $t_{PHZ}$; Output HIGH to Tri-state | | 0.03 | 2.0 | µs | $C_L$ = 100pF, Fig. 35 & 40; $S_2$ closed |

## OTHER AC CHARACTERISTICS (Continued)

$T_A$ = +25°C and $V_{CC}$ = +5.0V unless otherwise noted.

| PARAMETER | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| **RS-422/V.11** | | | | | |
| $t_{PZL}$; Tri-state to Output LOW | | 0.04 | 2.0 | µs | $C_L$ = 100pF, Fig. 35 & 39; $S_1$ closed |
| $t_{PZH}$; Tri-state to Output HIGH | | 0.03 | 2.0 | µs | $C_L$ = 100pF, Fig. 35 & 39; $S_2$ closed |
| $t_{PLZ}$; Output LOW to Tri-state | | 0.03 | 2.0 | µs | $C_L$ = 15pF, Fig. 35 & 39; $S_1$ closed |
| $t_{PHZ}$; Output HIGH to Tri-state | | 0.03 | 2.0 | µs | $C_L$ = 15pF, Fig. 35 & 39; $S_2$ close |
| **V.35** | | | | | |
| $t_{PZL}$; Tri-state to Output LOW | | 0.04 | 2.0 | µs | $C_L$ = 100pF, Fig. 35 & 39; $S_1$ closed |
| $t_{PZH}$; Tri-state to Output HIGH | | 0.03 | 2.0 | µs | $C_L$ = 100pF, Fig. 35 & 39; $S_2$ closed |
| $t_{PLZ}$; Output LOW to Tri-state | | 0.03 | 2.0 | µs | $C_L$ = 15pF, Fig. 35 & 39; $S_1$ closed |
| $t_{PHZ}$; Output HIGH to Tri-state | | 0.03 | 2.0 | µs | $C_L$ = 15pF, Fig. 35 & 39; $S_2$ closed |
| **TRANSCEIVER TO TRANSCEIVER SKEW** | | | (per Figures 32, 33, 36, 38) | | |
| RS-232 Driver | | 100 | | ns | $[ (t_{phl} )_{Tx1} – (t_{phl} )_{Txn} ]$ |
| | | 100 | | ns | $[ (t_{plh} )_{Tx1} – (t_{plh} )_{Txn}]$ |
| RS-232 Receiver | | 20 | | ns | $[ (t_{phl} )_{Rx1} – (t_{phl} )_{Rxn} ]$ |
| | | 20 | | ns | $[ (t_{phl} )_{Rx1} – (t_{phl} )_{Rxn} ]$ |
| RS-422 Driver | | 2 | | ns | $[ (t_{phl} )_{Tx1} – (t_{phl} )_{Txn} ]$ |
| | | 2 | | ns | $[ (t_{plh} )_{Tx1} – (t_{plh} )_{Txn} ]$ |
| RS-422 Receiver | | 2 | | ns | $[ (t_{phl} )_{Rx1} – (t_{phl} )_{Rxn} ]$ |
| | | 3 | | ns | $[ (t_{phl} )_{Rx1} – (t_{phl} )_{Rxn} ]$ |
| RS-423 Driver | | 5 | | ns | $[ (t_{phl} )_{Tx2} – (t_{phl} )_{Txn} ]$ |
| | | 5 | | ns | $[ (t_{plh} )_{Tx2} – (t_{plh} )_{Txn} ]$ |
| RS-423 Receiver | | 5 | | ns | $[ (t_{phl} )_{Rx2} – (t_{phl} )_{Rxn} ]$ |
| | | 5 | | ns | $[ (t_{phl} )_{Rx2} – (t_{phl} )_{Rxn} ]$ |
| V.35 Driver | | 2 | | ns | $[ (t_{phl} )_{Tx1} – (t_{phl} )_{Txn} ]$ |
| | | 2 | | ns | $[ (t_{plh} )_{Tx1} – (t_{plh} )_{Txn} ]$ |
| V.35 Receiver | | 2 | | ns | $[ (t_{phl} )_{Rx1} – (t_{phl} )_{Rxn} ]$ |
| | | 2 | | ns | $[ (t_{phl} )_{Rx1} – (t_{phl} )_{Rxn} ]$ |



| Pin Number | Pin Name | Description | Pin Number | Pin Name | Description |
|---|---|---|---|---|---|
| 1 | VCC | 5V Power Supply Input | 51 | TxC(b) | TxC Non-Inverting Input |
| 2 | GND | Signal Ground | 52 | GND | Signal Ground |
| 3 | SDEN | TxD Driver Enable Input | 53 | TxC(a) | TxC Inverting Input |
| 4 | TTEN | TxCE Driver Enable Input | 54 | CS(b) | CTS Non-Inverting Input |
| 5 | STEN | ST Driver Enable Input | 55 | CS(a) | CTS Inverting Input |
| 6 | RSEN | RTS Driver Enable Input | 56 | DM(b) | DSR Non-Inverting Input |
| 7 | TREN | DTR Driver Enable Input | 57 | DM(a) | DSR Inverting Input |
| 8 | RRCEN | DCD Driver Enable Input | 58 | GNDV10 | V.10 Rx Reference Node |
| 9 | RLEN | RL Driver Enable Input | 59 | RRT(b) | $DCD_{DTE}$ Non-Inverting Input |
| 10 | LLEN# | LL Driver Enable Input | 60 | RRT(a) | $DCD_{DTE}$ Inverting Input |
| 11 | RDEN# | RxD Receiver Enable Input | 61 | IC | RI Receiver Input |
| 12 | RTEN# | RxC Receiver Enable Input | 62 | TM(a) | TM Receiver Input |
| 13 | TxCEN# | TxC Receiver Enable Input | 63 | LL(a) | LL Driver Output |
| 14 | CSEN# | CTS Receiver Enable Input | 64 | VCC | Power Supply Input |
| 15 | DMEN# | DSR Receiver Enable Input | 65 | RL(a) | RL Driver Output |
| 16 | RRTEN# | $DCD_{DTE}$ Receiver Enable Input | 66 | VSS1 | -2xVCC Charge Pump Output |
| 17 | ICEN# | RI Receiver Enable Input | 67 | C2N | Charge Pump Capacitor |
| 18 | TMEN | TM Receiver Enable Input | 68 | GND | Signal Ground |
| 19 | D0 | Mode Select Input | 69 | C1N | Charge Pump Capacitor |
| 20 | D1 | Mode Select Input | 70 | C2P | Charge Pump Capacitor |
| 21 | D2 | Mode Select Input | 71 | VCC | Power Supply Input |
| 22 | TERM_OFF | Termination Disable Input | 72 | C1P | Charge Pump Capacitor |
| 23 | D_LATCH# | Decoder Latch Input | 73 | VDD | 2xVCC Charge Pump Output |
| 24 | NC | No Connect | 74 | GND | Signal Ground |
| 25 | GND | Signal Ground | 75 | TR(a) | DTR Inverting Output |
| 26 | VCC | 5V Power Supply Input | 76 | NC | No Connect |
| 27 | LOOPBACK# | Loopback Mode Enable Input | 77 | VCC | Power Supply Input |
| 28 | TxD | TxD Driver TTL Input | 78 | TR(b) | DTR Non-Inverting Output |
| 29 | TxCE | TxCE Driver TTL Input | 79 | RRC(b) | DCD Non-Inverting Output |
| 30 | ST | ST Driver TTL Input | 80 | VCC | Power Supply Input |
| 31 | RTS | RTS Driver TTL Input | 81 | RRC(a) | DCD Inverting Output |
| 32 | DTR | DTR Driver TTL Input | 82 | GND | Signal Ground |
| 33 | DCD_DCE | $DCD_{DCE}$ Driver TTL Input | 83 | RS(a) | RTS Inverting Output |
| 34 | RL | RL Driver TTL Input | 84 | VCC | Power Supply Input |
| 35 | LL | LL Driver TTL Input | 85 | RS(b) | RTS Non-Inverting Output |
| 36 | RxD | RxD Receiver TTL Output | 86 | GND | Signal Ground |
| 37 | RxC | RxC Receiver TTLOutput | 87 | ST(a) | ST Inverting Output |
| 38 | TxC | TxC Receiver TTL Output | 88 | VCC | Power Supply Input |
| 39 | CTS | CTS Receiver TTL Output | 89 | V35TGND3 | ST Termination Referance |
| 40 | DSR | DSR Receiver TTL Output | 90 | ST(b) | ST Non-Inverting Output |
| 41 | DCD_DTE | $DCD_{DTE}$ Receiver TTL Output | 91 | GND | Signal Ground |
| 42 | RI | RI Receiver TTL Output | 92 | TT(a) | TxCE Inverting Output |
| 43 | TM | TM Receiver TTL Output | 93 | VCC | 5V Power Supply Input |
| 44 | GND | Signal Ground | 94 | V35TGND2 | ST Termination Referance |
| 45 | VCC | Power Supply Input | 95 | TT(b) | TxCE Non-Inverting Output |
| 46 | V35RGND | Reciever Termination Refrence | 96 | GND | Signal Ground |
| 47 | RD(b) | RXD Non-Inverting Input | 97 | SD(a) | TxD Inverting Output |
| 48 | RD(a) | RXD Inverting Input | 98 | VCC | 5V Power Supply Input |
| 49 | RT(b) | RxC Non-Inverting Input | 99 | V35TGND1 | ST Termination Referance |
| 50 | RT(a) | RxC Inverting Input | 100 | SD(b) | TxD Non-Inverting Output |

# SP508 Driver Table

| Driver Output Pin | V.35 Mode | EIA-530 Mode | RS-232 Mode (V.28) | EIA-530A Mode | RS-449 Mode (V.36) | X.21 Mode (V.11) | Shutdown | Suggested Signal |
|---|---|---|---|---|---|---|---|---|
| MODE (D0, D1, D2) | 001 | 010 | 011 | 100 | 101 | 110 | 111 | |
| $T_1$OUT(a) | V.35 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | TxD(a) |
| $T_1$OUT(b) | V.35 | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | TxD(b) |
| $T_2$OUT(a) | V.35 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | TxCE(a) |
| $T_2$OUT(b) | V.35 | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | TxCE(b) |
| $T_3$OUT(a) | V.35 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | TxC_DCE(a) |
| $T_3$OUT(b) | V.35 | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | TxC_DCE(b) |
| $T_4$OUT(a) | V.28 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | RTS(a) |
| $T_4$OUT(b) | High-Z | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | RTS(b) |
| $T_5$OUT(a) | V.28 | V.11 | V.28 | V.10 | V.11 | V.11 | High-Z | DTR(a) |
| $T_5$OUT(b) | High-Z | V.11 | High-Z | High-Z | V.11 | V.11 | High-Z | DTR(b) |
| $T_6$OUT(a) | V.28 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | DCD_DCE(a) |
| $T_6$OUT(b) | High-Z | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | DCD_DCE(b) |
| $T_7$OUT(a) | V.28 | V.10 | V.28 | V.10 | V.10 | High-Z | High-Z | RL |
| $T_8$OUT(a) | V.28 | V.10 | V.28 | V.10 | V.10 | High-Z | High-Z | LL |

**Table 1. Driver Mode Selection**

# SP508 Receiver Table

| Receiver Input Pin | V.35 Mode | EIA-530 Mode | RS-232 Mode (V.28) | EIA-530A Mode | RS-449 Mode (V.36) | X.21 Mode (V.11) | Shutdown | Suggested Signal |
|---|---|---|---|---|---|---|---|---|
| MODE (D0, D1, D2) | 001 | 010 | 011 | 100 | 101 | 110 | 111 | |
| $R_1$IN(a) | V.35 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | RxD(a) |
| $R_1$IN(b) | V.35 | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | RxD(b) |
| $R_2$IN(a) | V.35 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | RxC(a) |
| $R_2$IN(b) | V.35 | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | RxC(b) |
| $R_3$IN(a) | V.35 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | TxC_DTE(a) |
| $R_3$IN(b) | V.35 | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | TxC_DTE(b) |
| $R_4$IN(a) | V.28 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | CTS(a) |
| $R_4$IN(b) | High-Z | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | CTS(b) |
| $R_5$IN(a) | V.28 | V.11 | V.28 | V.10 | V.11 | V.11 | High-Z | DSR(a) |
| $R_5$IN(b) | High-Z | V.11 | High-Z | High-Z | V.11 | V.11 | High-Z | DSR(b) |
| $R_6$IN(a) | V.28 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | DCD_DTE(a) |
| $R_6$IN(b) | High-Z | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | DCD_DTE(b) |
| $R_7$IN(a) | V.28 | V.10 | V.28 | V.10 | V.10 | High-Z | High-Z | RI |
| $R_8$IN(a) | V.28 | V.10 | V.28 | V.10 | V.10 | High-Z | High-Z | TM |

**Table 2. Receiver Mode Selection**

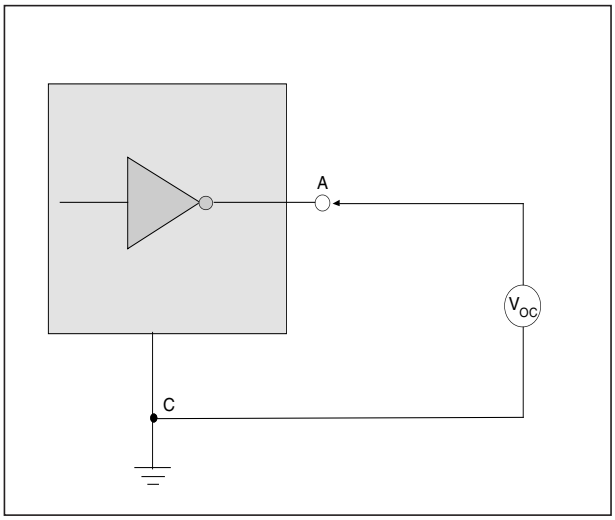



Figure 1. V.28 Driver Output Open Circuit Voltage

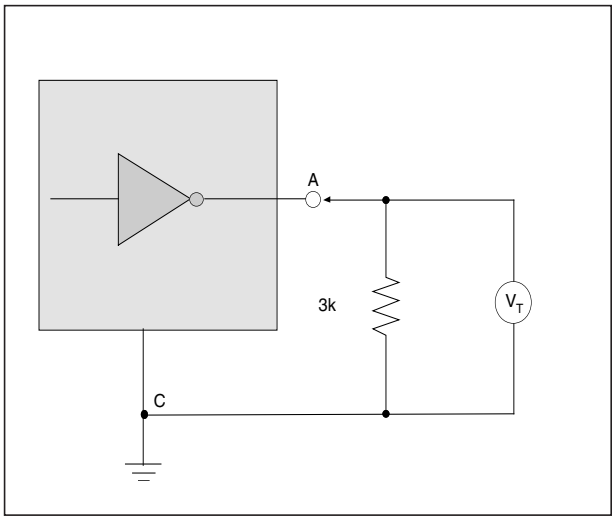



Figure 2. V.28 Driver Output Loaded Voltage

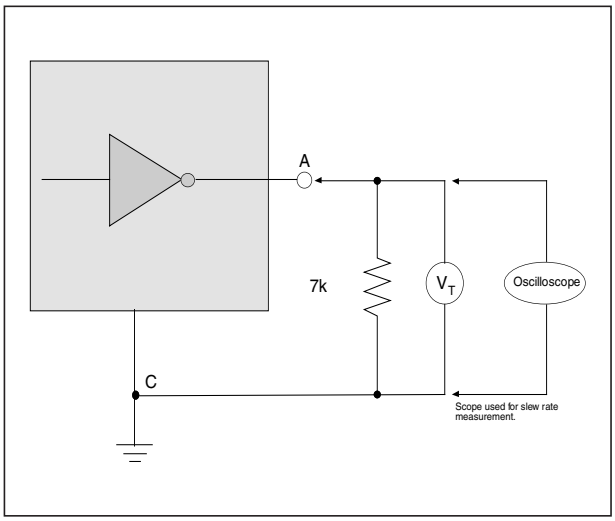



Figure 3. V.28 Driver Output Slew Rate

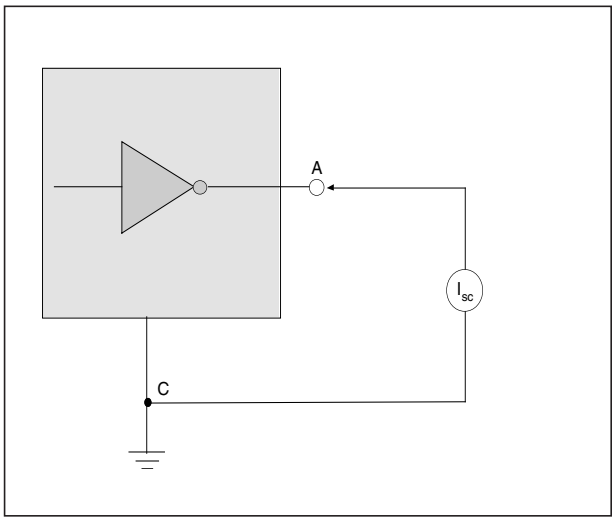



Figure 4. V.28 Driver Output Short-Circuit Current

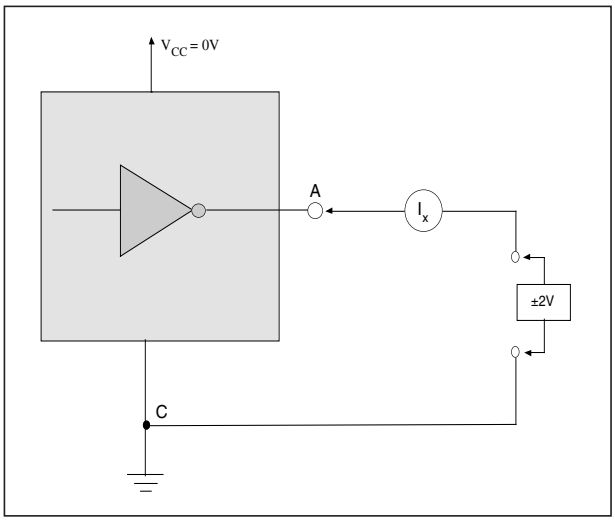



Figure 5. V.28 Driver Output Power-Off Impedance

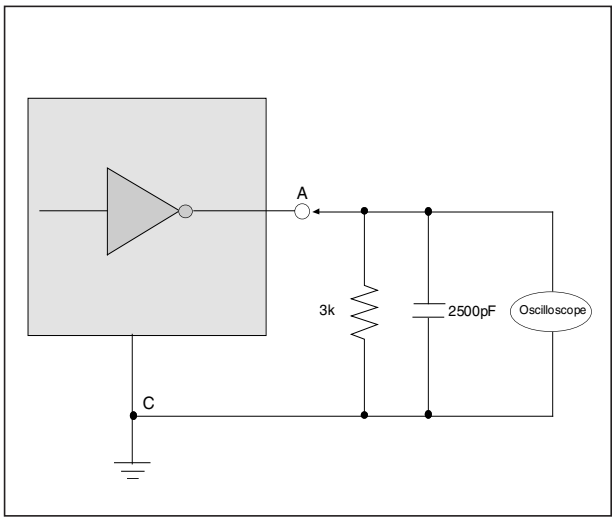



Figure 6. V.28 Driver Output Rise/Fall Times

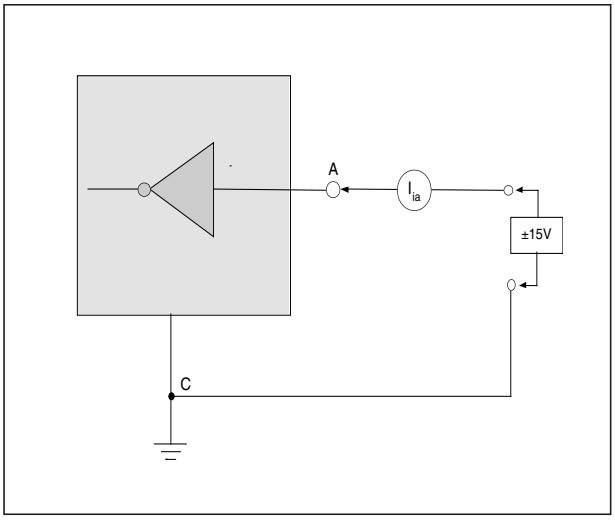



Figure 7. V.28 Receiver Input Impedance

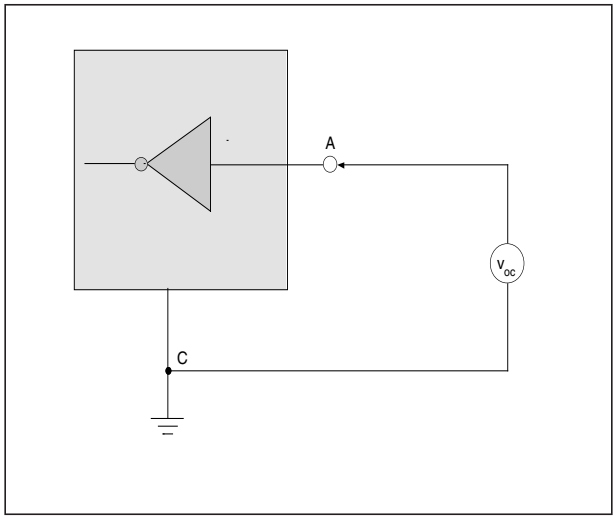



Figure 8. V.28 Receiver Input Open Circuit Bias

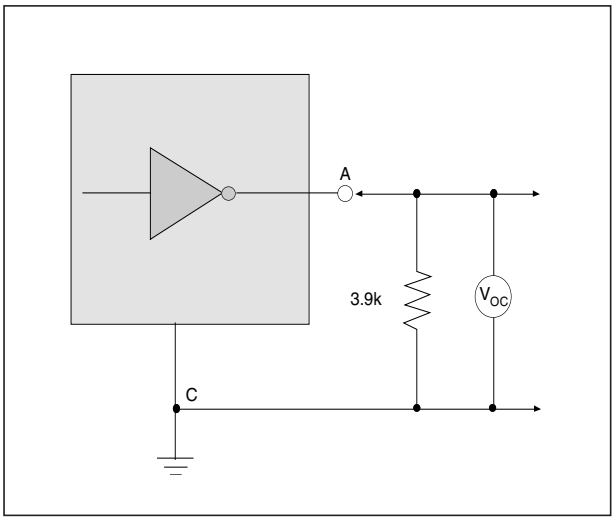



Figure 9. V.10 Driver Output Open-Circuit Voltage

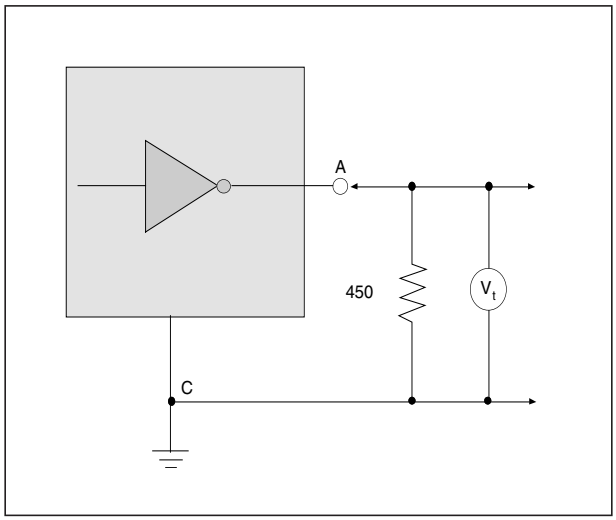



Figure 10. V.10 Driver Output Test Terminated Volt-

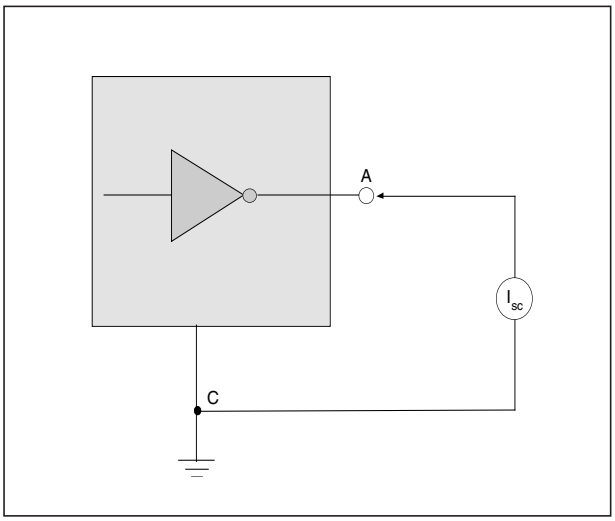



Figure 11. V.10 Driver Output Short-Circuit Current

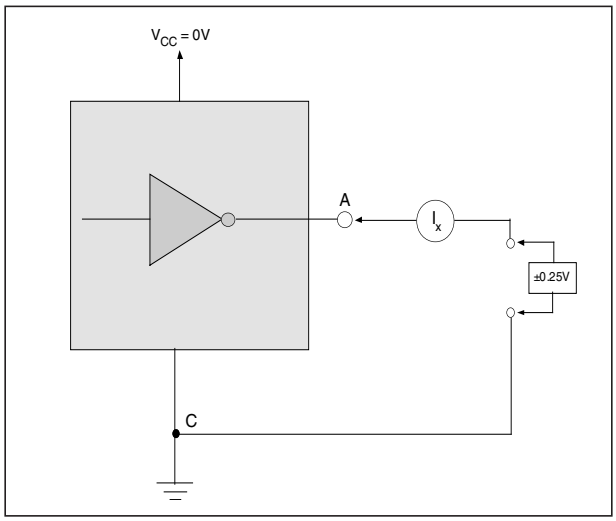



Figure 12. V.10 Driver Output Power-Off Current

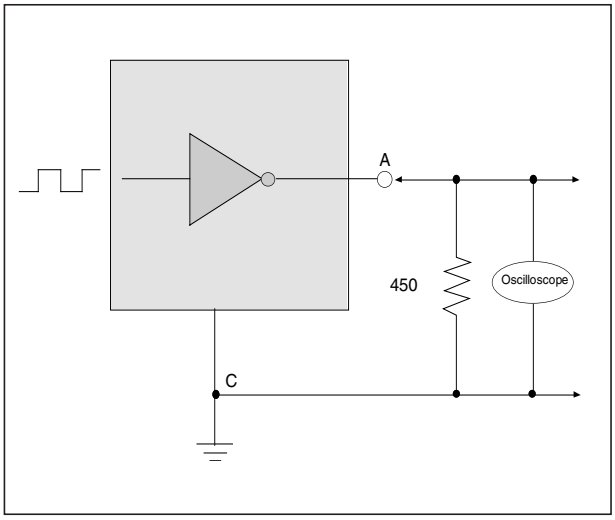



Figure 13. V.10 Driver Output Transition Time

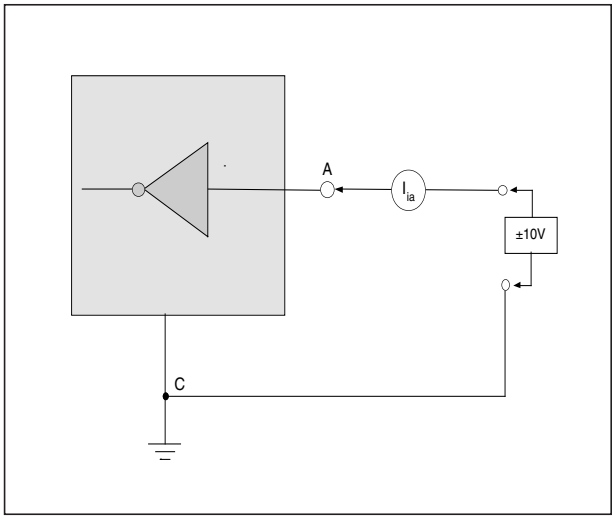



Figure 14. V.10 Receiver Input Current

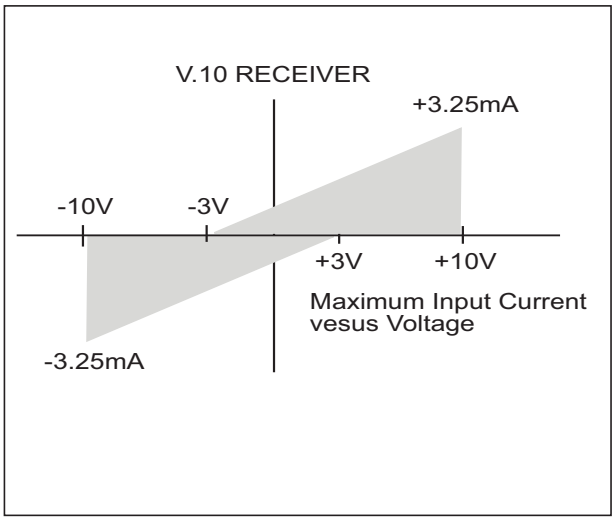



Figure 15. V.10 Receiver Input IV Graph

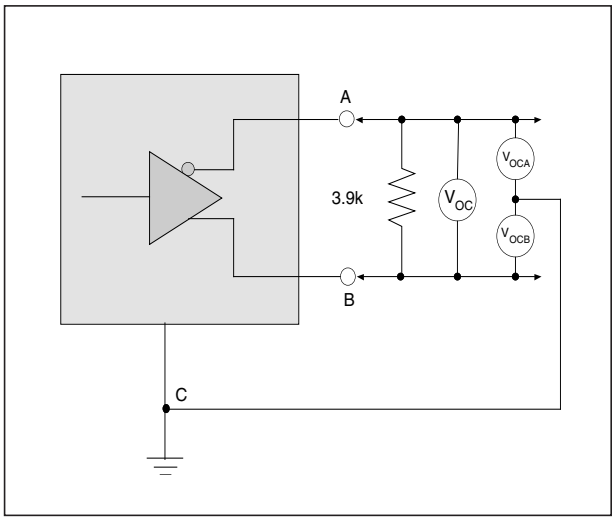



Figure 16. V.11 Driver Output Open-Circuit Voltage

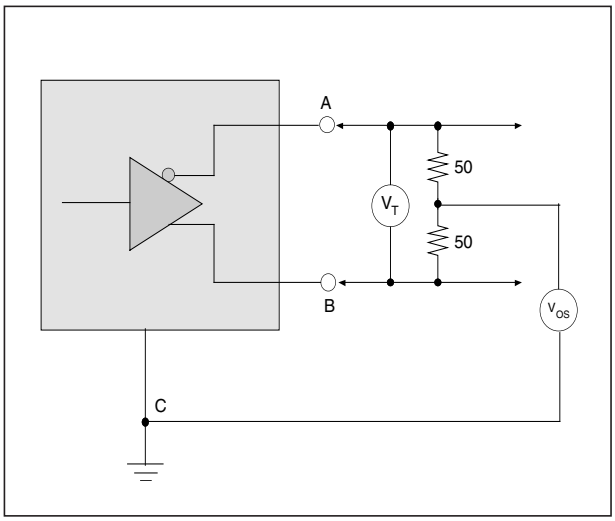



Figure 17. V.11 Driver Output Test Terminated Voltage

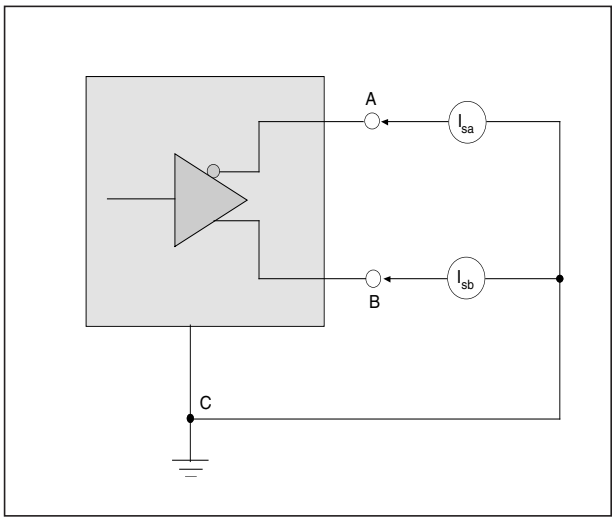



Figure 18. V.11 Driver Output Short-Circuit Current

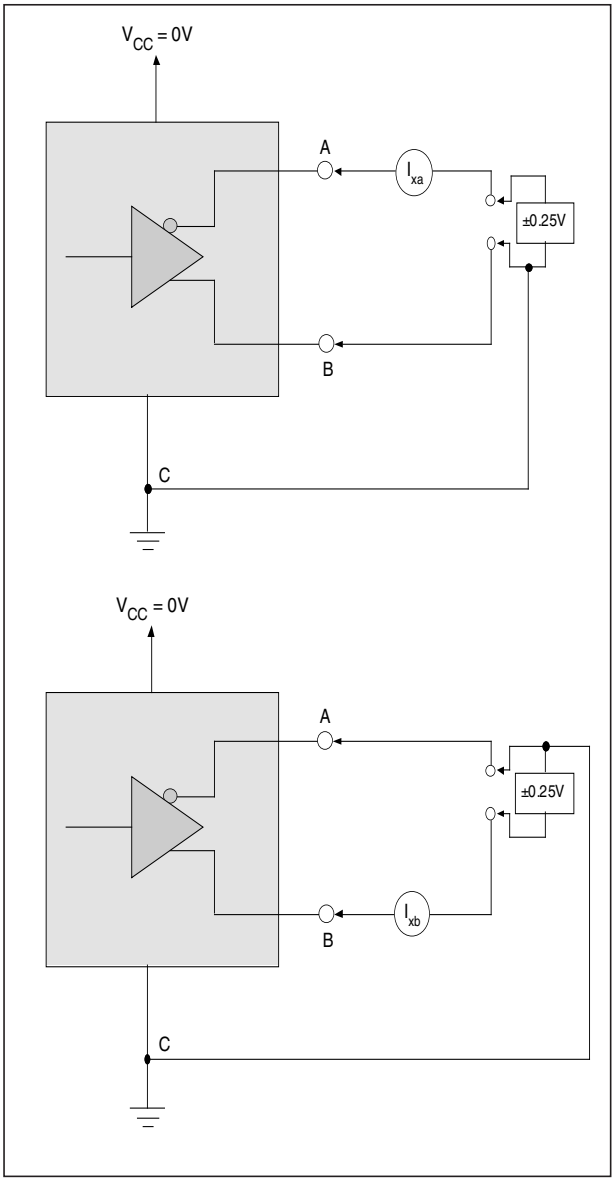



Figure 19. V.11 Driver Output Power-Off Current

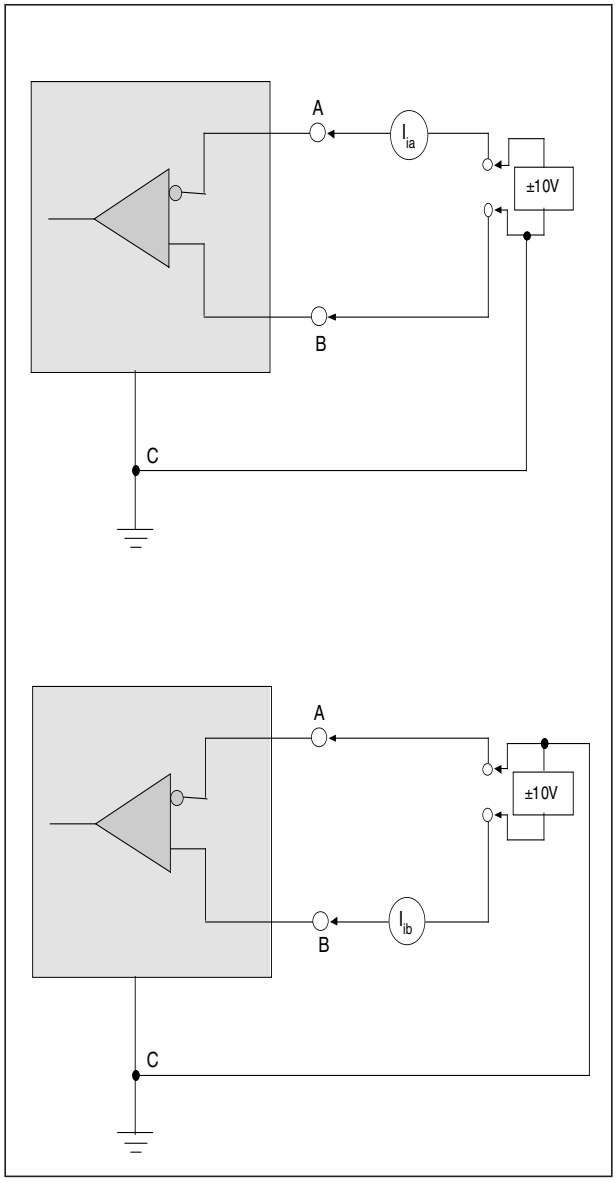



Figure 20. V.11 Receiver Input Current

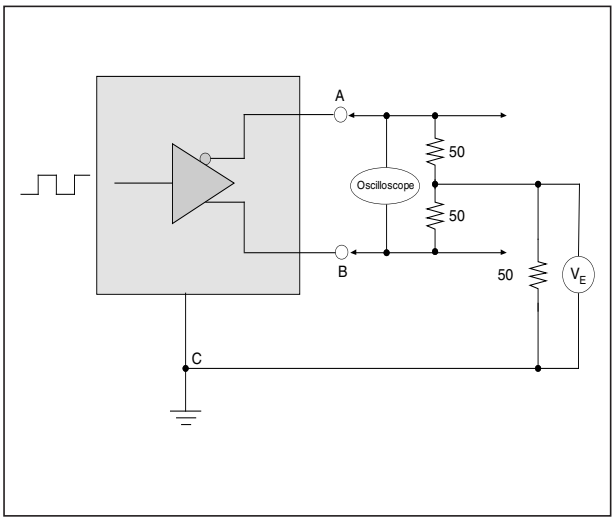



Figure 21. V.11 Driver Output Rise/Fall Time

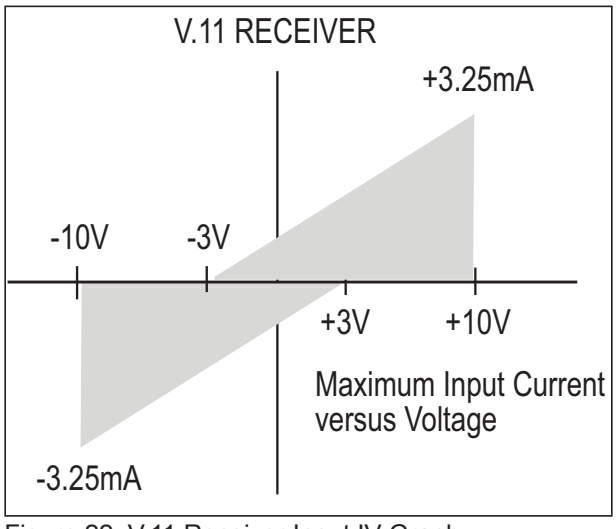



Figure 22. V.11 Receiver Input IV Graph

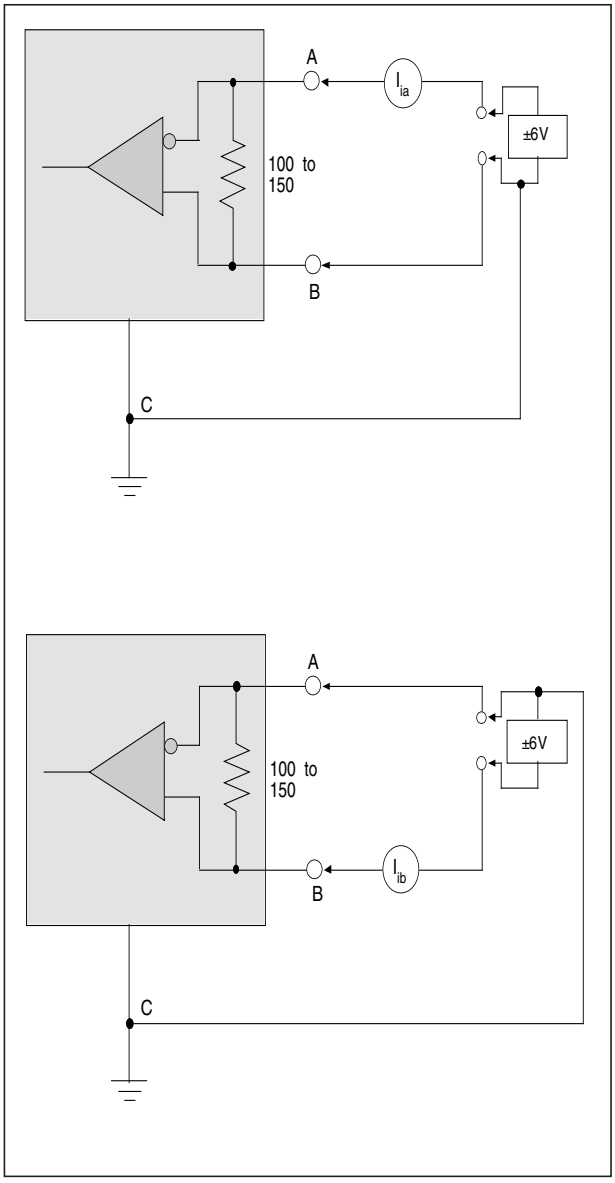



Figure 23. V.11 Receiver Input Current w/ Termination

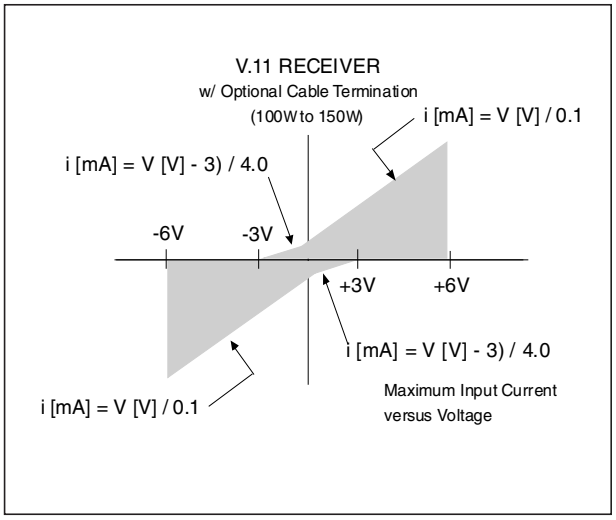



Figure 24. V.11 Receiver Input Graph w/ Termination

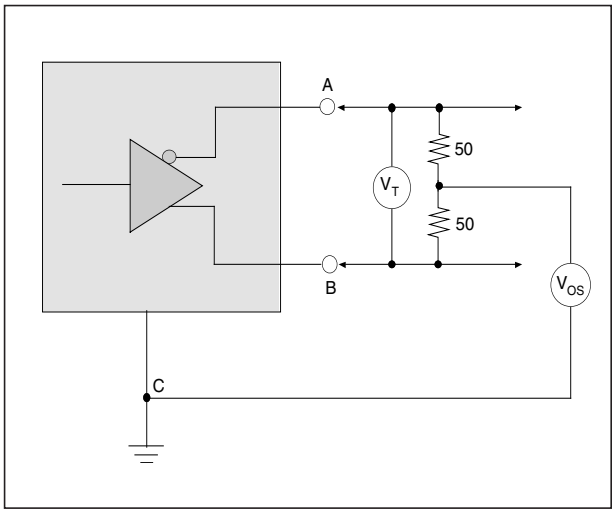



Figure 25. V.35 Driver Output Test Terminated Voltage

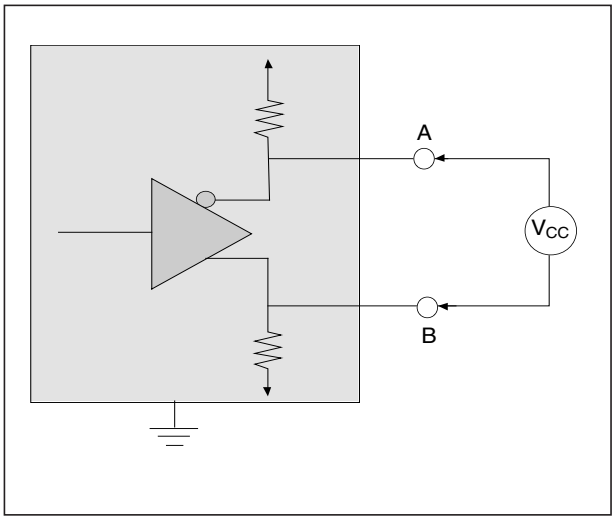



Figure 26. V.35 Driver Output Offset Voltage

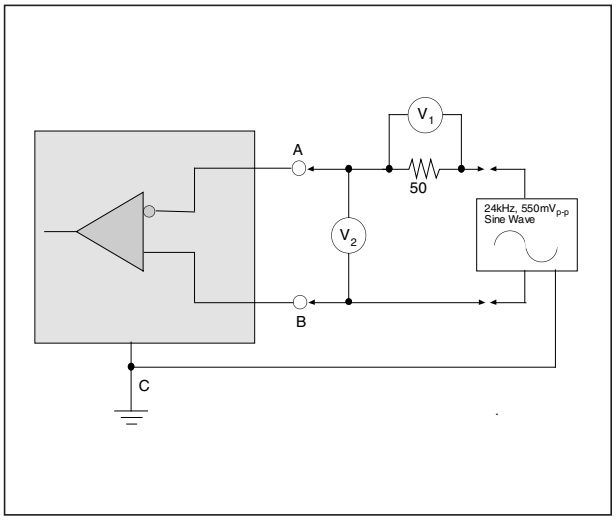



Figure 27. V.35 Driver Output Source Impedance

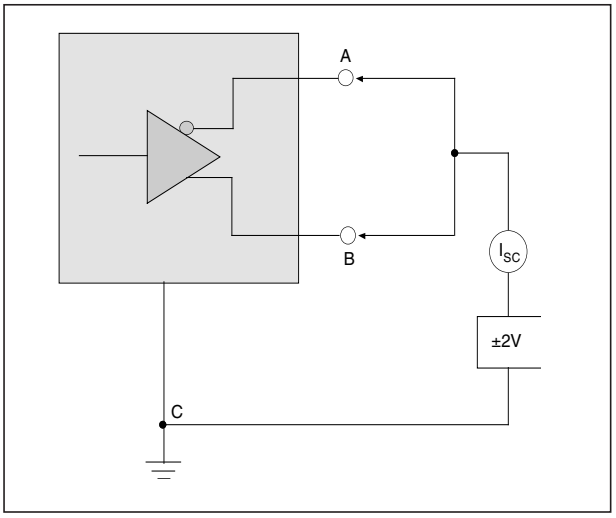



Figure 28. V.35 Driver Output Short-Circuit Impedance

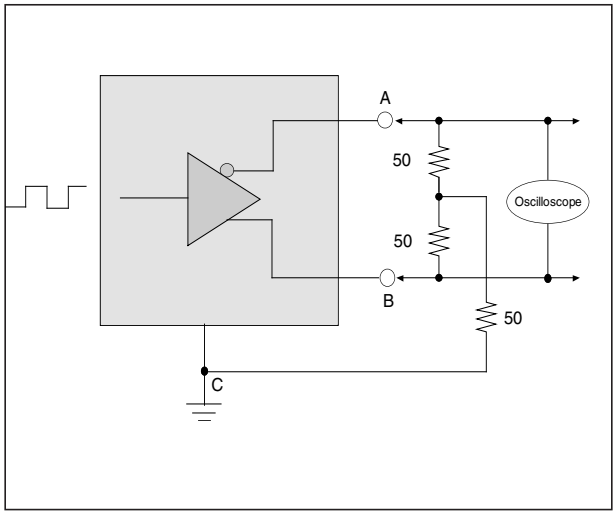



Figure 29. V.35 Driver Output Rise/Fall Time

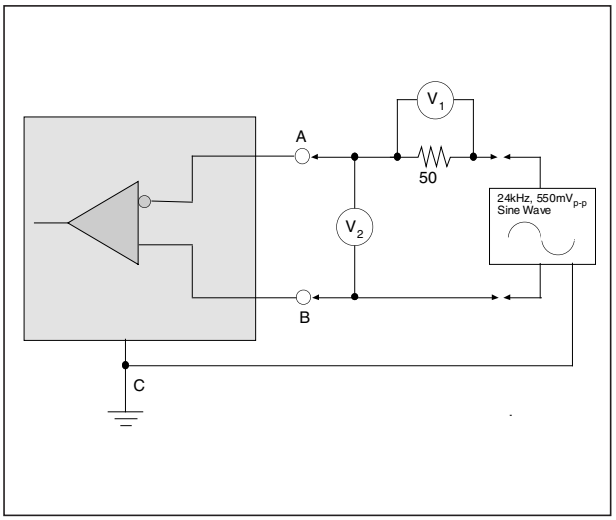



Figure 30. V.35 Receiver Input Source Impedance

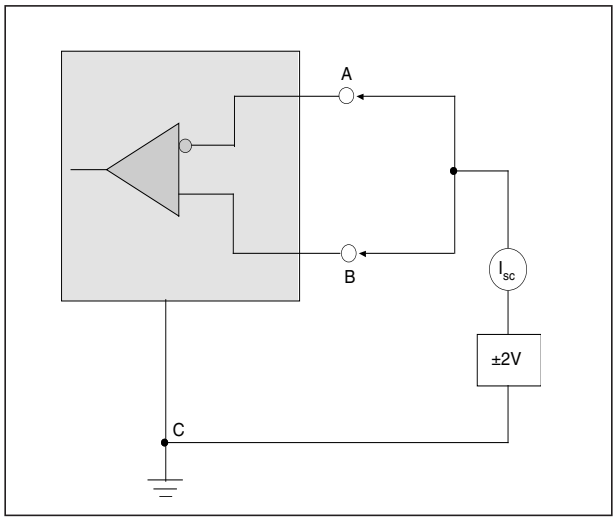



Figure 31. V.35 Receiver Input Short-Circuit Impedance

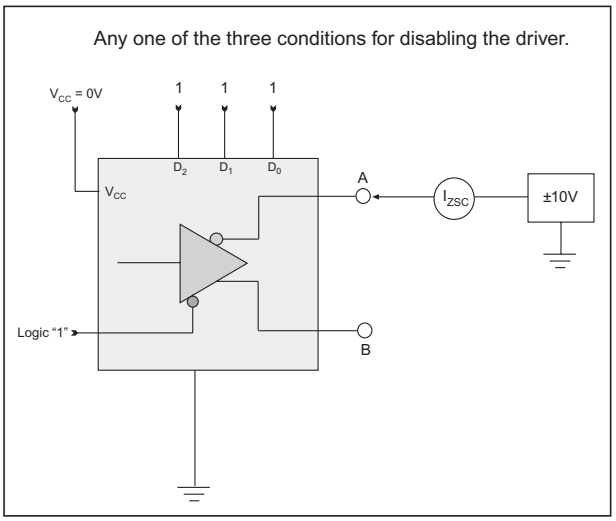



Figure 32. Driver Output Leakage Current Test

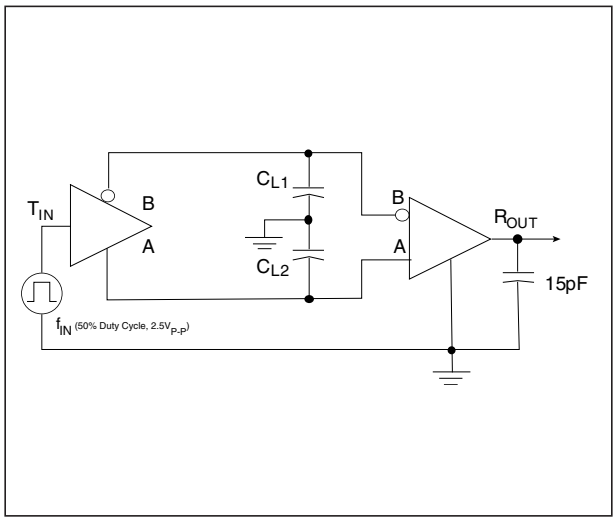



Figure 33. Driver/Receiver Timing Test Circuit

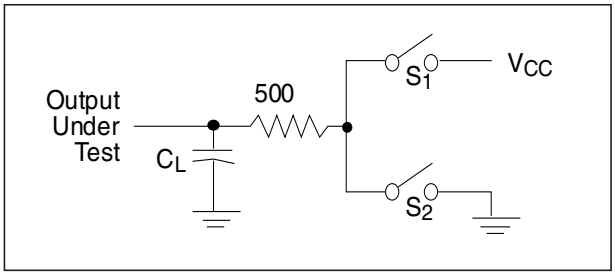



Figure 34. Driver Timing Test Load Circuit

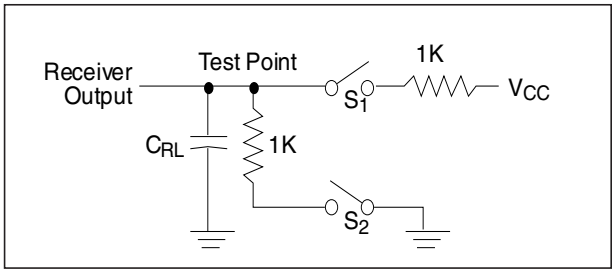



Figure 35. Receiver Timing Test Load Circuit

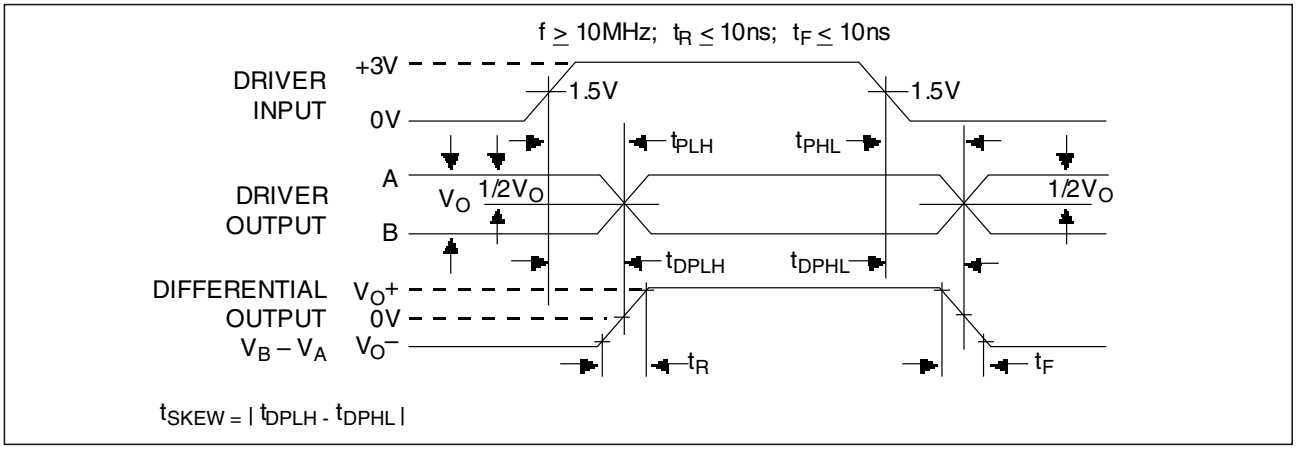



Figure 36. Driver Propagation Delays

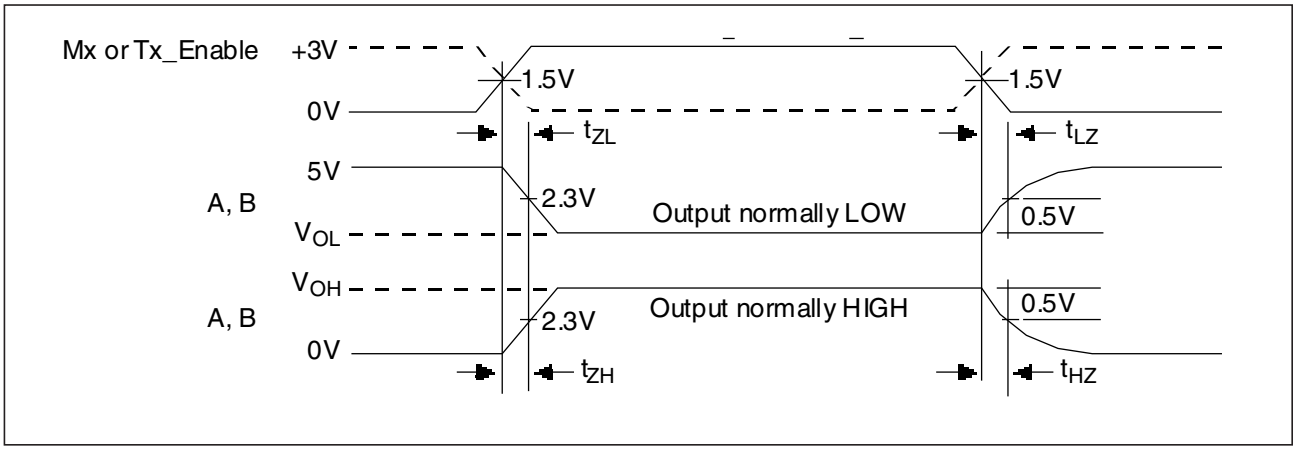



Figure 37. Driver Enable and Disable Times

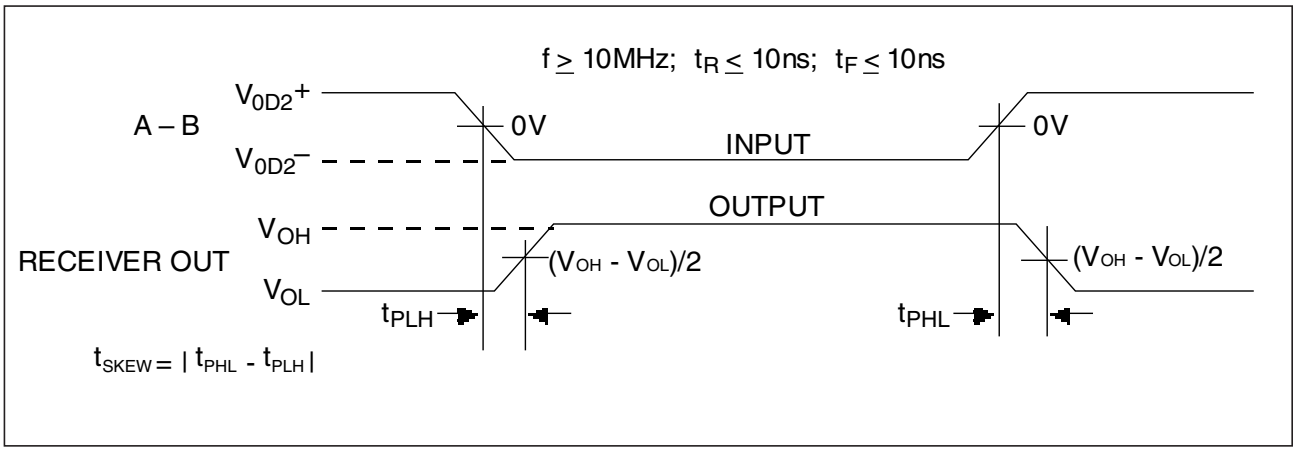



Figure 38. Receiver Propagation Delays

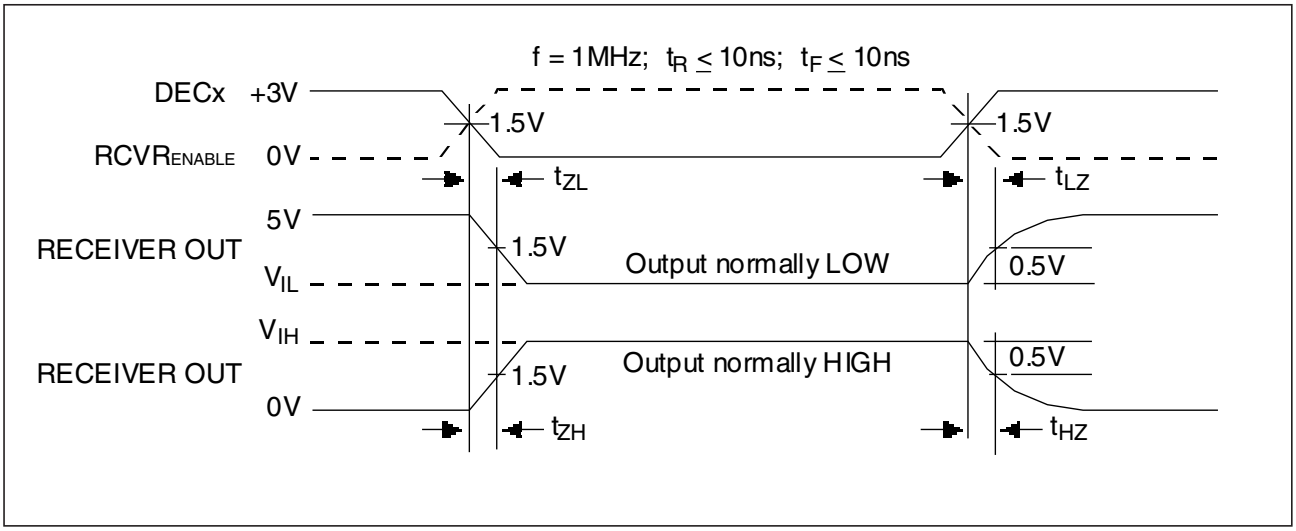



Figure 39. Receiver Enable and Disable Times

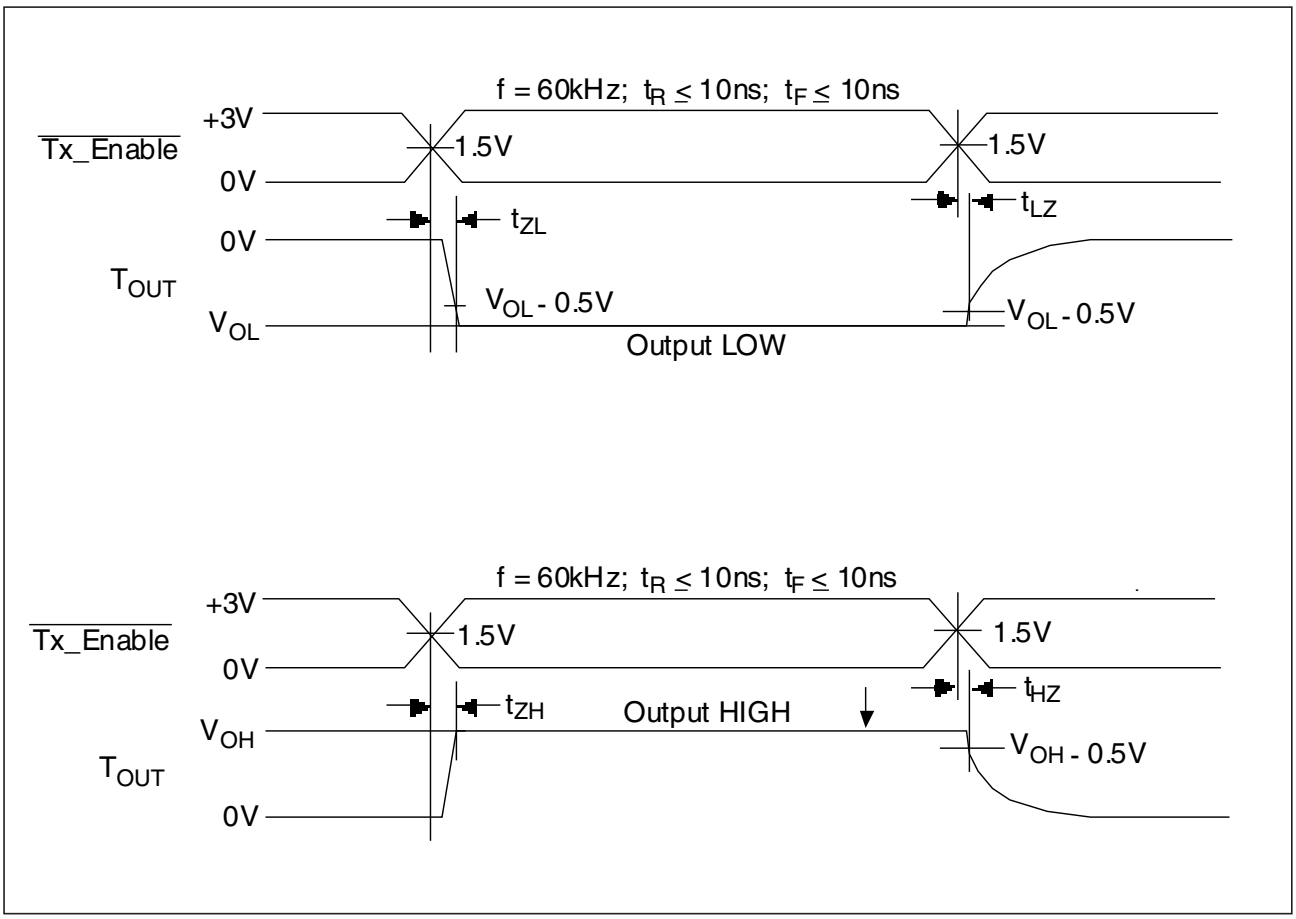



Figure 40. V.28 (RS-232) and V.10 (RS-423) Driver Enable and Disable Times

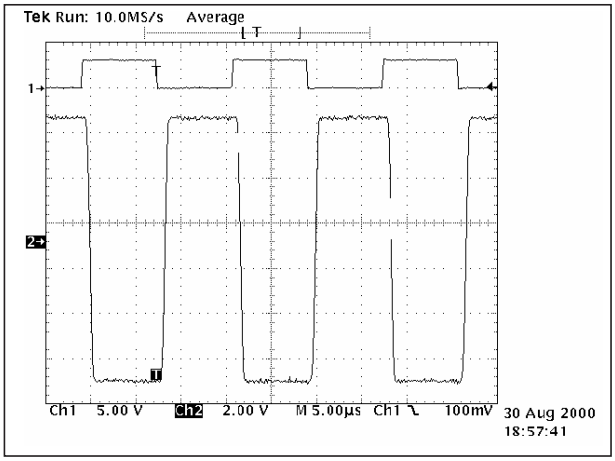



Figure 41. Typical V.28 Driver Output Waveform

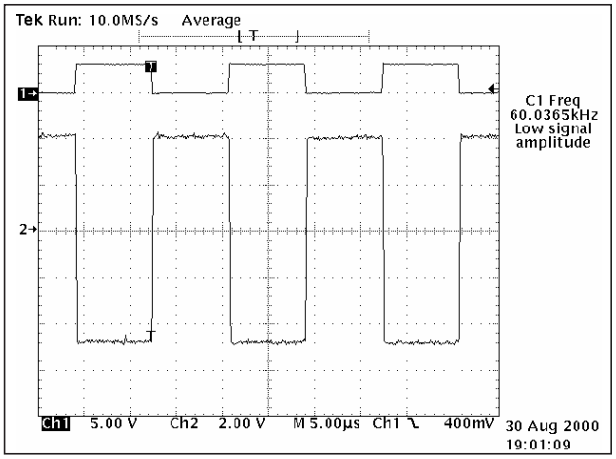



Figure 42. Typical V.10 Driver Output Waveform

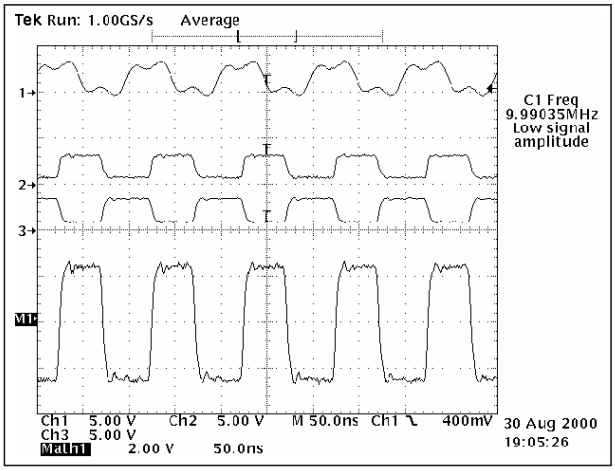



Figure 43. Typical V.11 Driver Output Waveform

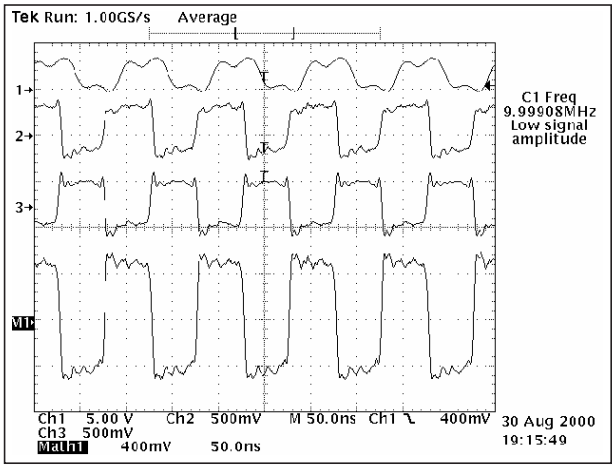



Figure 44. Typical V.35 Driver Output Waveform

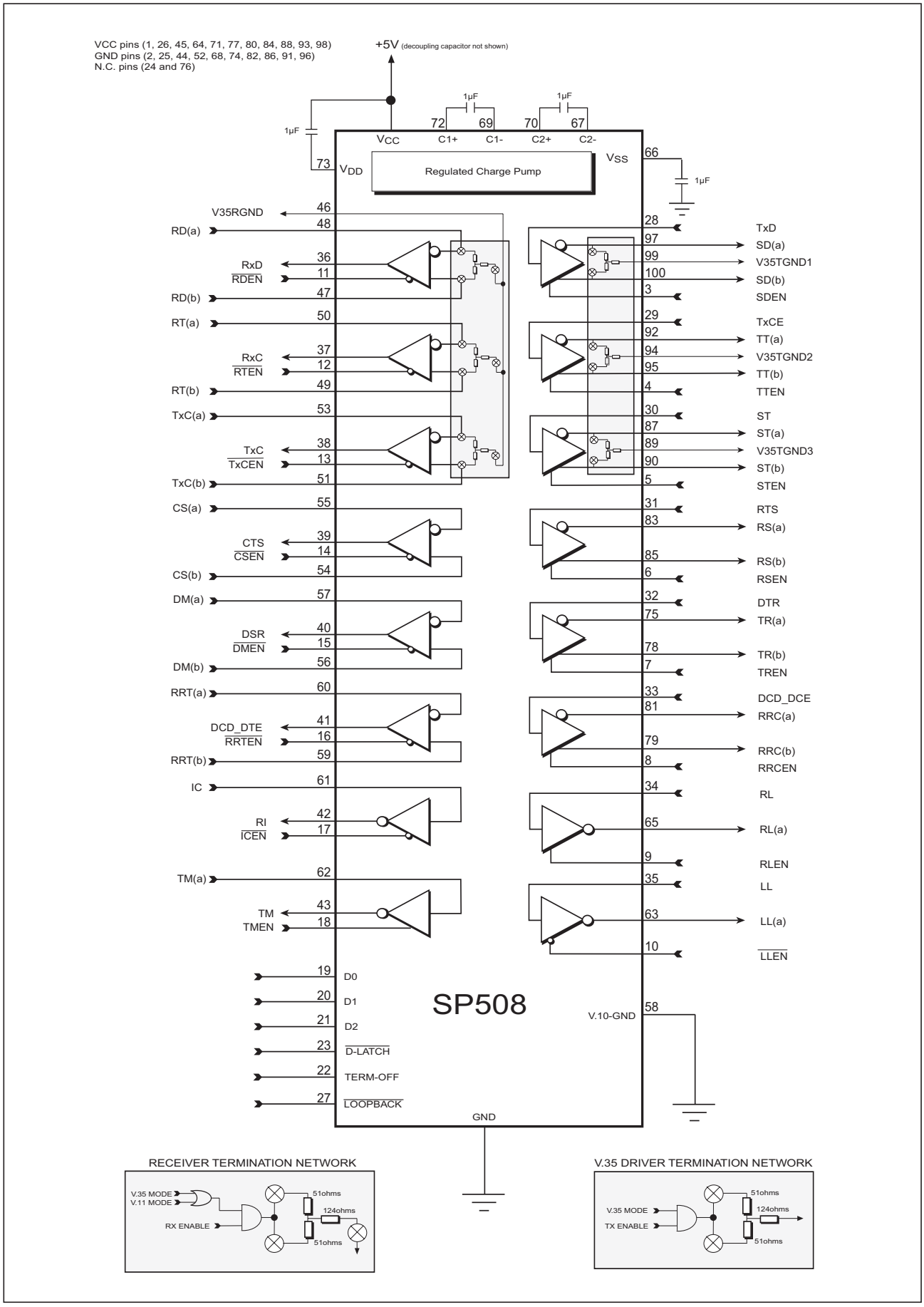



Figure 45. Functional Diagram

The SP508 contains highly integrated serial transceivers that offer programmability between interface modes through software control. The SP508 offers the hardware interface modes for RS-232 (V.28), RS-449/V.36 (V.11 and V.10), EIA-530 (V.11 and V.10), EIA-530A (V.11 and V.10), V.35 (V.35 and V.28) and X.21(V.11). The interface mode selection is done via three control pins, which can be latched via microprocessor control.

The SP508 has eight drivers, eight receivers, and Exar's patented on-board charge pump (5,306,954) that is ideally suited for wide area network connectivity and other multi-protocol applications. Other features include digital and line loopback modes, individual enable/disable control lines for each driver and receiver, fail-safe when inputs are either open or shorted, individual termination resistor ground paths, separate driver and receiver ground outputs, enhanced ESD protection on driver outputs and receiver inputs.

## THEORY OF OPERATION

The SP508 device is made up of 1) the drivers, 2) the receivers, 3) a charge pump, 4) DTE/DCE switching algorithm, and 5) control logic.

### Drivers

The SP508 has eight enhanced independent drivers. Control for the mode selection is done via a three-bit control word into D0, D1, and D2. The drivers are prearranged such that for each mode of operation, the relative position and functionality of the drivers are set up to accommodate the selected interface mode. As the mode of the drivers is changed, the electrical characteristics will change to support the required signal levels. The mode of each driver in the different interface modes that can be selected is shown in Table 1.

There are four basic types of driver circuits – ITU-T-V.28 (RS-232), ITU-T-V.10 (RS-423), ITU-T-V.11 (RS-422), and CCITT-V.35.

The V.28 (RS-232) drivers output single-ended signals with a minimum of ±5V (with 3kΩ & 2500pF loading), and can operate over 120kbps. Since the SP508 uses a charge pump to generate the RS-232 output rails, the driver outputs will never exceed ±10V. The V.28 driver architecture is similar to Exar's standard line of RS-232 transceivers.

The RS-423 (V.10) drivers are also single-ended signals which produce open circuit $V_{OL}$ and $V_{OH}$ measurements of ±4.0V to ±6.0V. When terminated with a 450Ω load to ground, the driver output will not deviate more than 10% of the open circuit value. This is in compliance of the ITU V.10 specification. The V.10 (RS-423) drivers are used in RS-449/V.36, EIA-530, and EIA-530A modes as Category II signals from each of their corresponding specifications. The V.10 drivers are guaranteed to transmit over 120kbps, but can operate at over 1Mbps if necessary.

The third type of drivers are V.11 (RS-422) differential drivers. Due to the nature of differential signaling, the drivers are more immune to noise as opposed to single-ended transmission methods. The advantage is evident over high speeds and long transmission lines. The strength of the driver outputs can produce differential signals that can maintain ±2V differential output levels with a load of 100Ω. The signal levels and drive capability of these drivers allow the drivers to also support RS-485 requirements of ±1.5V differential output levels with a 54Ω load. The strength allows the SP508 differential driver to drive over long cable lengths with minimal signal degradation. The V.11 drivers are used in RS-449, EIA-530, EIA-530A and V.36 modes as Category I signals which are used for clock and data. Exar's new driver design over its predecessors allow the SP508 to operate over 20Mbps for differential transmission.

The fourth type of drivers are V.35 differential drivers. There are only three available on the SP508 for data and clock (TxD, TxCE, and TxC in DCE mode). These drivers are current sources that drive loop current through a differential pair resulting in a 550mV differential voltage at the receiver. These drivers also incorporate fixed termination networks for each driver in order to set the $V_{OH}$ and $V_{OL}$ depending on load conditions. This termination network is basically a "Y" configuration consisting of two 51Ω resistors connected in series and a 124Ω resistor connected between the two 50Ω resistors and a V35TGND output. Each of the three drivers and its associated termination will have its own V35TGND output for grounding convenience. Filtering can be done on these pins to reduce common mode noise transmitted over the transmission line by connecting a capacitor to ground.

The drivers also have separate enable pins which simplifies half-duplex configurations for some applications, especially programmable DTE/DCE. The enable pins will either enable or disable the output of the drivers according to the appropriate active logic illustrated on Figure 45. The enable pins have internal pull-up and pull-down devices, depending on the active polarity of the receiver, that enable the driver upon power-on if the enable lines are left floating. During disabled conditions, the driver outputs will be at a high impedance 3-state.

The driver inputs are both TTL and CMOS compatible. All driver inputs have an internal pull-up resistor so that the output will be at a defined state at logic LOW ("0"). Unused driver inputs can be left floating. The internal pull-up resistor value is approximately 500kΩ.

**Receivers**

The SP508 has eight enhanced independent receivers. Control for the mode selection is done via a three-bit control word that is the same as the driver control word. Therefore, the modes for the drivers and receivers are identical in the application.

Like the drivers, the receivers are prearranged for the specific requirements of the synchronous serial interface. As the operating mode of the receivers is changed, the electrical characteristics will change to support the required serial interface protocols of the receivers. Table 2 shows the mode of each receiver in the different interface modes that can be selected. There are two basic types of receiver circuits—ITU-T-V .28 (RS-232) and ITU-T-V.11, (RS-422).

The RS-232 (V.28) receiver is single-ended and accepts RS-232 signals from the RS-232 driver. The RS-232 receiver has an operating input voltage range of ±15V and can receive signals downs to ±3V. The input sensitivity complies with RS-232 and V .28 at ±3V. The input impedance is 3kΩ to 7kΩ in accordance to RS-232 and V .28. The receiver output produces a TTL/CMOS signal with a +2.4V minimum for a logic "1" and a +0.4V maximum for a logic "0". The RS-232 (V.28) protocol uses these receivers for all data, clock and control signals. They are also used in V.35 mode for control line signals: CTS, DSR, LL, and RL. The RS-232 receivers can operate over 120kbps.

The second type of receiver is a differential type that can be configured internally to support ITU-T-V.10 and CCITT-V.35 depending on its input conditions. This receiver has a typical input impedance of 10kΩ and a differential threshold of less than ±200mV, which complies with the ITU-T-V.11 (RS-422) specifications. V.11 receivers are used in RS-449/V.36, EIA-530, EIA-530A and X.21 as Category I signals for receiving clock, data, and some control line signals not covered by Category II V.10 circuits. The differential V.11 transceiver has improved architecture that allows over 20Mbps transmission rates.

Receivers dedicated for data and clock (RxD, RxC, TxC) incorporate internal termination for V.11. The termination resistor is typically 120Ω connected between the A and B inputs. The termination is essential for minimizing crosstalk and signal reflection over the transmission line . The minimum value is guaranteed to exceed 100Ω, thus complying with the V.11 and RS-422 specifications.

This resistor is invoked when the receiver is operating as a V.11 receiver, in modes EIA-530, EIA-530A, RS-449/V.36, and X.21. The same receivers also incorporate a termination network internally for V.35 applications. For V.35, the receiver input termination is a "Y" termination consisting of two 51Ω resistors connected in series and a 124Ω resistor connected between the two 50Ω resistors and V35RGND output. The V35RGND is usually grounded. The receiver itself is identical to the V.11 receiver.

The differential receivers can be configured to be ITU-T-V.10 single-ended receivers by internally connecting the non-inverting input to ground. This is internally done by default from the decoder. The non-inverting input is rerouted to V10GND and can be grounded separately. The ITU-T-V.10 receivers can operate over 1Mbps and are used in RS-449/V.36, E1A-530, E1A-530A and X.21 modes as Category II signals as indicated by their corresponding specifications. All receivers include an enable/disable line for disabling the receiver output allowing convenient half-duplex configurations. The enable pins will either enable or disable the output of the receivers according to the appropriate active logic illustrated on Figure 45. The receiver's enable lines include an internal pull-up or pull-down device, depending on the active polarity of the receiver, that enables the receiver upon power up if the enable lines are left floating. During disabled conditions, the receiver outputs will be at a high impedance state. If the receiver is disabled any associated termination is also disconnected from the inputs.

All receivers include a fail-safe feature that outputs a logic high when the receiver inputs are open, terminated but open, or shorted together. For single-ended V.28 and V.10 receivers, there are internal 5kΩ pull-down resistors on the inputs which produces a logic high ("1") at the receiver outputs. The differential receivers have a proprietary circuit that detect open or shorted inputs and if so, will produce a logic HIGH ("1") at the receiver output.

## CHARGE PUMP

The charge pump is a Exar-patented design (5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses four-phase voltage shifting technique to attain symmetrical power supplies. The charge pump $V_{DD}$ and $V_{SS}$ outputs are regulated to +5.8V and -5.8V, respectively. There is a free-running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

### Phase 1

__$V_{SS}$ charge storage ——During this phase of the clock cycle, the positive side of capacitors $C_1$ and $C_2$ are initially charged to $V_{CC}$. C+ is then switched to ground and the charge in $C_1$- is transferred to $C_2$-. Since $C_2$+ is connected to $V_{CC}$, the voltage potential across capacitor $C_2$ is now $2_XV_{CC}$.

### Phase 2

—$V_{SS}$ transfer —Phase two of the clock connects the negative terminal of $C_2$ to the $V_{SS}$ storage capacitor and the positive terminal of $C_2$ to ground, and transfers the negative generated voltage to $C_3$. This generated voltage is regulated to –5.8V. Simultaneously, the positive side of the capacitor $C_1$ is switched to $V_{CC}$ and the negative side is connected to ground.

### Phase 3

—$V_{DD}$ charge storage —The third phase of the clock is identical to the first phase—the charge transferred in $C_1$ produces $–V_{CC}$ in the negative terminal of $C_1$ which is applied to the negative side of the capacitor $C_2$ . Since $C_2$+ is at $V_{CC}$, the voltage potential across $C_2$ is $2_XV_{CC}$.

### Phase 4

—$V_{DD}$ transfer —The fourth phase of the clock connects the negative terminal of $C_2$ to ground, and transfers the generated 5.8V across $C_2$ to $C_4$, the $V_{DD}$ storage capacitor. This voltage is regulated to +5.8V. At the regulated voltage, the internal oscillator is disabled and simultaneously with this, the positive side of capacitor $C_1$ is switched to $V_{CC}$ and the negative side is connected to ground, and the cycle begins again.

The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both $V^+$ and $V^-$ are separately generated from $V_{CC}$; in a no-load condition $V^+$ and $V^-$ will be symmetrical. Older charge pump approaches that generate $V^-$ from $V^+$ will show a decrease in the magnitude of $V^-$ compared to $V^+$ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 250kHz. The external capacitors can be as low as 1µF with a 16V breakdown voltage rating.

## TERM_OFF FUNCTION

The SP508 contains a TERM_OFF pin that disables all three receiver input termination networks regardless of mode. This allows the device to be used in monitor mode applications that are typically found in networking test equipment. The TERM_OFF pin internally contains a pull-down device with an impedance of over 500kΩ, which will default in a "ON" condition during power-up if V.35 receivers are used. The individual receiver enable line and the SHUTDOWN mode from the decoder will disable the termination regardless of TERM_OFF.

## LOOPBACK FUNCTION

The SP508 contains a LOOPBACK pin that invokes a loopback path. This loopback path is illustrated in Figure 46. LOOPBACK has an internal pull-up resistor that defaults to normal mode during power up or if the pin is left floating. During loopback, the driver output and receiver input characteristics will still adhere to its appropriate specifications.

## DECODER AND D_LATCH FUNCTION

The SP508 contains a D_LATCH pin that latches the data into the D0, D1, and D2 decoder inputs. If tied to a logic LOW ("0"), the latch is transparent, allowing the data at the decoder inputs to propagate through and program the SP508 accordingly. If tied to a logic HIGH("1"), the latch locks out the data and prevents the mode from changing until this pin is brought to a logic LOW.

There are internal pull-up devices on D0, D1, and D2, which allow the device to be in SHUTDOWN mode ("111") upon power up. However , if the device is powered -up with the D_LATCH at a logic HIGH, the decoder state of the SP508 will be undefined.

## ESD TOLERANCE

The SP508 device incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electrostatic discharges and associated transients.

## CTR1/CTR2 EUROPEAN COMPLIANCY

As with all of Exar's previous multi-protocol serial transceiver IC's, the drivers and receivers have been designed to meet all the requirements to NET1/NET2 and TBR2 in order to meet CTR1/CTR2 compliancy. The SP508 is also tested in-house at Exar and adheres to all the NET1/2 physical layer testing and the ITU Series V specifications before shipment. Please note that although the SP508 , as with its predecessors, adhere to CTR1/CTR2 compliancy testing, any complex or unusual configuration should be double-checked to ensure CTR1/CTR2 compliance. Consult the factory for details.

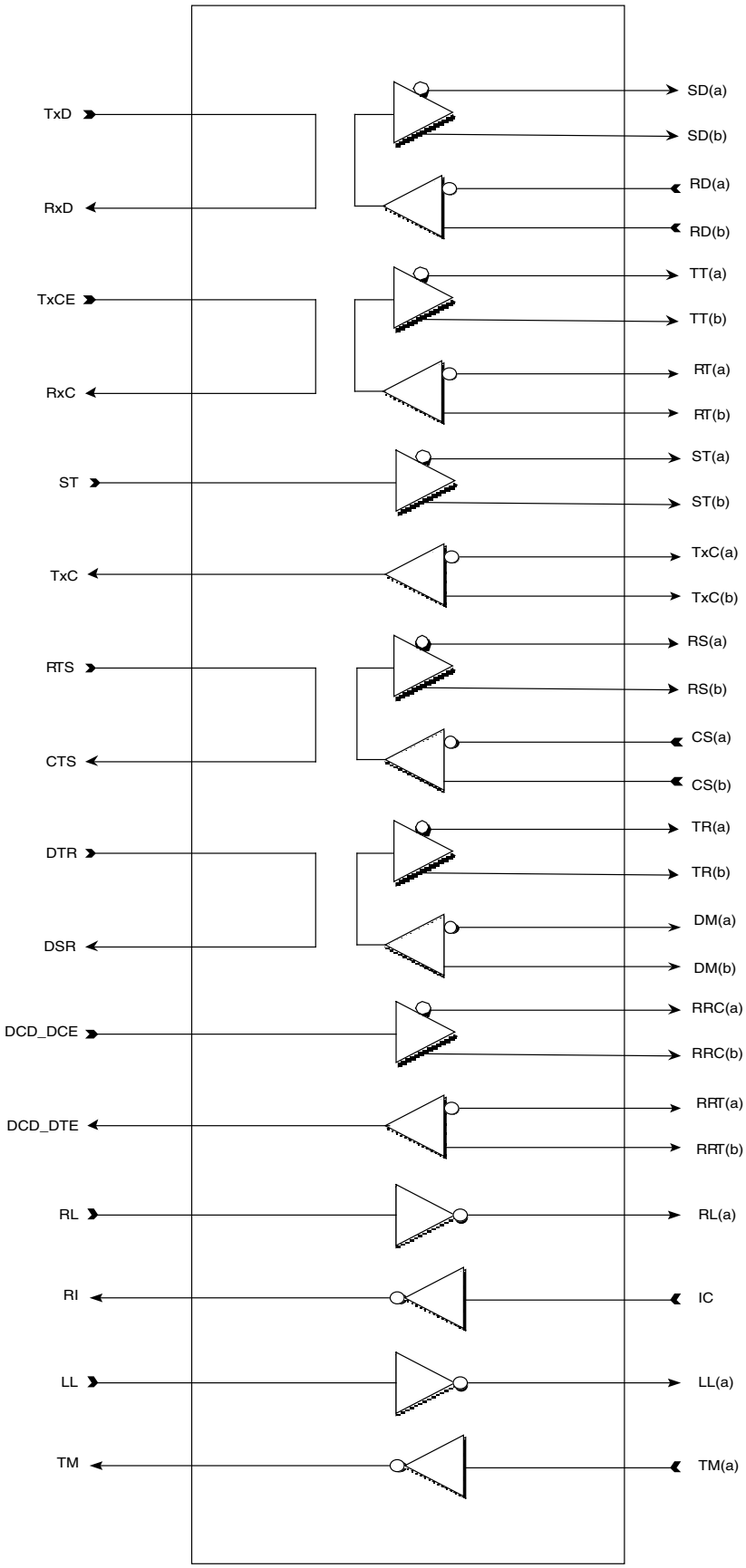



Figure 46. SP508 Loopback Path

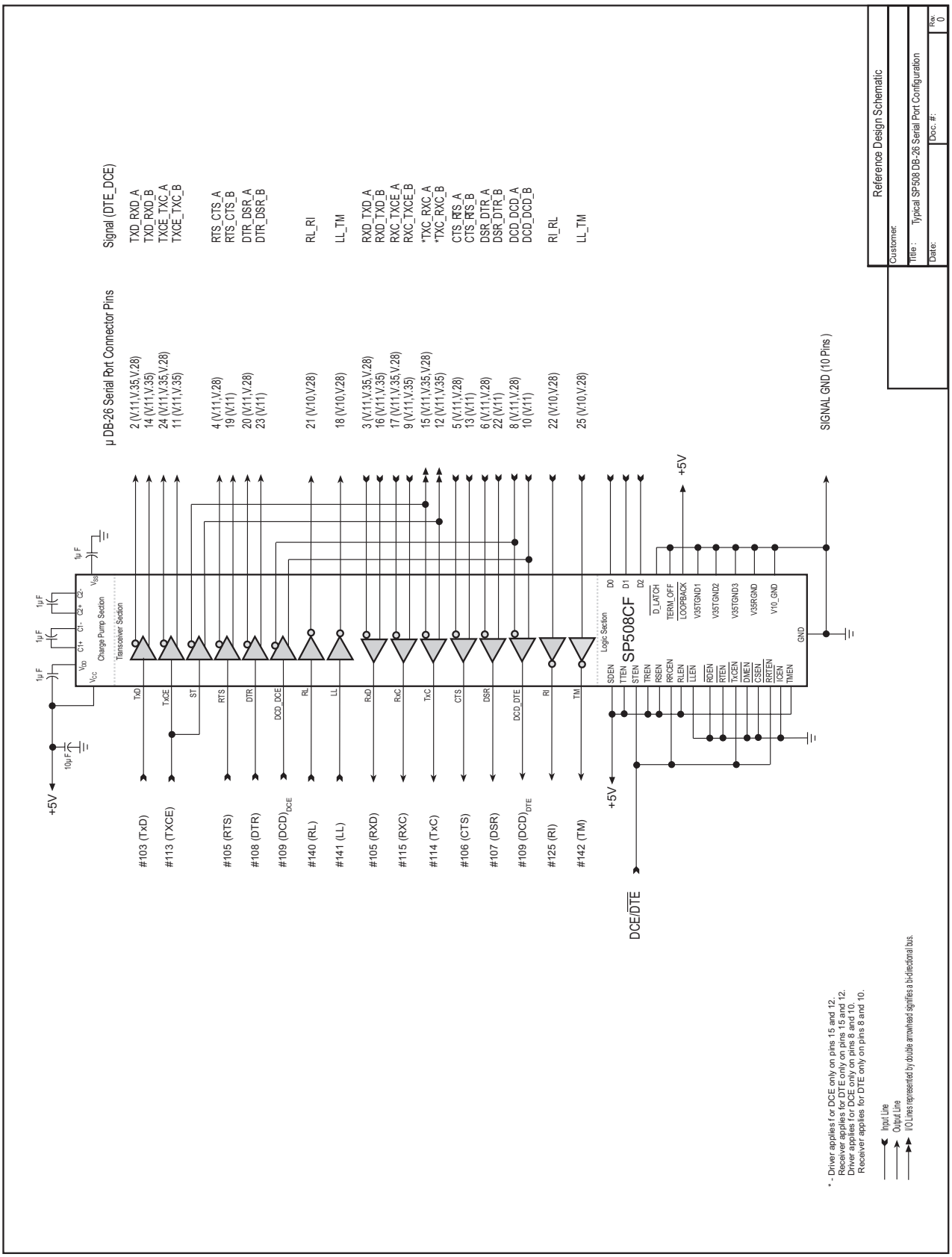
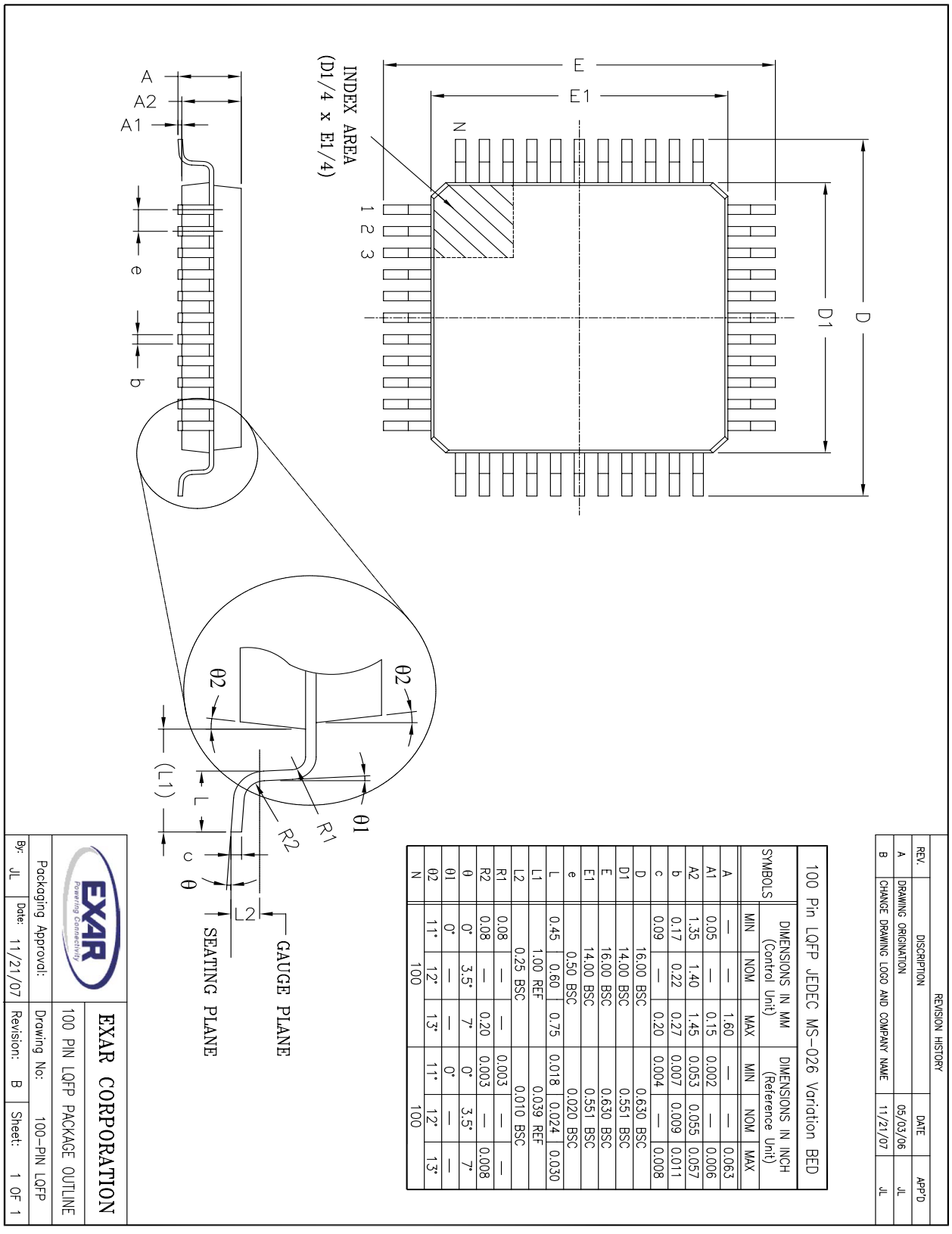



Figure 47. SP508 Typical Operating Configuration to Serial Port Connector with DCE/DTE programmability




| REVISION HISTORY | | | |
|---|---|---|---|
| REV. | DISCRIPTION | DATE | APP'D |
| A | DRAWING ORIGINATION | 05/03/06 | JL |
| B | CHANGE DRAWING LOGO AND COMPANY NAME | 11/21/07 | JL |

100 Pin LQFP JEDEC MS-026 Variation BED

| SYMBOLS | DIMENSIONS IN MM (Control Unit) | | | DIMENSIONS IN INCH (Reference Unit) | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.17 | 0.22 | 0.27 | 0.007 | 0.009 | 0.011 |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| D | 16.00 BSC | | | 0.630 BSC | | |
| D1 | 14.00 BSC | | | 0.551 BSC | | |
| E | 16.00 BSC | | | 0.630 BSC | | |
| E1 | 14.00 BSC | | | 0.551 BSC | | |
| e | 0.50 BSC | | | 0.020 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| L2 | 0.25 BSC | | | 0.010 BSC | | |
| R1 | 0.08 | — | — | 0.003 | — | — |
| R2 | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | — | — | 0° | — | — |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° |
| N | 100 | | | 100 | | |

EXAR CORPORATION

100 PIN LQFP PACKAGE OUTLINE

| Packaging Approval: | Drawing No: | 100-PIN LQFP |
|---|---|---|
| By: JL | Revision: B | Sheet: 1 OF 1 |
| Date: 11/21/07 | | |

SP508 Multiprotocol Configured as DCE

| Interface to System Logic | | | Interface to Port - Connector | |
|---|---|---|---|---|
| Pin Number | Pin Mnemonic | Circuit | Pin Mnemonic | Pin Number |
| 28 | TxD | Driver_1 | SD(A) | 97 |
| 3 | SDEN | | SD(B) | 100 |
| 29 | TxCE | Driver_2 | TT(A) | 92 |
| 4 | TTEN | | TT(B) | 95 |
| 30 | ST | Driver_3 | ST(A) | 87 |
| 5 | STEN | | ST(B) | 90 |
| 31 | RTS | Driver_4 | RS(A) | 83 |
| 6 | RSEN | | RS(B) | 85 |
| 32 | DTR | Driver_5 | TR(A) | 75 |
| 7 | TREN | | TR(B) | 78 |
| 33 | DCD_DCE | Driver_6 | RRC(A) | 81 |
| 8 | RRCEN | | RRC(B) | 79 |
| 34 | RL | Driver_7 | RL(A) | 65 |
| 9 | RLEN | | | |
| 35 | LL | Driver_8 | LL(A) | 63 |
| 10 | LLEN# | | | |
| 36 | RxD | Receiver_1 | RD(A) | 48 |
| 11 | RDEN# | | RD(B) | 47 |
| 37 | RxC | Receiver_2 | RT(A) | 50 |
| 12 | RTEN# | | RT(B) | 49 |
| 38 | TxC | Receiver_3 | TxC(A) | 53 |
| 13 | TxCEN# | | TxC(B) | 51 |
| 39 | CTS | Receiver_4 | CS(A) | 55 |
| 14 | CSEN# | | CS(B) | 54 |
| 40 | DSR | Receiver_5 | DM(A) | 57 |
| 15 | DMEN# | | DM(B) | 56 |
| 41 | DCD_DTE | Receiver_6 | RRT(A) | 60 |
| 16 | RRTEN# | | RRT(B) | 59 |
| 42 | RI | Receiver_7 | IC | 61 |
| 17 | ICEN# | | | |
| 43 | TM | Receiver_8 | TM(A) | 62 |
| 18 | TMEN | | | |

Spare drivers and receivers may be used for optional signals (Signal Quality, Rate Detect, Standby) or may be disabled using individual enable pins for each driver and receiver

Recommended Signals and Port Pin Assignments

| RS-232 or V.24 | | | EIA-530 | | | RS-449 | | | V.35 | | | X.21 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Signal Type | Mnemonic | DB-25 Pin(F) | Signal Type | Mnemonic | DB-25 Pin(F) | Signal Type | Mnemonic | DB-37 Pin(F) | Signal Type | Mnemonic | M34 Pin(F) | Signal Type | Mnemonic | DB-15 Pin(F) |
| V.28 | BB | 3 | V.11 | BB(A) | 3 | V.11 | RD(A) | 6 | V.35 | 104 | R | V.11 | R(A) | 4 |
| | | | V.11 | BB(B) | 16 | V.11 | RD(B) | 24 | V.35 | 104 | T | V.11 | R(B) | 11 |
| V.28 | DD | 17 | V.11 | DD(A) | 17 | V.11 | RT(A) | 8 | V.35 | 115 | V | V.11 | B(A) | 7** |
| | | | V.11 | DD(B) | 9 | V.11 | RT(B) | 26 | V.35 | 115 | X | V.11 | B(B) | 14** |
| V.28 | DB | 15 | V.11 | DB(A) | 15 | V.11 | ST(A) | 5 | V.35 | 114 | Y | V.11 | S(A) | 6 |
| | | | V.11 | DB(B) | 12 | V.11 | ST(B) | 23 | V.35 | 114 | AA | V.11 | S(B) | 13 |
| V.28 | CB | 5 | V.11 | CB(A) | 5 | V.11 | CS(A) | 9 | V.28 | 106 | D | V.11 | I(A) | 5 |
| | | | V.11 | CB(B) | 13 | V.11 | CS(B) | 27 | | | | V.11 | I(B) | 12 |
| V.28 | CC | 6 | V.11 | CC(A) | 6 | V.11 | DM(A) | 11 | V.28 | 107 | E | | | |
| | | | V.11 | CC(B) | 22 | V.11 | DM(B) | 29 | | | | | | |
| V.28 | CF | 8 | V.11 | CF(A) | 8 | V.11 | RR(A) | 13 | V.28 | 109 | F | | | |
| | | | V.11 | CF(B) | 10 | V.11 | RR(B) | 31 | | | | | | |
| V.28 | CE | 22 | | | | | | | V.28 | 125 | J | | | |
| | | | | | | | | | | | | | | |
| V.28 | TM | 25 | V.10 | TM | 25 | V.10 | TM | 18 | V.28 | 142 | NN | | | |
| | | | | | | | | | | | | | | |
| V.28 | BA | 2 | V.11 | BA(A) | 2 | V.11 | SD(A) | 4 | V.35 | 103 | P | V.11 | T(A) | 2 |
| | | | V.11 | BA(B) | 12 | V.11 | SD(B) | 22 | V.35 | 103 | S | V.11 | T(B) | 9 |
| V.28 | DA | 24 | V.11 | DA(A) | 24 | V.11 | TT(A) | 17 | V.35 | 113 | U | V.11 | X(A) | 7** |
| | | | V.11 | DA(B) | 11 | V.11 | TT(B) | 35 | V.35 | 113 | W | V.11 | X(B) | 14** |
| | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| V.28 | CA | 4 | V.11 | CA(A) | 4 | V.11 | RS(A) | 7 | V.28 | 105 | C | V.11 | C(A) | 3 |
| | | | V.11 | CA(B) | 19 | V.11 | RS(B) | 25 | | | | V.11 | C(B) | 10 |
| V.28 | CD | 20 | V.11 | CD(A) | 20 | V.11 | TR(A) | 12 | V.28 | 108 | H | | | |
| | | | V.11 | CD(B) | 23 | V.11 | TR(B) | 30 | | | | | | |
| | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| V.28 | RL | 21 | V.10 | RL | 21 | V.10 | RL | 14 | V.28 | 140 | N | | | |
| | | | | | | | | | | | | | | |
| V.28 | LL | 18 | V.10 | LL | 18 | V.10 | LL | 10 | V.28 | 141 | L | | | |
| | | | | | | | | | | | | | | |

Pin assignments and signal functions are subject to national or regional variation and proprietary / non-standard implementations

** X.21 use either B() or X(), not both

SP508 Multiprotocol Configured as DTE

| Interface to System Logic | | | Interface to Port-Connector | |
|---|---|---|---|---|
| Pin Number | Pin Mnemonic | Circuit | Pin Mnemonic | Pin Number |
| 28 | TxD | Driver_1 | SD(A) | 97 |
| 3 | SDEN | | SD(B) | 100 |
| 29 | TxCE | Driver_2 | TT(A) | 92 |
| 4 | TTEN | | TT(B) | 95 |
| 30 | ST | Driver_3 | ST(A) | 87 |
| 5 | STEN | | ST(B) | 90 |
| 31 | RTS | Driver_4 | RS(A) | 83 |
| 6 | RSEN | | RS(B) | 85 |
| 32 | DTR | Driver_5 | TR(A) | 75 |
| 7 | TREN | | TR(B) | 78 |
| 33 | DCD_DCE | Driver_6 | RRC(A) | 81 |
| 8 | RRCEN | | RRC(B) | 79 |
| 34 | RL | Driver_7 | RL(A) | 65 |
| 9 | RLEN | | | |
| 35 | LL | Driver_8 | LL(A) | 63 |
| 10 | LLEN# | | | |
| 36 | RxD | Receiver_1 | RD(A) | 48 |
| 11 | RDEN# | | RD(B) | 47 |
| 37 | RxC | Receiver_2 | RT(A) | 90 |
| 12 | RTEN# | | RT(B) | 49 |
| 38 | TxC | Receiver_3 | TxC(A) | 53 |
| 13 | TxCEN# | | TxC(B) | 51 |
| 39 | CTS | Receiver_4 | CS(A) | 55 |
| 14 | CSEN# | | CS(B) | 54 |
| 40 | DSR | Receiver_5 | DM(A) | 57 |
| 15 | DMEN# | | DM(B) | 56 |
| 41 | DCD_DTE | Receiver_6 | RRT(A) | 60 |
| 16 | RRTEN# | | RRT(B) | 59 |
| 42 | RI | Receiver_7 | IC | 61 |
| 17 | ICEN# | | | |
| 43 | TM | Receiver_8 | TM(A) | 62 |
| 18 | TMEN | | | |

Spare drivers and receivers may be used for optional signals (Signal Quality, Rate Detect, Standby) or may be disabled using individual enable pins for each driver and receiver

Recommended Signals and Port Pin Assignments

| RS-232 or V.24 | | | EIA-530 | | | RS-449 | | | V.35 | | | X.21 | | | AppleTalk™ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Signal Type | Mnemonic | DB-25 Pin(M) | Signal Type | Mnemonic | DB-25 Pin(M) | Signal Type | Mnemonic | DB-37 Pin(M) | Signal Type | Mnemonic | M34 Pin(M) | Signal Type | Mnemonic | DB-15 Pin(M) | Signal Type | Mnemonic | DIN-8 Pin(F) |
| V.28 | BA | 2 | V.11 | BA(A) | 2 | V.11 | SD(A) | 4 | V.35 | 103 | P | V.11 | T(A) | 2 | V.11 | TxD - | 3 |
| | | | V.11 | BA(B) | 14 | V.11 | SD(B) | 22 | V.35 | 103 | S | V.11 | T(B) | 9 | V.11 | TxD+ | 6 |
| V.28 | DA | 24 | V.11 | DA(A) | 24 | V.11 | TT(A) | 17 | V.35 | 113 | U | V.11 | X(A) | 7** | | | |
| | | | V.11 | DA(B) | 11 | V.11 | TT(B) | 35 | V.35 | 113 | W | V.11 | X(B) | 14** | | | |
| | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | |
| V.28 | CA | 4 | V.11 | CA(A) | 4 | V.11 | RS(A) | 7 | V.28 | 105 | C | V.11 | C(A) | 3 | | | |
| | | | V.11 | CA(B) | 19 | V.11 | RS(B) | 25 | | | | V.11 | C(B) | 10 | | | |
| V.28 | CD | 20 | V.11/10 | CD(A) | 20 | V.11 | TR(A) | 12 | V.28 | 108 | H | | | | V.10 | HSKo | 1 |
| | | | V.11/Z | CD(B) | 23 | V.11 | TR(B) | 30 | | | | | | | | | |
| | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | |
| V.28 | RL | 21 | V.10 | RL | 21 | V.10 | RL | 14 | V.28 | 140 | N | | | | | | |
| | | | | | | | | | | | | | | | | | |
| V.28 | LL | 18 | V.10 | LL | 18 | V.10 | LL | 10 | V.28 | 141 | L | | | | | | |
| | | | | | | | | | | | | | | | | | |
| V.28 | BB | 3 | V.11 | BB(A) | 3 | V.11 | RD(A) | 6 | V.35 | 104 | R | V.11 | R(A) | 4 | V.11 | RxD- | 5 |
| | | | V.11 | BB(B) | 16 | V.11 | RD(B) | 24 | V.35 | 104 | T | V.11 | R(B) | 11 | V.11 | RxD+ | 8 |
| V.28 | DD | 17 | V.11 | DD(A) | 17 | V.11 | RT(A) | 8 | V.35 | 115 | V | | | | | | |
| | | | V.11 | DD(B) | 9 | V.11 | RT(B) | 26 | V.35 | 115 | X | | | | | | |
| V.28 | DB | 15 | V.11 | DB(A) | 15 | V.11 | ST(A) | 5 | V.35 | 114 | Y | V.11 | S(A) | 6 | | | |
| | | | V.11 | DB(B) | 12 | V.11 | ST(B) | 23 | V.35 | 114 | AA | V.11 | S(B) | 13 | | | |
| V.28 | CB | 5 | V.11 | CB(A) | 5 | V.11 | CS(A) | 9 | V.28 | 106 | D | V.11 | I(A) | 5 | | GND | |
| | | | V.11 | CB(B) | 13 | V.11 | CS(B) | 27 | | | | V.11 | I(B) | 12 | V.10* | HSKi | 2 |
| V.28 | CC | 6 | V.11/10 | CC(A) | 6 | V.11 | DM(A) | 11 | V.28 | 107 | E | V.11 | B(A) | 7** | V.10 | GPi | 7 |
| | | | V.11/Z | CC(B) | 22 ‡ | V.11 | DM(B) | 29 | | | | V.11 | B(B) | 14** | | | |
| V.28 | CF | 8 | V.11 | CF(A) | 8 | V.11 | RR(A) | 13 | V.28 | 109 | F | | | | | | |
| | | | V.11 | CF(B) | 10 | V.11 | RR(B) | 31 | | | | | | | | | |
| V.28 | CE | 22 | V.10 | RI | 22 ‡ | | | | V.28 | 125 | J | | | | | | |
| | | | | | | | | | | | | | | | | | |
| V.28 | TM | 25 | V.10 | TM | 25 | V.10 | TM | 18 | V.28 | 142 | NN | | | | | | |
| | | | | | | | | | | | | | | | | | |

Pin assignments and signal functions are subject to national or regional variation and proprietary / non-standard implementations

‡ EIA-530 uses V.11 (differential) for DSR (CC) and DTR (CD) signals; EIA-530-A uses single-ended V.10 for DSR and DTR and adds RI signal on pin 22

** X.21 use either B() or X(), not both

## ORDERING INFORMATION

| Part Number | Top Mark | Temperature Range | Package Types |
|---|---|---|---|
| SP508CF-L | SP508CFYYWW | 0°C to +70°C | 100 Lead LQFP |
| SP508EF-L | SP508EFYYWW | -40°C to +85°C | 100 Lead LQFP |

## REVISION HISTORY

| DATE | REVISION | DESCRIPTION |
|---|---|---|
| 01/19/05 | -- | Legacy Sipex Datasheet |
| 10/27/09 | 1.0.0 | Convert to Exar Format and change revision to 1.0.0. Change Driver output leakage test (figure 32) from +/-12V to +/-10V. Change V.11 and V.35 driver and receiver propagation delay limits from 60ns to 80ns |



Datasheet October 2009

Send your Interface technical inquiry with technical details to: uarttechsupport@exar.com