



Subject: AT91SAM7S256 and AT91SAMS128 Errata Update

Date: November 13th, 2006

Device Part Numbers Affected (all Date Codes)

AT91SAM7S256-AU-001	AT91SAM7S128-AU-001
AT91SAM7S256-AU-999	AT91SAM7S128-AU-999
AT91SAM7S256-MU	AT91SAM7S128-MU
AT91SAM7S256-MU-999	AT91SAM7S128-MU-999

Watchdog Timer (WDT)

Under certain rare circumstances, if the Watchdog Timer is used with the Watchdog Reset enabled (WDRSTEN set at 1), the watchdog timer may lock the device in a reset state when the user restarts the watchdog (WDDRSTT). The only way to recover from this state is a power-on reset. The issue depends on the values of WDD and WDV in register WDT_MR.

Workaround:

Two workarounds are possible.

- 1) Either do not use the Watchdog Timer with the Watchdog Reset enabled (WDRSTEN set at 1),
- 2) or set WDD to 0xFFFF and in addition use only one of the following values for WDV:

0xFFFF, 0xDFFF, 0xBFFF, 0x9FFF, 0x7FFF, 0x77F, 0x6FFF, 0x67F, 0x5FFF, 0x57F, 0x4FFF, 0x47F, 0x3FFF, 0x37F, 0x2FFF, 0x27F, 0x1FFF, 0x1BF, 0x17F, 0x13F, 0x0FFF, 0x0DF, 0x0BF, 0x09F, 0x07F, 0x06F, 0x05F, 0x04F, 0x03F, 0x037, 0x02f, 0x027, 0x01F, 0x01B, 0x017, 0x013 and 0x00F.

Real-time Timer (RTT)

Under certain rare circumstances, the Real-time Timer Value (RTT_VR) may be corrupted.

Workaround

Use RTTINC as an increment for a software counter.

Slow clock selected in PMC and a Transition occurs on PA1

Under certain rare circumstances, when CSS=00 in PMC_MCKR, and PA1 is set as an input, and a transition occurs on PA1, device malfunction might occur.

Workaround

Do not transition PA1 as an input when CSS=00 in PMC_MCKR.

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Programming CSS in PMC MCKR register.

Under certain rare circumstances , reprogramming the CSS value in the PMC_MCKR register (i.e switching the main clock source) might generate malfunction of the device if the following 2 actions occur simultaneously.

1) Switching from:

- PLL Clock to Slow Clock or
- PLL Clock to Main Clock or
- Main Clock to PLL Clock or
- Main Clock to Slow Clock

AND

2) Program code is being executed out of flash, OR a transition is occurring on PA1, either as an input or output.

Note this issue does not occur when transitioning from slow clock to main clock or from slow clock to PLL clock.

Workaround

When changing CSS in the PMC_MCKR to switch from

- PLL Clock to Slow Clock or
- PLL Clock to Main Clock or
- Main Clock to PLL Clock or
- Main Clock to Slow Clock

Ensure that the processor is executing out of SRAM, AND ensure no transition occurs on PA1 either as an input or output, starting from writing to the PMC_MCKR register until MCKRDY=1.

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