AK5392

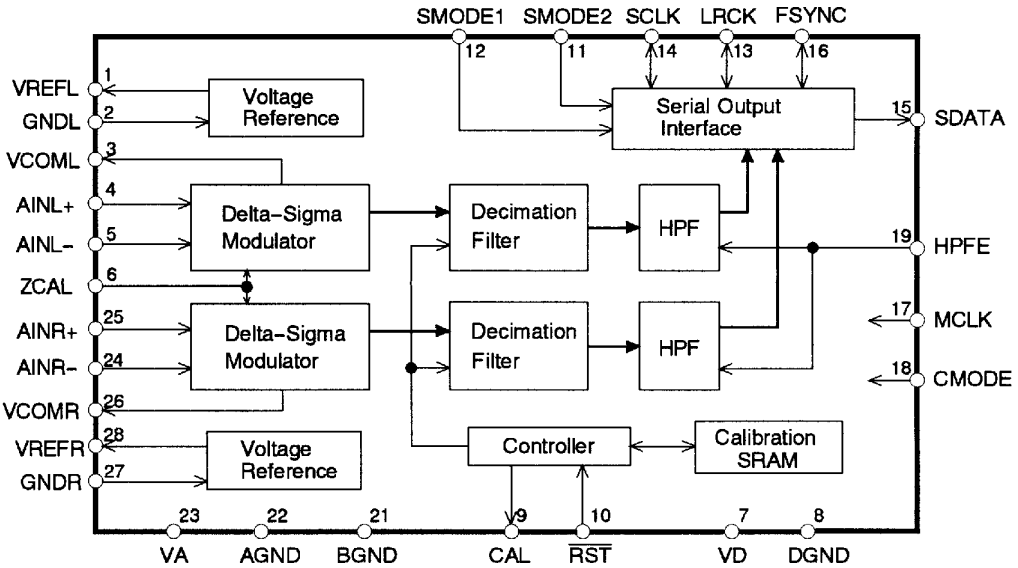
Enhanced Dual Bit ΔΣ 24Bit ADC

General Description

The AK5392 is a 24bit, 128x oversampling 2ch A/D Converterfor professional digital audio systems. The modulator in the AK5392 uses the new developed Enhanced Dual Bit architecture. This new architecture achieves the wider dynamic range, while keeping much the same superior distortion characteristics as conventional Single Bit way. The AK5392 performs 116dB dynamic range, so the device is suitable for professional studio equipments such as digital mixer, digital VTR etc.

Features

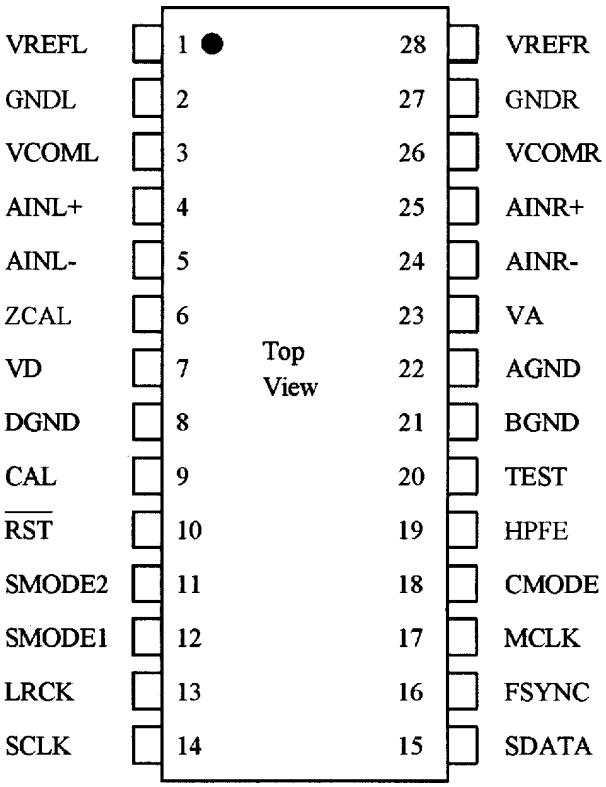
- ☐ Enhanced Dual Bit ADC
- ☐ Sampling Rate: 1kHz~54kHz
- ☐ Full Differential Inputs
- ☐ S/(N+D): 105dB
- ☐ DR: 116dB
- ☐ S/N: 116dB
- ☐ High Performance Linear Phase Digital Anti-Alias filter
  - Passband: 0~21.768kHz(@fs=48kHz)
  - Ripple: 0.001dB
  - Stopband: 110dB
- ☐ Digital HPF & Offset Calibration for Offset Cancel
- ☐ Master Clock: 256/384fs
- ☐ Power Supply: 5V±5%(Analog), 3~5.25V(Digital)
- ☐ Power Dissipation: 470mW
- ☐ Package: 28pin SOP



■ Ordering Guide

AK5392-VS	-10~+70°C	28pin SOP
AKD5392	AK5392 Evaluation Board	

■ Pin Layout



■ Compatibility with AK5391

1. Changed Specs

Parameter	AK5391	AK5392
HPF	No	Yes
Output Resolution	20/24bit	24bit
DR	113dB	116dB
Input Offset	Required	Not required

2. Pin Compatibility

The following pin functions are changed from AK5391. AK5392 supports 24bit only.

Pin No.	AK5391	AK5392
2	VREFL-	GNDL
19	SEL24	HPFE
27	VREFR-	GNDR

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VREFL	O	Lch Reference Voltage Pin, 3.75V Normally connected to GNDL with a 10uF electrolytic capacitor and a 0.1uF ceramic capacitor
2	GNDL	-	Lch Reference Ground Pin, 0V
3	VCOML	O	Lch Common Voltage Pin, 2.5V
4	AINL+	I	Lch Analog positive input Pin
5	AINL-	I	Lch Analog negative input Pin
6	ZCAL	I	Zero Calibration Control Pin This pin controls the calibration reference signal. "L":VCOML and VCOMR "H":Analog Input Pins(AINL±,AINR±)
7	VD	-	Digital Power Supply Pin, 3.3V
8	DGND	-	Digital Ground Pin, 0V
9	CAL	O	Calibration Active Signal Pin "H" means the offset calibration cycle is in progress. Offset calibration starts when $\overline{RST}$ goes "H". CAL goes "L" after 8704 LRCK cycles.
10	$\overline{RST}$	I	Reset Pin When "L", Digital section is powered-down. Upon returning "H", an offset calibration cycle is started. An offset calibration cycle should always be initiated after power-up.
11 12	SMODE2 SMODE1	I I	Serial Interface Mode Select Pin MSB first, 2's compliment. SMODE2 SMODE1 MODE LRCK L L Slave mode : MSB justified : H/L L H Master mode : Similar to I2S : H/L H L Slave mode : I2S : L/H H H Master mode : I2S : L/H
13	LRCK	I/O	Left/Right Channel Select Clock Pin LRCK goes "H" at SMODE2="L" and "L" at SMODE2="H" during reset when SMODE1 "H".

14	SCLK	I/O	Serial Data Clock Pin Data is clocked out on the falling edge of SCLK. Slave mode: SCLK requires more than 48fs clock. Master mode: SCLK outputs a 128fs clock. SCLK stays "L" during reset.
15	SDATA	O	Serial Data Output Pin MSB first, 2's complement. SDATA stays "L" during reset.
16	FSYNC	I/O	Frame Synchronization Signal Pin Slave mode: When "H", the data bits are clocked out on SDATA. Master mode: FSYNC outputs 2fs clock. FSYNC stays "L" during reset.
17	CLK	I	Master Clock Input Pin CMODE="H":384fs CMODE="L":256fs
18	CMODE	I	Master Clock Select Pin "L": CLK=256fs (12.288MHz @fs=48kHz) "H": CLK=384fs (18.432MHz @fs=48kHz)
19	HPFE	I	High Pass Filter Enable Pin "L": Disable "H": Enable
20	TEST	I	Test Pin Should be connected DGND.
21	BGND	-	Substrate Ground Pin, 0V
22	AGND	-	Analog Ground Pin, 0V
23	VA	-	Analog Supply Pin, 5V
24	AINR-	I	Rch Analog negative input Pin
25	AINR+	I	Rch Analog positive input Pin
26	VCOMR	O	Rch Common Voltage Pin, 2.5V
27	GNDR	-	Rch Reference Ground Pin, 0V
28	VREFR	O	Rch Reference Voltage Pin, 3.75V Normally connected to GNDR with a 10uF electrolytic capacitor and a 0.1uF ceramic capacitor

ABSOLUTE MAXIMUM RATINGS

(AGND,BGND,DGND=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supplies: Analog	VA	-0.3	6.0	V
Digital	VD	-0.3	6.0	V
|BGND-DGND| (Note 2)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies	IIN	-	±10	mA
Analog Input Voltage	VINA	-0.3	VA+0.3	V
Digital Input Voltage	VIND	-0.3	VD+0.3	V
Ambient Temperature (power applied)	Ta	-10	70	°C
Storage Temperature	Tstg	-65	150	°C

Note: 1 . All voltages with respect to ground.
2 . AGND and BGND must be same voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND,BGND,DGND=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supplies: Analog	VA	4.75	5.0	5.25	V
(Note 3) Digital	VD	3.0	3.3	5.25	V

Notes: 1 . All voltages with respect to ground.
3 . The power up sequence between VA and VD is not critical.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VA=5.0V; VD=3.3V; AGND,BGND,DGND=0V; fs=48kHz; Signal Frequency=1kHz;
24bit Output; Measurement frequency=10Hz~20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
Resolution			24		Bits
Analog Input Characteristics:					
S/(N+D) (Note 4)	-1dBFS	98	105		dB
	-20dBFS	-	93		dB
	-60dBFS	-	53		dB
S/N (A-Weighted)		112	116		dB
Dynamic Range (A-Weighted,-60dBFS)		112	116		dB
Interchannel Isolation		110	120		dB
Interchannel Gain Mismatch			0.1	0.5	dB
Gain Drift				150	ppm/°C
Offset Error	after calibration, HPF=OFF		±200	±1000	LSB_{24}
	after calibration, HPF=ON		±1		LSB_{24}
Offset Drift (HPF=OFF)		-	±10	-	LSB_{24}/°C
Offset Calibration Range (HPF=OFF)			±50		mV
Input Voltage (AIN+)-(AIN-)		±2.36	±2.51	±2.66	V
Input Impedance		3	5		kΩ
Power Supplies					
Power Supply Current					
VA			90	130	mA
VD			6	9	mA
Power Dissipation			470	680	mW
Power Supply Rejection (Note 5)			70		dB

Notes: 4 . The ratio of the rms value of the signal to the rms sum of all the spectral components from 20Hz to 20kHz, without A-weight. Full power input signal is -0.5dBFS.

5 . DC to 26kHz. 110dB(typ) beyond 26kHz.

FILTER CHARACTERISTICS

(Ta=25°C; VA=5.0V±5%; VD=3.0~5.25V; fs=48kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter(Decimation LPF):						
Passband (Note 6)		PB	0		21.768	kHz
Stopband (Note 6)		SB	26.232			kHz
Passband Ripple		PR			±0.001	dB
Stopband Attenuation (Note 7)		SA	110			dB
Group Delay Distortion		ΔGD			0	us
Group Delay (Note 8)		GD		38.7		1/fs
ADC Digital Filter(HPF):						
Freqency response (Note 6)	-3dB	FR		1.0		Hz
	-0.5dB			2.9		Hz
	-0.1dB			6.5		Hz

Notes: 6 . The passband and stopband frequencies scale with fs. PB=0.4535fs, SB=0.5465fs

7 . The analog modulator samples the input at 6.144MHz for an output word rate of 48kHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for n x 6.144MHz±21.768kHz, where n=1,2,3···).

8 . The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 24bit data of both channels to the output register. 40.7/fs at HPF:ON.

DIGITAL CHARACTERISTICS

(Ta=25°C; VA=5.0V±5%; VD=3.0~5.25V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%VD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VD	V
High-Level Output Voltage Iout=-20uA	VOH	VD-0.1	-	-	V
Low-Level Output Voltage Iout=20uA	VOL	-		0.1	V
Input Leakage Current	Iin	-	-	±10	uA

SWITCHING CHARACTERISTICS

(Ta=25°C; VA=5.0V±5%; VD=3.0~5.25V; CL=20pF)

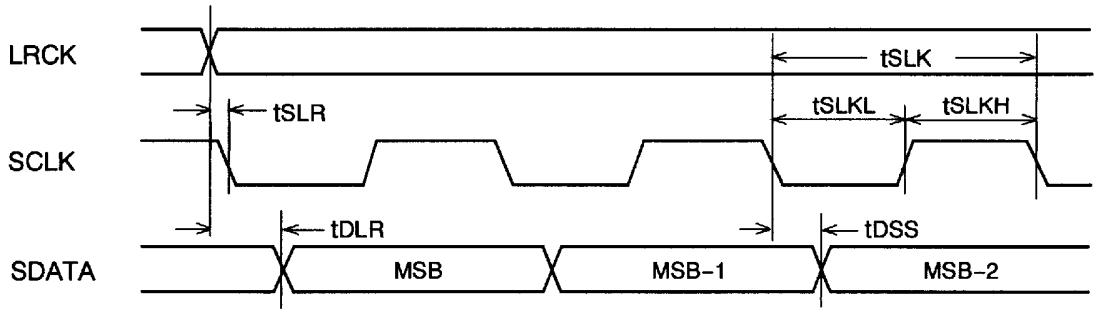
Parameter	Symbol	Min	Typ	Max	Units
Control Clock Frequency					
Master Clock 256fs:	fCLK	0.256	12.288	13.824	MHz
Pulse width Low	tCLKL	29			ns
Pulse width High	tCLKH	29			ns
384fs:	fCLK	0.384	18.432	20.736	MHz
Pulse width Low	tCLKL	20			ns
Pulse width High	tCLKH	20			ns
Serial Data Output Clock (SCLK)	fSLK		6.144	6.912	MHz
Channel Select Clock (LRCK)	fs	1	48	54	kHz
duty cycle		25		75	%
Serial Interface Timing (Note 9)					
Slave Mode(SMODE1="L")					
SCLK Period	tSLK	144.7			ns
SCLK Pulse Width Low	tSLKL	65			ns
Pulse width High	tSLKH	65			ns
SCLK falling to LRCK Edge (Note 10)	tSLR	-45		45	ns
LRCK Edge to SDATA MSB Valid	tDLR			45	ns
SCLK falling to SDATA Valid	tDSS			45	ns
SCLK falling to FSYNC Edge	tSF	-45		45	ns
Master Mode(SMODE1="H")					
SCLK Frequency	fSLK		128fs		Hz
duty cycle			50		%
FSYNC Frequency	fFSYNC		2fs		Hz
duty cycle			50		%
SCLK falling to LRCK Edge	tSLR	-20		20	ns
LRCK Edge to FSYNC rising	tLRF		1		tslk
SCLK falling to SDATA Valid	tDSS			45	ns
SCLK falling to FSYNC Edge	tSF	-20		20	ns
Reset/Calibration timing					
$\overline{\text{RST}}$ Pulse width	tRTW	150			ns
$\overline{\text{RST}}$ falling to CAL rising	tRCR			50	ns
$\overline{\text{RST}}$ rising to CAL falling (Note 11)	tRCF		8704		1/fs
$\overline{\text{RST}}$ rising to SDATA Valid (Note 11)	tRTV		8960		1/fs

Notes: 9 . Refer to Serial Data interface.

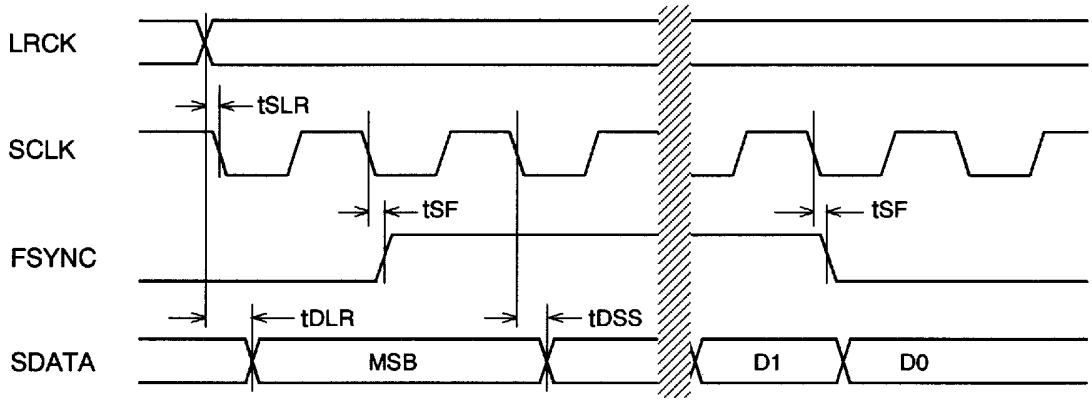
10 . Specified LRCK edges not to coincide with the rising edges of SCLK.

11 . The number of the LRCK rising edges after $\overline{\text{RST}}$ brought high. The value is in master mode. In slave mode it becomes one LRCK clock(1/fs) longer.

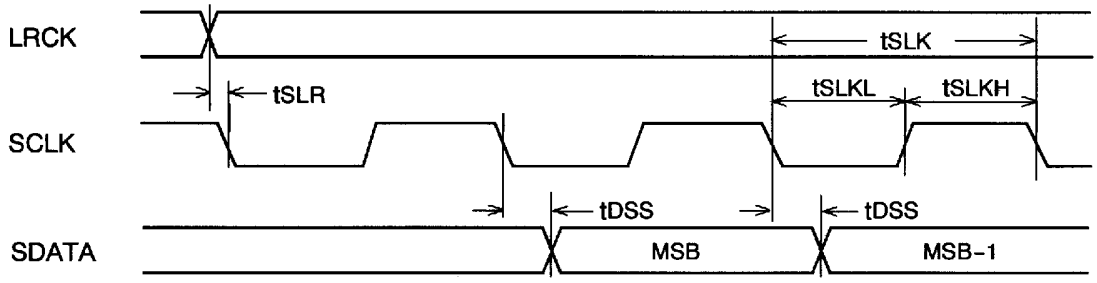
■ **Timing Diagram**



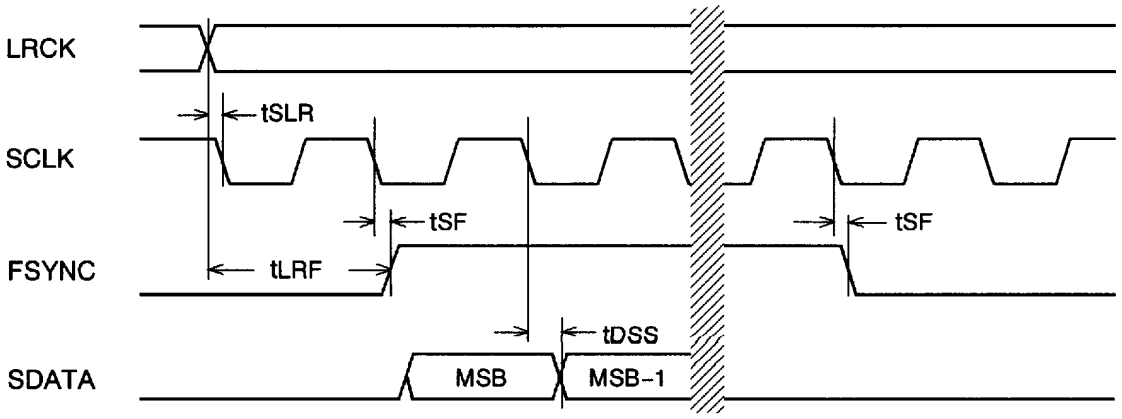
Serial Data Timing(Slave Mode, FSYNC="H")



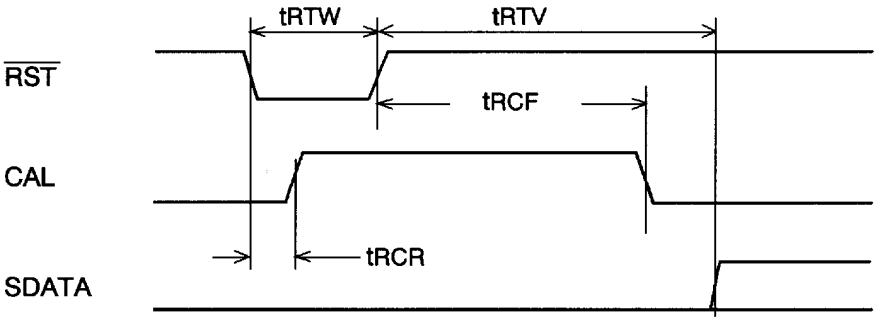
Serial Data Timing(Slave Mode)



Serial Data Timing(I^2S Slave Mode, FSYNC=Don't Care)



Serial Data Timing(Master Mode & I^2S Master Mode)



Reset & Calibration Timing

OPERATION OVERVIEW

■ System Clock Input

The external clocks which are required to operate the AK5392 are MCLK, LRCK(fs),SCLK. MCLK should be synchronized with LRCK but the phase is free of care. MCLK can be either 256fs or 384fs by setting CMODE pin. When the 384fs is selected, the internal master clock becomes 256fs(=384fs*2/3). Table 1 illustrates standard audio word rates and corresponding frequencies used in the AK5392.

As the AK5392 includes the phase detect circuit for LRCK, the AK5392 is reset automatically when the synchronization is out of phase by changing the clock frequencies. Therefore, the reset is only needed for power-up.

fs	MCLK		SCLK(128fs)
	256fs	384fs	
32.0kHz	8.1920MHz	12.2880MHz	4.0960MHz
44.1kHz	11.2896MHz	16.9344MHz	5.6448MHz
48.0kHz	12.2880MHz	18.4320MHz	6.1440MHz

Table 1 . Examples of System Clock

■ Serial Data Interface

AK5392 supports four serial data formats which can be selected via SMODE1 and SMODE2 pins(Table 2). The data format is MSB-first, 2's complement.

Figure	SMODE2	SMODE1	Mode	LRCK
Figure 1	L	L	Slave Mode	Lch=H, Rch=L
Figure 2	L	H	Master Mode	Lch=H, Rch=L
Figure 3	H	L	I2S Slave Mode	Lch=L, Rch=H
Figure 4	H	H	I2S Master Mode	Lch=L, Rch=H

Table 2 . Serial I/F Format

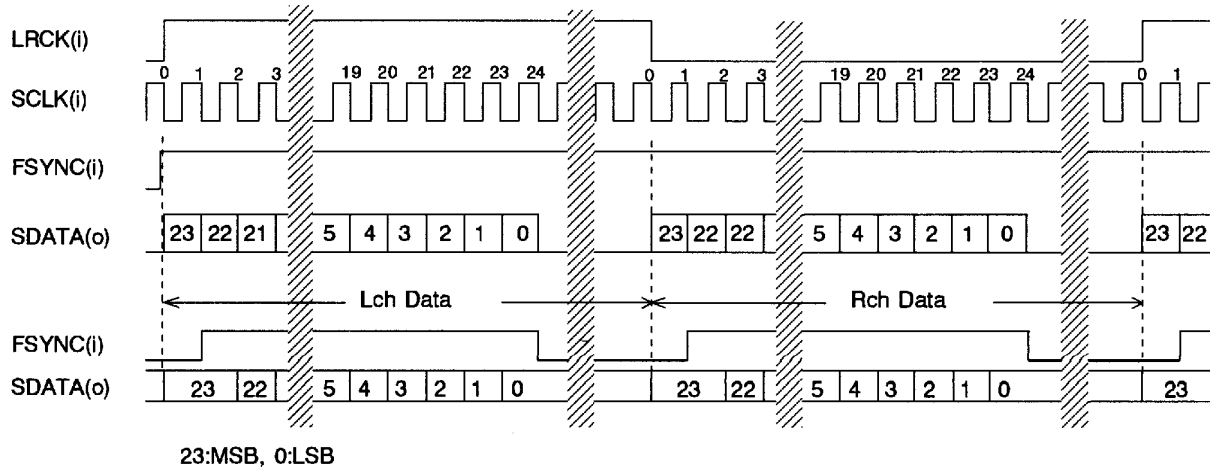


Figure 1. Serial Data Timing (Slave mode)

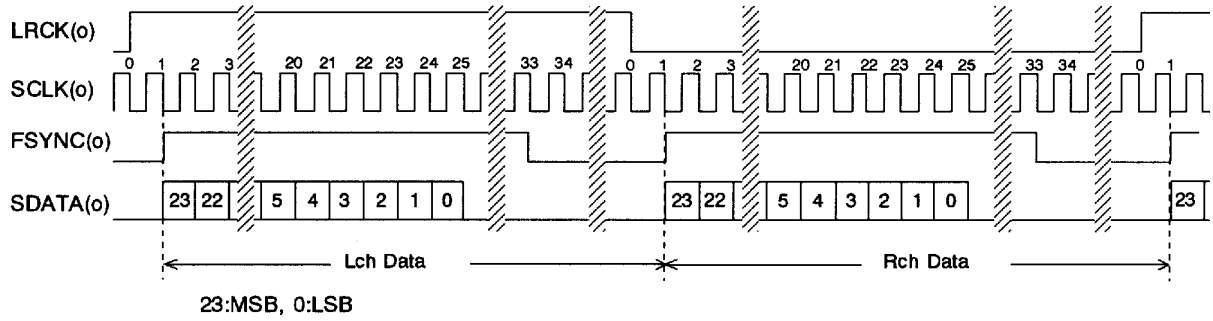


Figure 2. Serial Data Timing (Master mode)

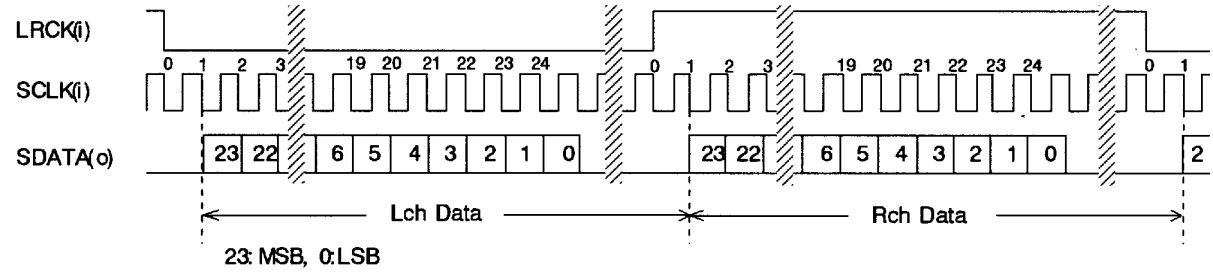


Figure 3. Serial Data Timing (I2S Slave mode)

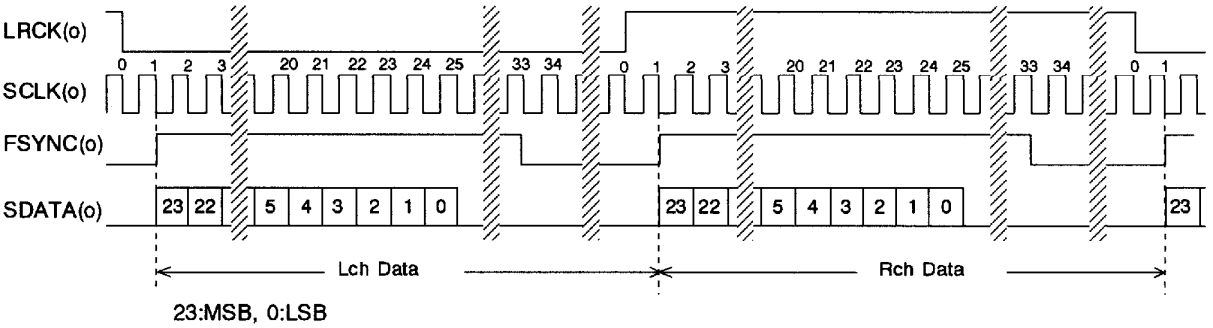


Figure 4. Serial Data Timing (I2S Master mode)

■ Offset Calibration

When $\overline{\text{RST}}$ pin goes to "L", the digital section is powered-down. Upon returning "H", an offset calibration cycle is started. An offset calibration cycle should always be initiated after power-up.

During the offset calibration cycle, the digital section of the part measures and stores the values of calibration input of each channel in registers. The calibration input value is subtracted from all future outputs. The calibration input may be obtained from either the analog input pins (AIN+/-) or the VCOM pins depending on the state of the ZCAL pin. With ZCAL "H", the analog input pin voltages are measured, and with ZCAL "L", the VCOM pin voltages are measured. The CAL output is "H" during calibration.

■ Digital High Pass Filter

The AK5392 also has a digital high pass filter for DC offset cancel. The cut-off frequency of the HPF is 1Hz at fs=48kHz and also scales with sampling rate(fs).

SYSTEM DESIGN

Figure 5 shows the system connection diagram. An evaluation board[AKD5392] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

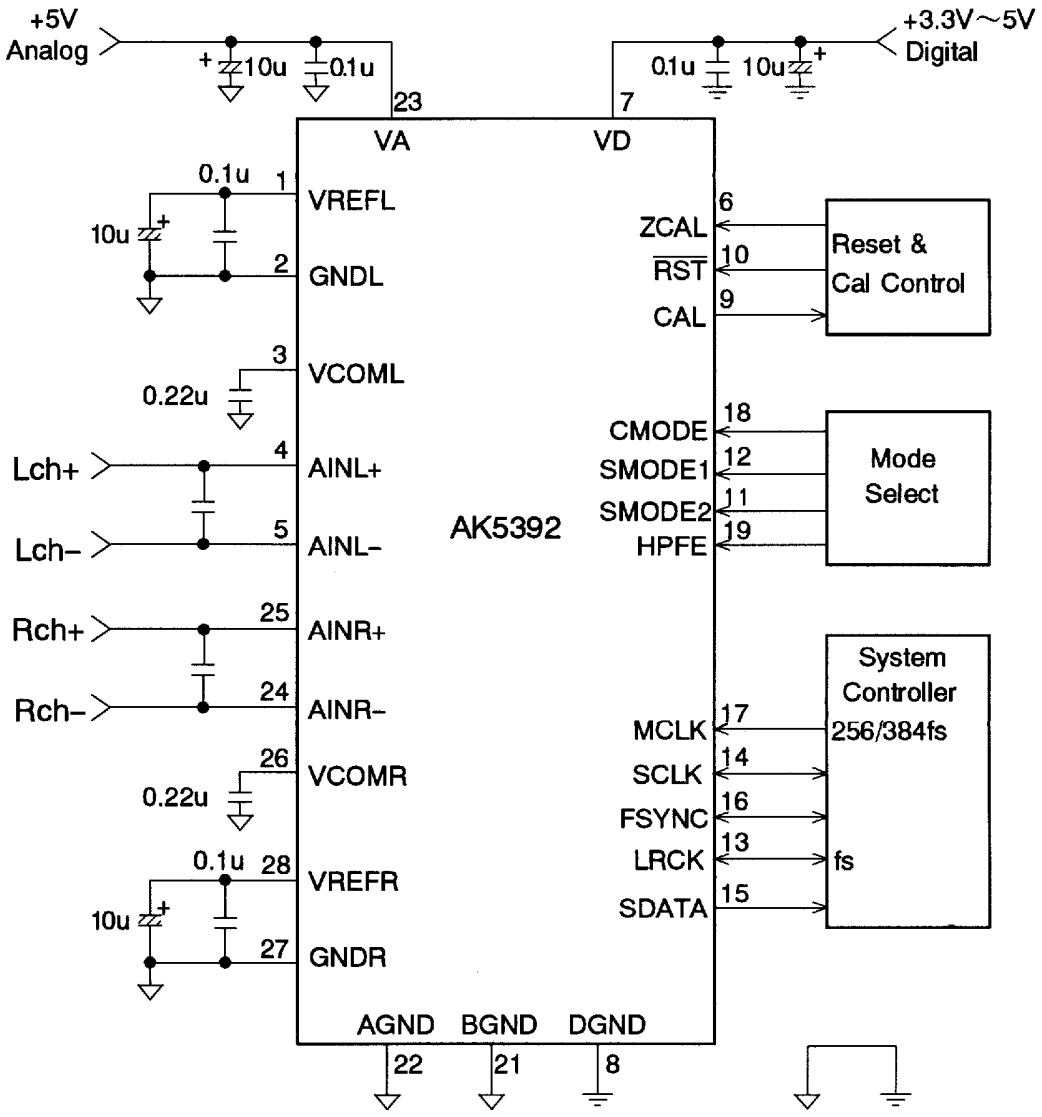


Figure 5 . Typical Connection Diagram

1. Grounding and Power Supply Decoupling

The AK5392 requires careful attention to power supply and grounding arrangements. Analog ground and digital ground should be separate and connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5392 as possible,with the small value ceramic capacitor being the nearest.

2. On-chip voltage reference and VCOM

The reference voltage for A/D converter is a fifferemtial voltage between the VREFL/R output voltage and the GNDL/R input voltage. The GNDL/R are connected to AGND and a 10uF electrolytic capacitor parallel with a 0.1uF ceramic capacitor between the VREFL/R and the GNDL/R eliminate the effects of high frequency noise. Especially a ceramic capacitor should be as near to the pins as possible. And all digital signals, especially clocks, should be kept away from the VREFL/R pins in order to avoid unwanted coupling into the AK5392. No load current may be taken from the VREFL/R pins.

VCOM is a common voltage of the analog signal. In order to eliminate the effects of high frequency noise, a 0.22uF ceramic capacitor should be connected as near to the VCOM pin as possible. And all signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK5392. No load current may be drawn from the VCOM pin.

3. Analog Inputs

Analog signal is differentially input into the modulator via the AIN+ and the AIN- pins. The input voltage is the difference between AIN+ and AIN- pins. The full-scale of each pin is nominally ±2.5Vpp(typ). The AK5392 can accept input voltages from AGND to VA. The ADC output data format is 2's complement The output code is 7FFFFFH(@24bit) for input above a positive full scale and 800000H(@24bit) for input below a negative full scale. The ideal code is 000000H(@24bit) with no input signal. The DC offset is removed by the offset calibration.

The AK5392 samples the analog inputs at 128fs(6.144MHz @fs=48kHz). The digital filter rejects noise above the stop band except for multiples of 128fs. A simple RC filter may be used to attenuate any noise around 128fs and most audio signals do not have significant energy at 128fs.

The AK5392 accepts +5V supply voltage. Any voltage which exceeds the upper limit of VA+0.3V and lower limit of AGND-0.3V and any current beyond 10mA for the analog input pins(AIN+/-) should be avoided. Excessive currents to the input pins may damage the device. Hence input pins must be protected from signals at or beyond these limits. Use caution specially in case of using ±15V in other analog circuits.

Figure 6 shows a input buffer circuit example. This is a full-differential input buffer circuit with an inverted-amp (gain: -10dB). The capacitor of 2200pF between VREF+/- decreases the clock feed through noise of modulator. And the resistor of 51 ohms is inserted in order to stabilize the op-amps before the ADC. This circuit is also a low pass filter with cut-off frequency of about 220kHz. In this example, the internal offset is removed by self calibration. The evaluation board should be refered about the detail.

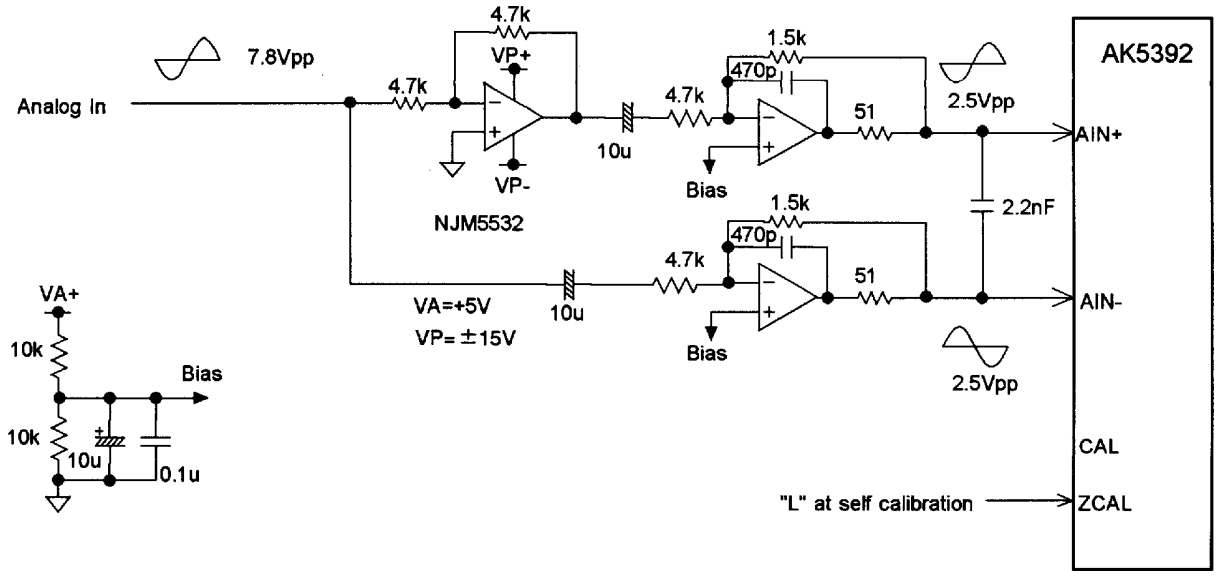
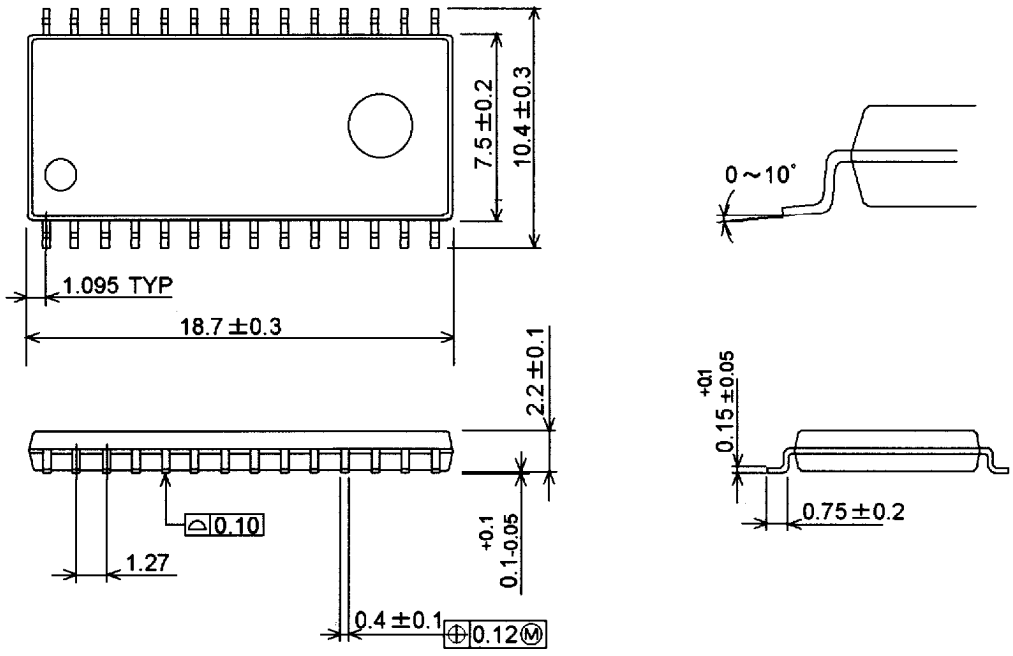


Figure 6 . Differential Input Buffer Example

PACKAGE

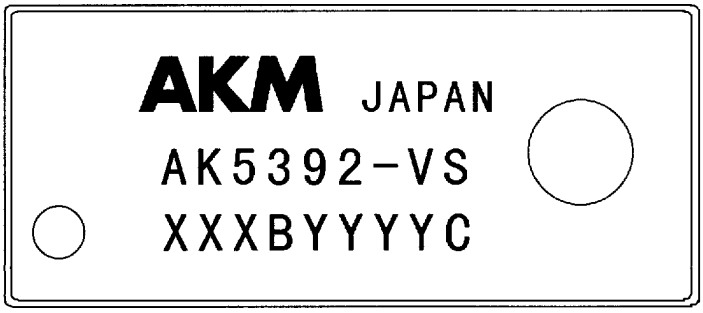
● 28pin SOP (Unit: mm)



■ **Package & Lead frame material**

Package molding compound :	Epoxy
Lead frame material :	Cu
Lead frame surface treatment :	Solder plate

MARKING



Contents of XXXBYYYYC

XXXB: Lot #(X:numbers,B:alphabet)

YYYYC: Date Code(Y:numbers,C:alphabet)

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