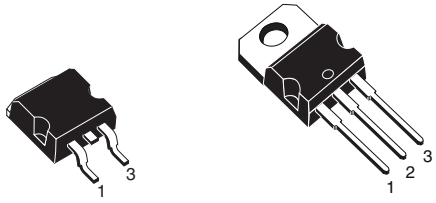
STB80N20M5
STP80N20M5

N-channel 200 V, 0.019 Ω, 61 A, TO-220, D^2PAK
MDmesh™ V Power MOSFET

Features

Type	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STB80N20M5	200 V	< 0.023 Ω	61 A
STP80N20M5			61 A

- Amongst the best $R_{DS(on)}$ * area
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested



D^2PAK TO-220

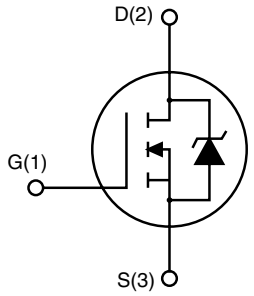
Application

Switching applications

Description

The devices are N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Figure 1. Internal schematic diagram



AM01475v1

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB80N20M5	80N20M5	D^2PAK	Tape and reel
STP80N20M5	80N20M5	TO-220	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	61	A
I_D	Drain current (continuous) at T_C = 100 °C	38	A
I_{DM} (1)	Drain current (pulsed)	244	A
P_{TOT}	Total dissipation at T_C = 25 °C	190	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	20	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	500	mJ
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 61$ A, di/dt ≤ 400 A/µs; $V_{Peak} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	D^2PAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.66		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.50		°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max		30	°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = max rating V_{DS} = max rating, T_C=125 °C				1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 30.5 A		0.019	0.023	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	4329 275 39	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 160 V, V_{GS} = 0	-	709	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	280	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	1.9	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 160 V, I_D = 30.5 A, V_{GS} = 10 V (see *Figure 15*)	-	104 23 53	-	nC nC nC

1. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
2. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 160 V, I_D = 61 A,	-	66	-	ns
$t_{r(v)}$	Voltage rise time	R_G = 4.7 Ω, V_{GS} = 10 V		31		ns
$t_{f(i)}$	Current fall time	(see *Figure 16*)		131		ns
$t_{c(off)}$	Crossing time	(see *Figure 19*)		176		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		61	A
I_{SDM} (1)	Source-drain current (pulsed)				244	A
V_{SD} (2)	Forward on voltage	I_{SD} = 61 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 61 A, di/dt = 100 A/µs	-	176		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V (see *Figure 19*)		1.4		µC
I_{RRM}	Reverse recovery current			16		A
t_{rr}	Reverse recovery time	I_{SD} = 61 A, di/dt = 100 A/µs	-	218		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_j = 150 °C		2		µC
I_{RRM}	Reverse recovery current	(see *Figure 19*)		19		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

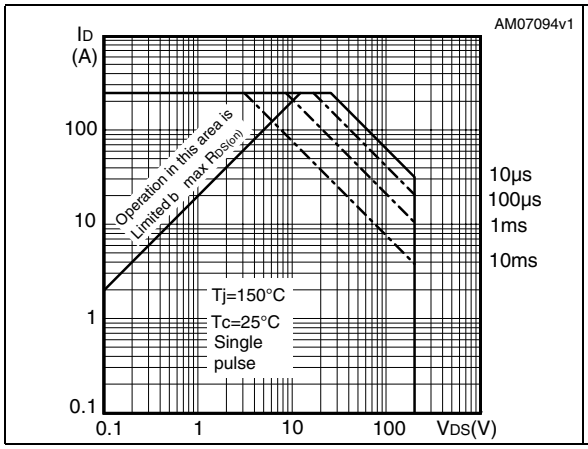


Figure 3. Thermal impedance

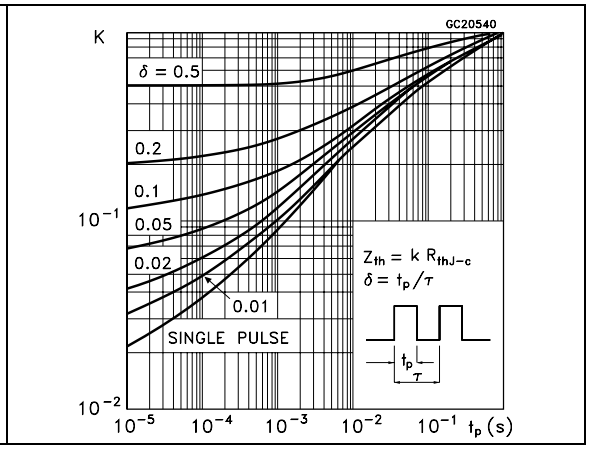


Figure 4. Output characteristics

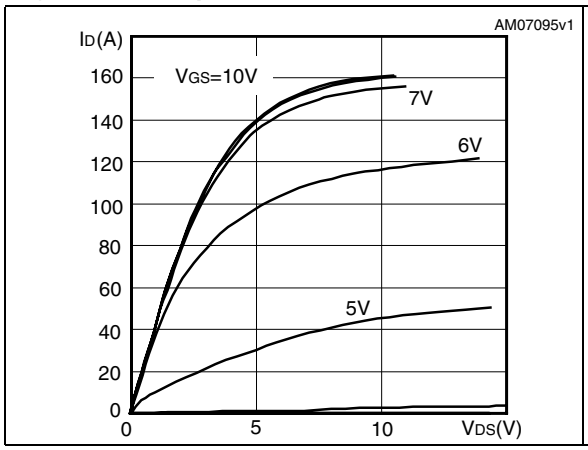


Figure 5. Transfer characteristics

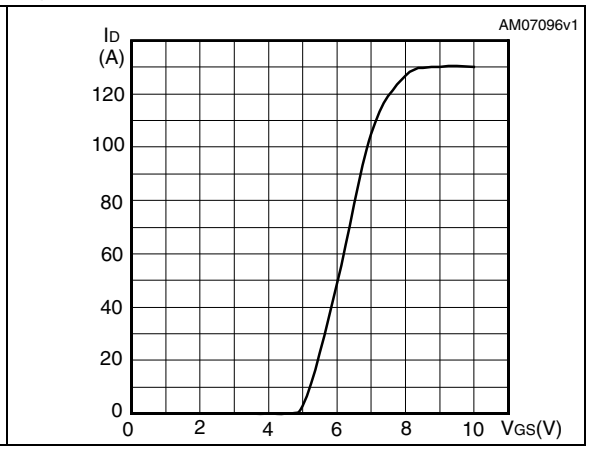


Figure 6. Gate charge vs gate-source voltage

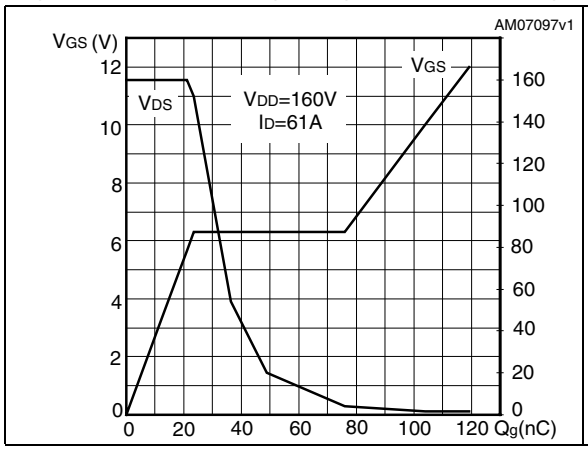


Figure 7. Static drain-source on resistance

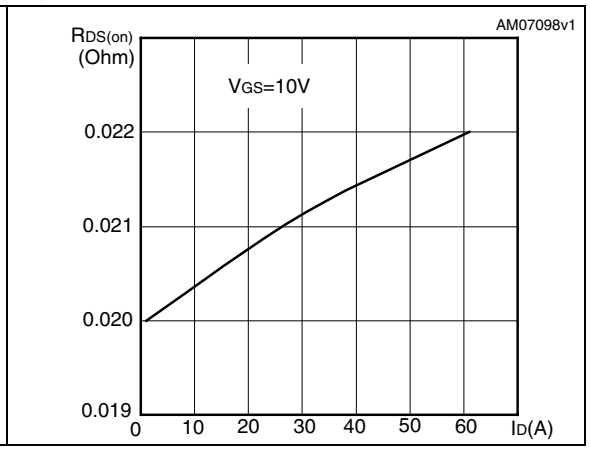


Figure 8. Capacitance variations

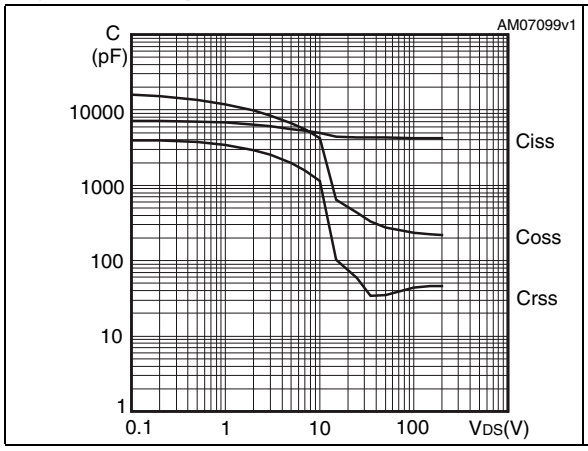


Figure 9. Output capacitance stored energy

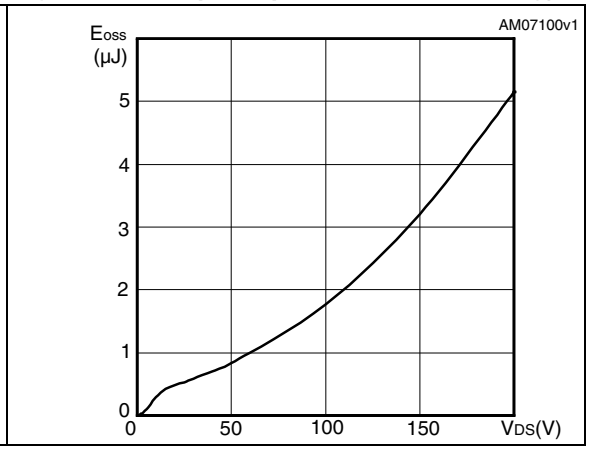


Figure 10. Normalized gate threshold voltage vs temperature

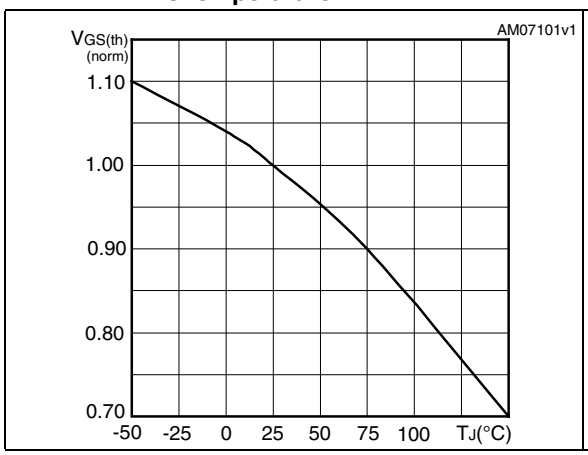


Figure 11. Normalized on resistance vs temperature

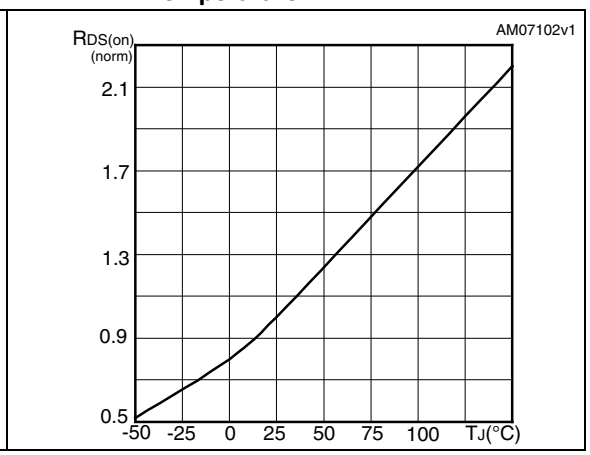


Figure 12. Source-drain diode forward characteristics

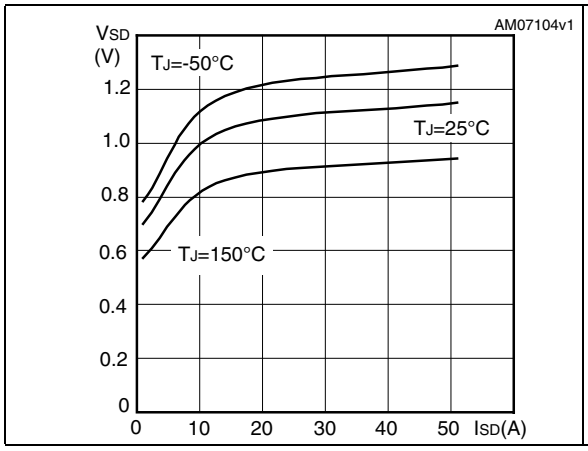
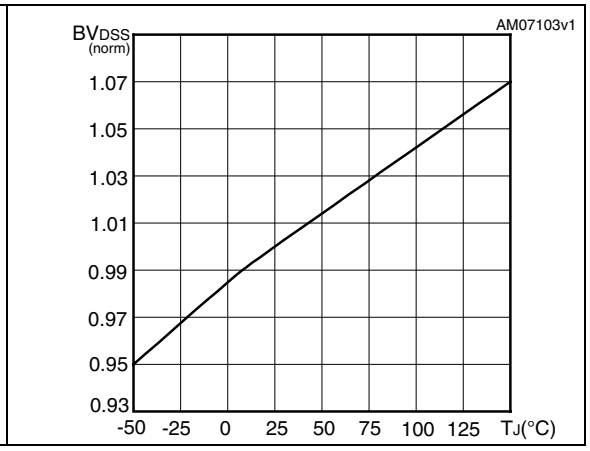


Figure 13. Normalized B_{VDSS} vs temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load

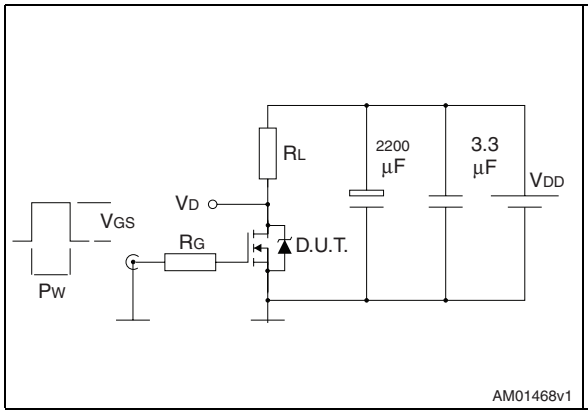


Figure 15. Gate charge test circuit

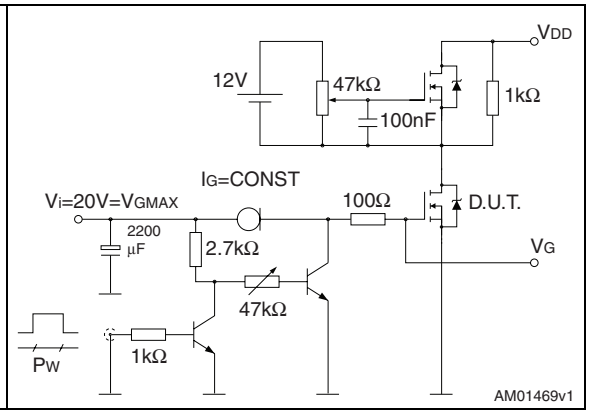


Figure 16. Test circuit for inductive load switching and diode recovery times

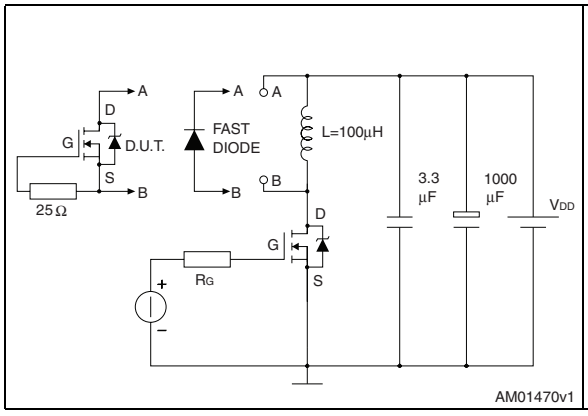


Figure 17. Unclamped inductive load test circuit

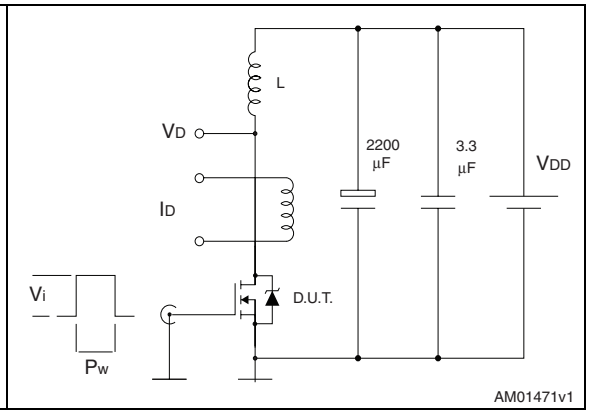


Figure 18. Unclamped inductive waveform

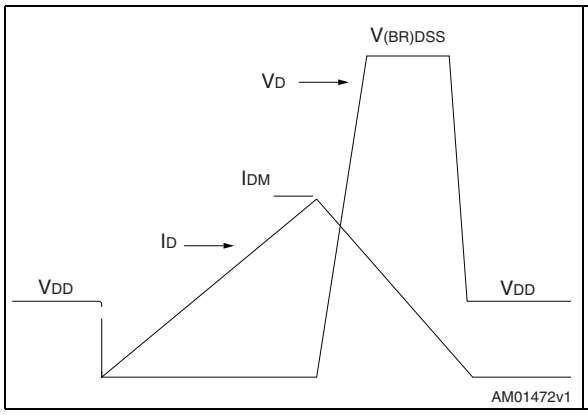
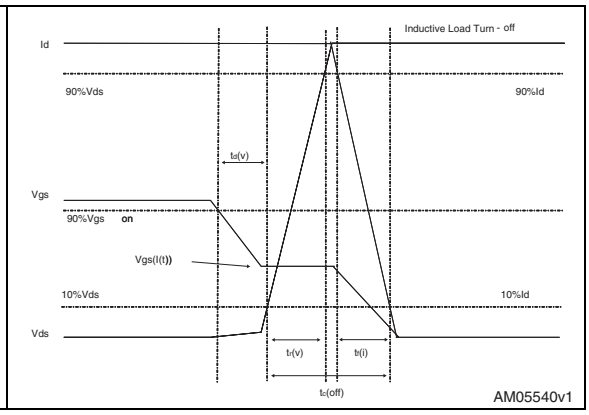


Figure 19. Switching time waveform

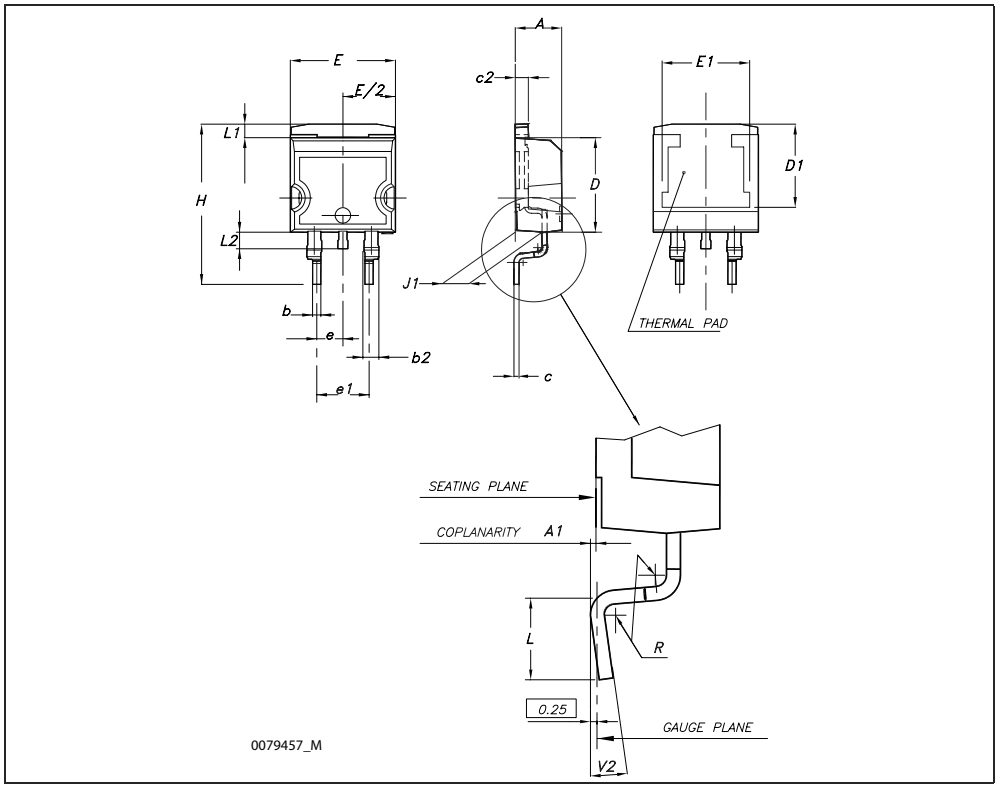


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

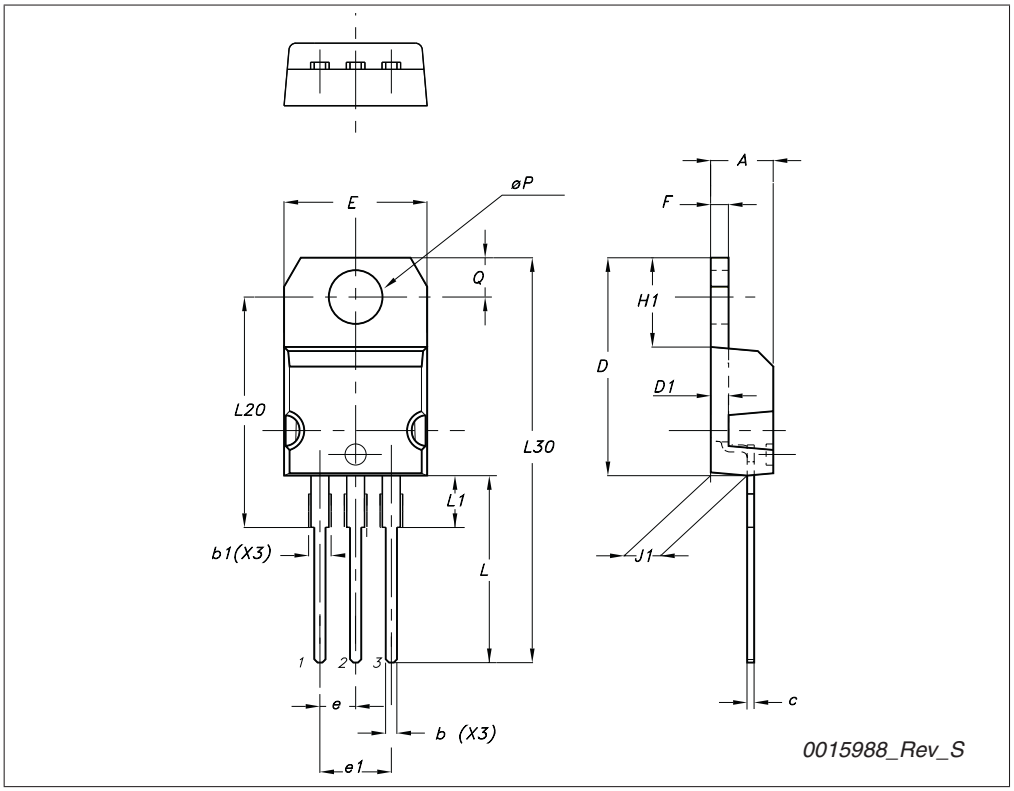
D²PAK (TO-263) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	0.03		0.23	0.001		0.009
b	0.70		0.93	0.027		0.037
b2	1.14		1.70	0.045		0.067
c	0.45		0.60	0.017		0.024
c2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1	7.50			0.295		
E	10		10.40	0.394		0.409
E1	8.50			0.334		
e		2.54			0.1	
e1	4.88		5.28	0.192		0.208
H	15		15.85	0.590		0.624
J1	2.49		2.69	0.099		0.106
L	2.29		2.79	0.090		0.110
L1	1.27		1.40	0.05		0.055
L2	1.30		1.75	0.051		0.069
R		0.4			0.016	
V2	0°		8°	0°		8°



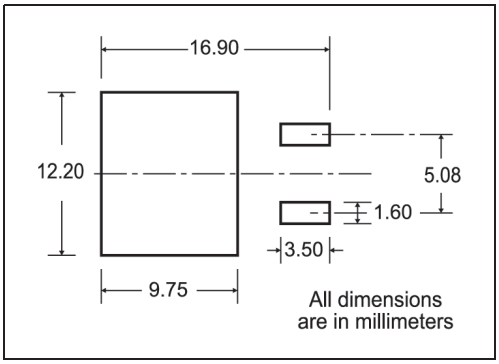
TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

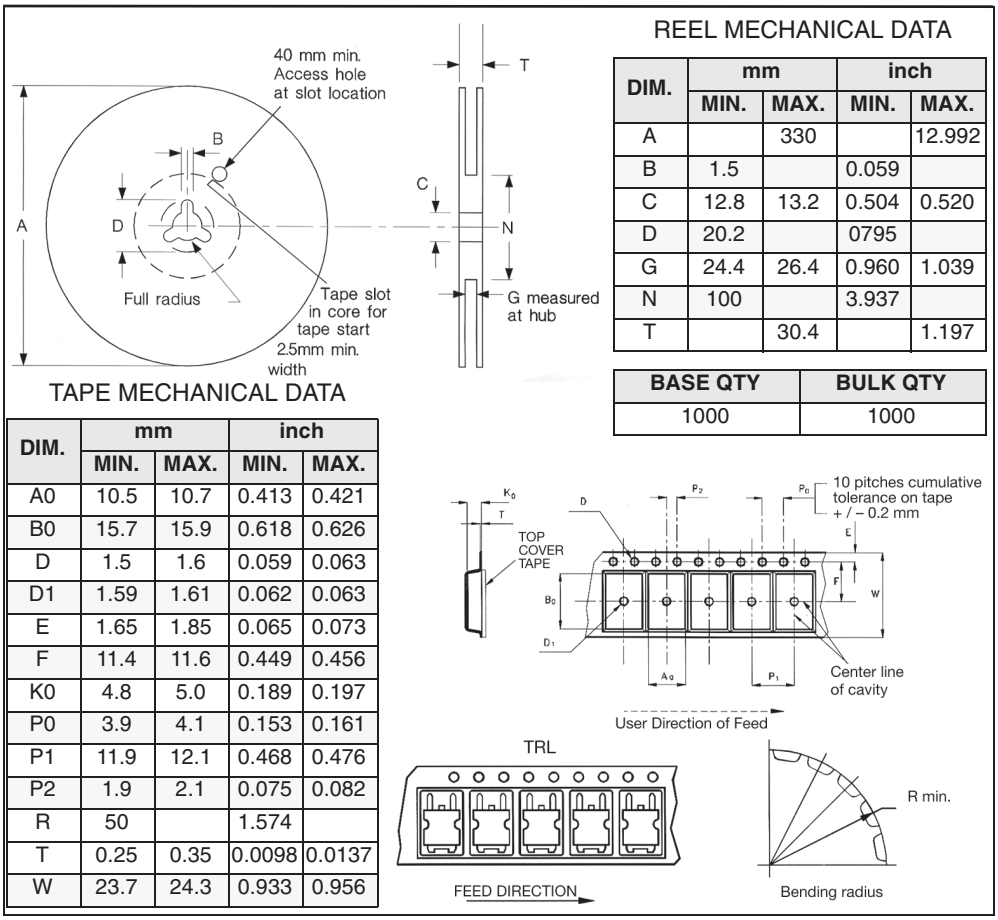


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

6 Revision history

Table 8. Document revision history

Date	Revision	Changes
01-Jul-2009	1	First release
03-Jul-2010	2	Document status promoted from preliminary data to datasheet