



# STD7N52DK3 STF7N52DK3, STP7N52DK3

N-channel 525 V, 0.95  $\Omega$ , 6 A, DPAK, TO-220FP, TO-220  
SuperFREDmesh3™ Power MOSFET

## Features

Order codes	V <sub>DSS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>w</sub>
STD7N52DK3	525 V	< 1.15 $\Omega$	6 A	90 W
STF7N52DK3			6 A <sup>(1)</sup>	25 W
STP7N52DK3			6 A	90 W

1. Limited by package

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

## Application

Switching applications

## Description

These devices are N-channel SuperFREDmesh3™, a new Power MOSFET technology that is obtained via improvements applied to STMicroelectronics' SuperMESH3™ technology. The resulting product has an extremely low on resistance, superior dynamic performance, high avalanche capability and a fast body-drain recovery diode, making it especially suitable for the most demanding applications.

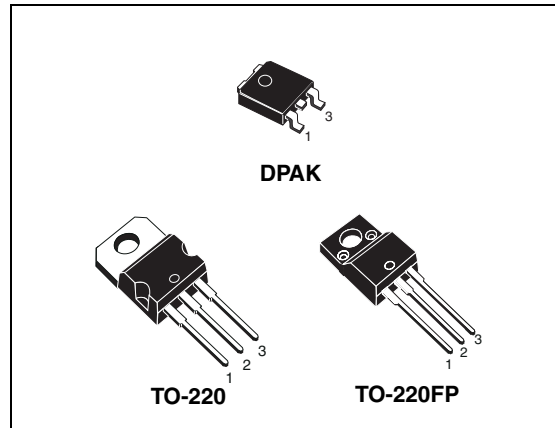
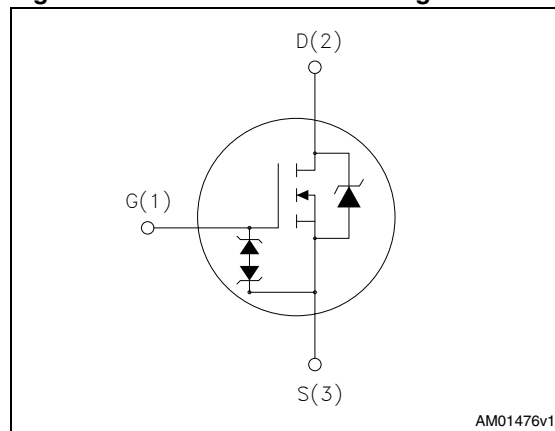


Figure 1. Internal schematic diagram



AM01476v1

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD7N52DK3	7N52DK3	DPAK	Tape and reel
STF7N52DK3	7N52DK3	TO-220FP	Tube
STP7N52DK3	7N52DK3	TO-220	Tube

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value			Unit
		TO-220	DPAK	TO-220FP	
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	525			V
$V_{GS}$	Gate- source voltage	$\pm 30$			V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	6		6 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	4		4 <sup>(1)</sup>	A
$I_{DM}^{(2)}$	Drain current (pulsed)	24		24 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	90		25	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	3			A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	100			mJ
$V_{ESD(G-S)}$	Gate source ESD(HBM-C = 100 pF, R = 1.5 k $\Omega$ )	2500			V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	20			V/ns
$di/dt$	Diode reverse recovery current slope	400			A/ $\mu$ s
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; $T_C = 25\text{ }^\circ\text{C}$ )			2500	V
$T_{stg}$	Storage temperature	-55 to 150			$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150			$^\circ\text{C}$

- Limited by package
- Pulse width limited by safe operating area
- $I_{SD} \leq 6\text{ A}$ , peak  $V_{DS} < V_{(BR)DSS}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value			Unit
		TO-220	DPAK	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	1.39		5	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max		50		$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5		62.5	$^\circ\text{C/W}$
$T_l$	Maximum lead temperature for soldering purpose	300		300	$^\circ\text{C}$

- When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	525			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ , $T_C = 125\text{ °C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 3\text{ A}$		0.95	1.15	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	870	-	$\mu\text{F}$
$C_{oss}$	Output capacitance			70		$\mu\text{F}$
$C_{rss}$	Reverse transfer capacitance			13		$\mu\text{F}$
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }525\text{ V}$ , $V_{GS} = 0$	-	53	-	$\mu\text{F}$
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			74		$\mu\text{F}$
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	3.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 420\text{ V}$ , $I_D = 6\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 20</a> )	-	33	-	nC
$Q_{gs}$	Gate-source charge			5		nC
$Q_{gd}$	Gate-drain charge			19		nC

- $C_{oss\text{ eq}}$  time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
- $C_{oss\text{ eq}}$  energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 260\text{ V}$ , $I_D = 3\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 19</a> )		12		ns
$t_r$	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off-delay time				37	ns
$t_f$	Fall time				19	ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				24	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 24</a> )	-	110		ns
$Q_{rr}$	Reverse recovery charge			440		nC
$I_{RRM}$	Reverse recovery current			8		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 24</a> )	-	140		ns
$Q_{rr}$	Reverse recovery charge			680		nC
$I_{RRM}$	Reverse recovery current			10		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ (open drain)	30		-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK

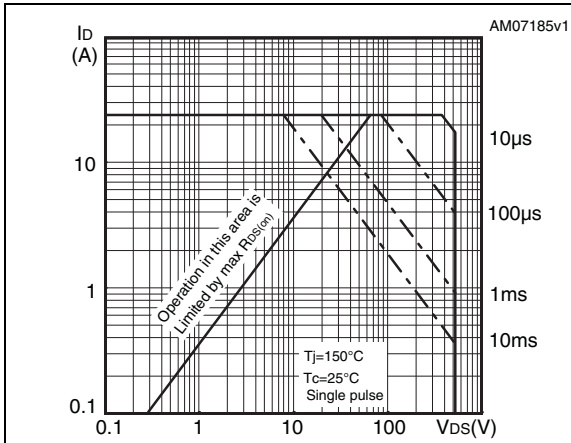


Figure 3. Thermal impedance for DPAK

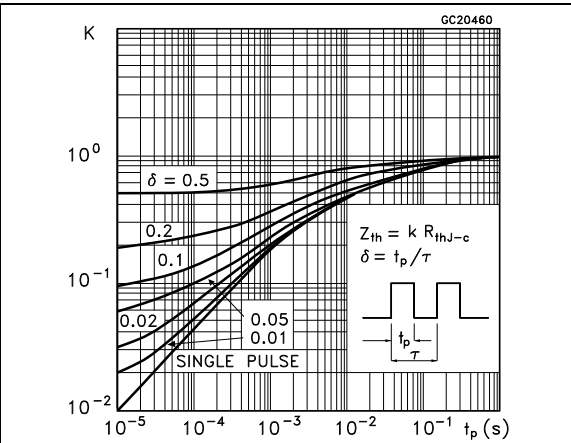


Figure 4. Safe operating area for TO-220FP

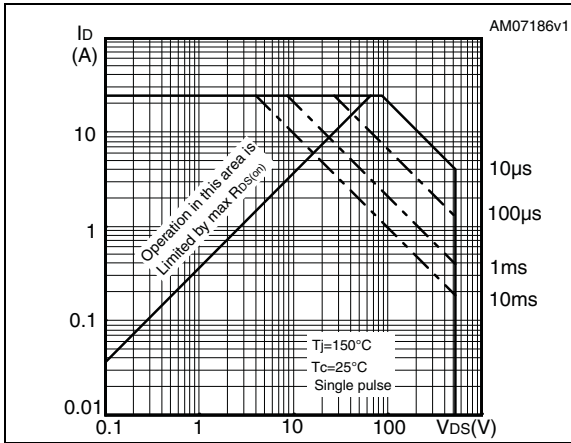


Figure 5. Thermal impedance for TO-220FP

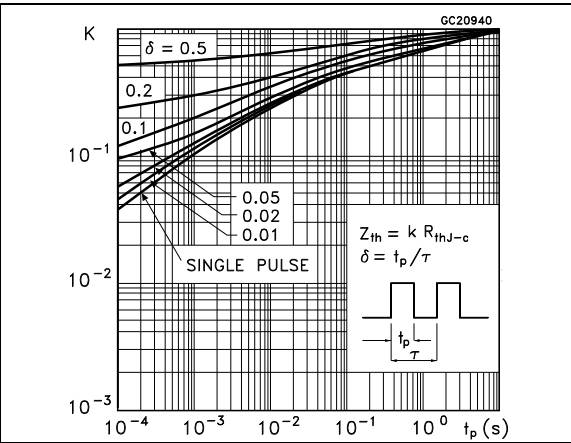


Figure 6. Safe operating area for TO-220

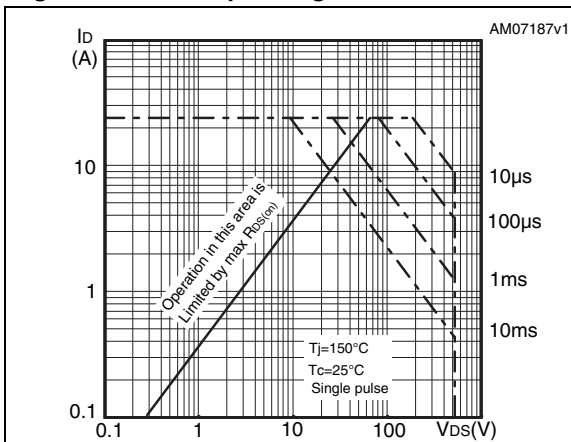


Figure 7. Thermal impedance for TO-220

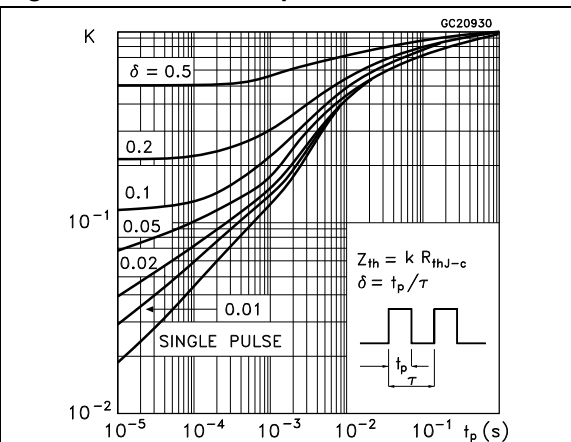


Figure 8. Output characteristics

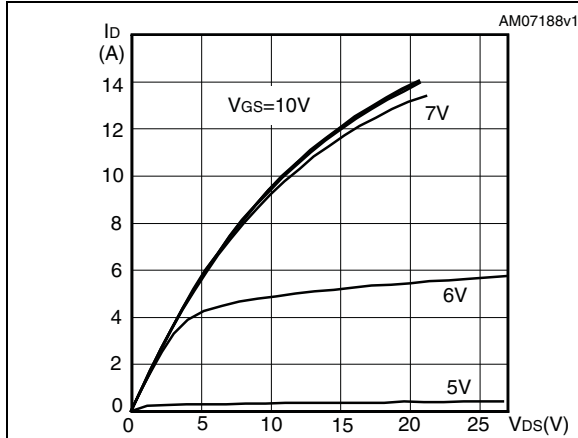


Figure 9. Transfer characteristics

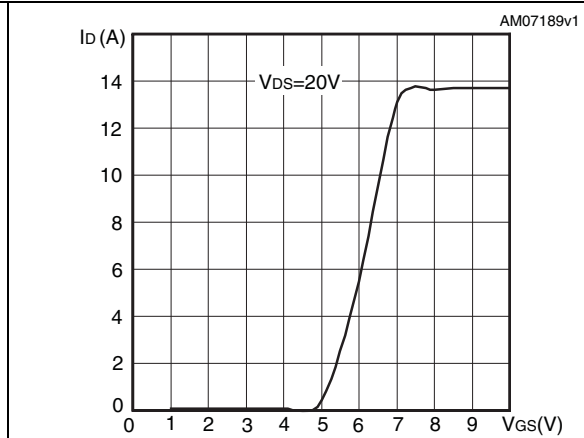


Figure 10. Gate charge vs gate-source voltage

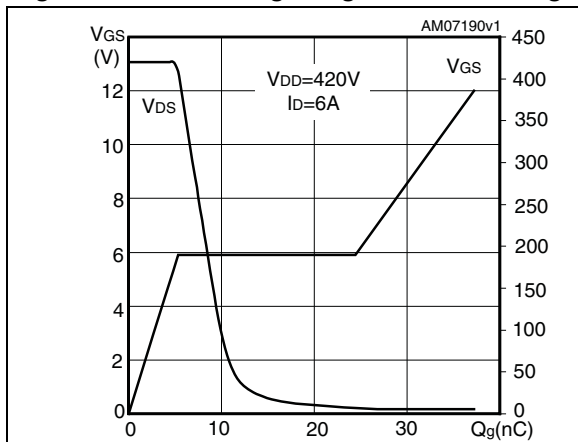


Figure 11. Static drain-source on resistance

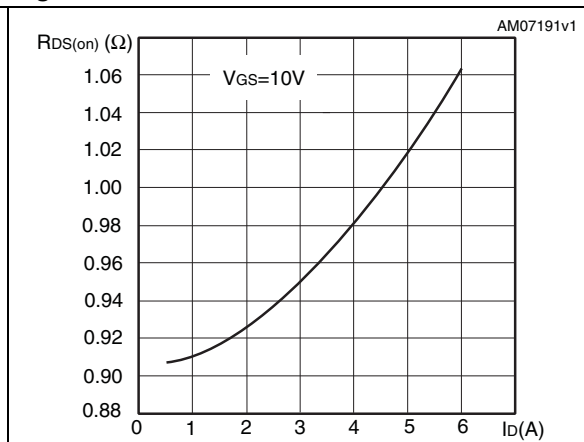


Figure 12. Capacitance variations

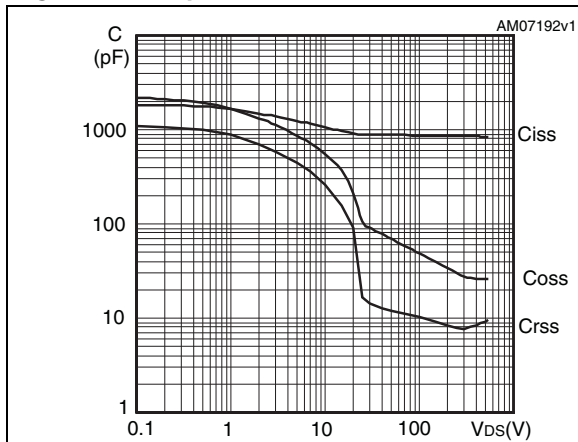


Figure 13. Output capacitance stored energy

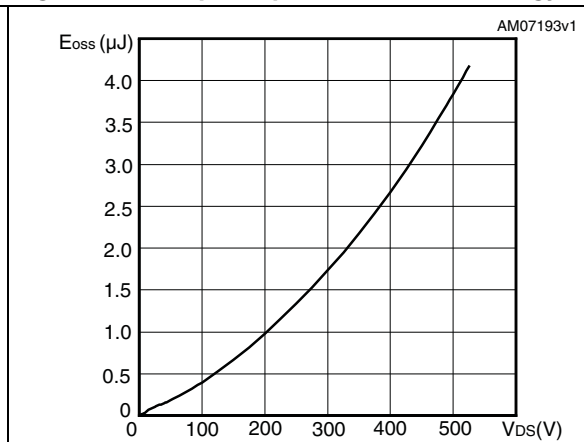


Figure 14. Normalized gate threshold voltage vs temperature

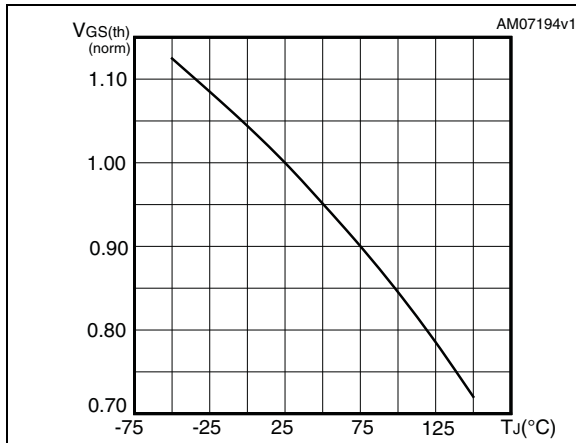


Figure 15. Normalized on resistance vs temperature

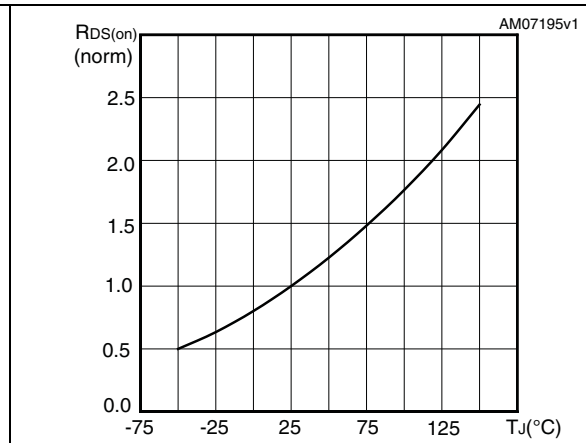


Figure 16. Source-drain diode forward characteristics

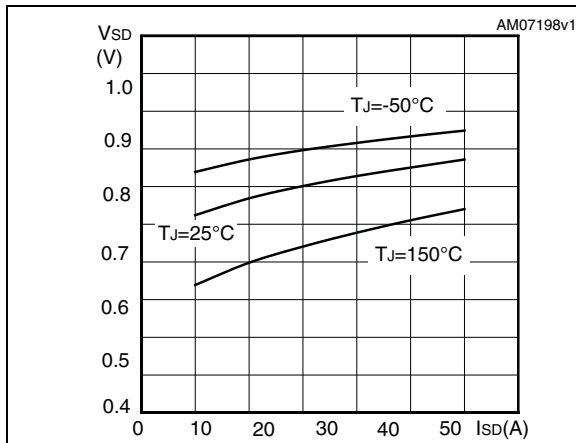


Figure 17. Normalized B<sub>V</sub>DSS vs temperature

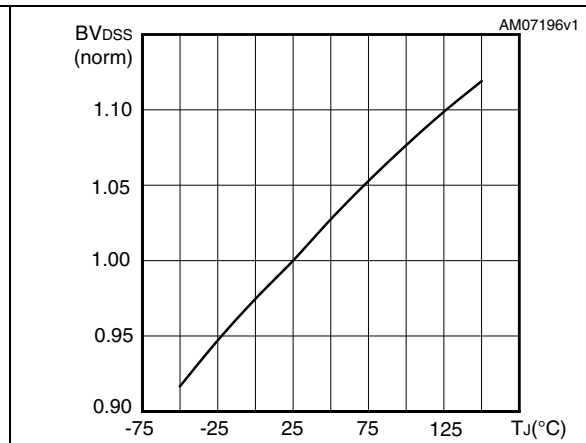
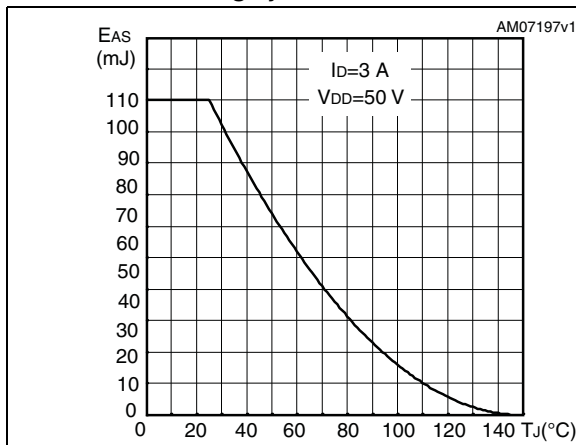


Figure 18. Maximum avalanche energy vs starting Tj





### 3 Test circuits

Figure 19. Switching times test circuit for resistive load

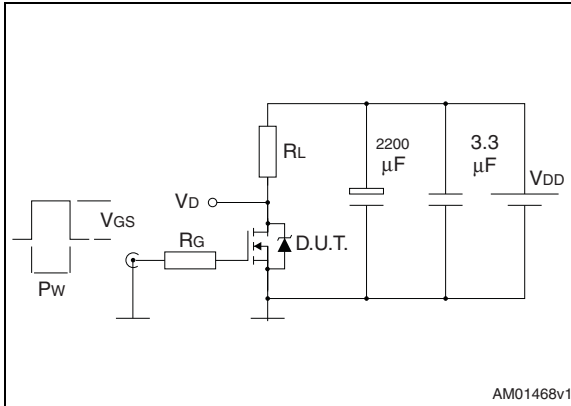


Figure 20. Gate charge test circuit

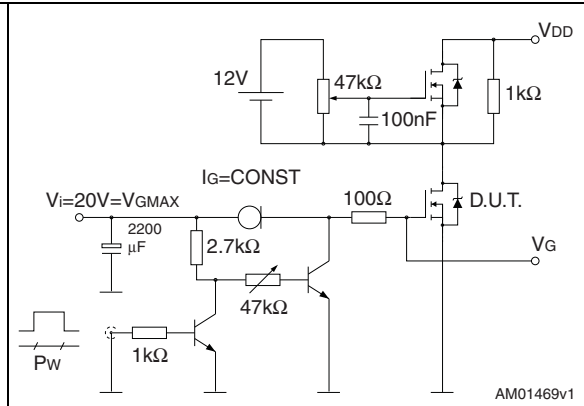


Figure 21. Test circuit for inductive load switching and diode recovery times

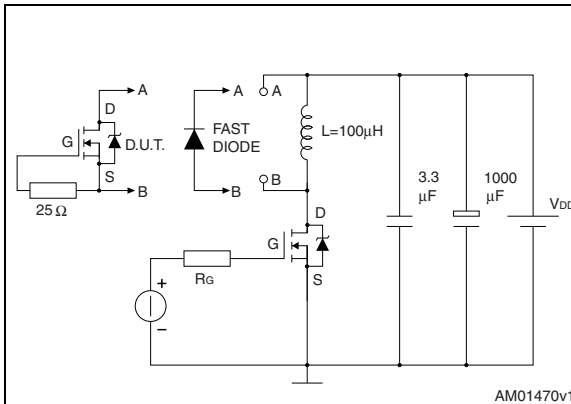


Figure 22. Unclamped inductive load test circuit

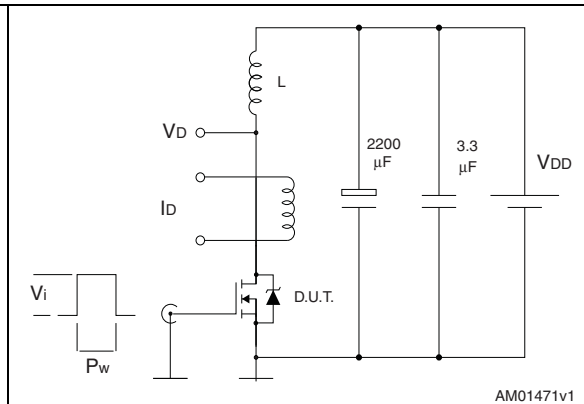


Figure 23. Unclamped inductive waveform

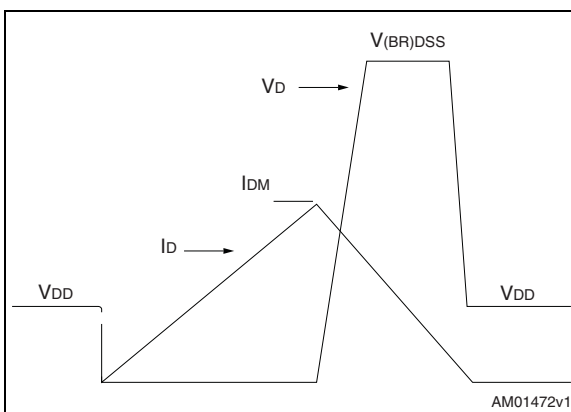
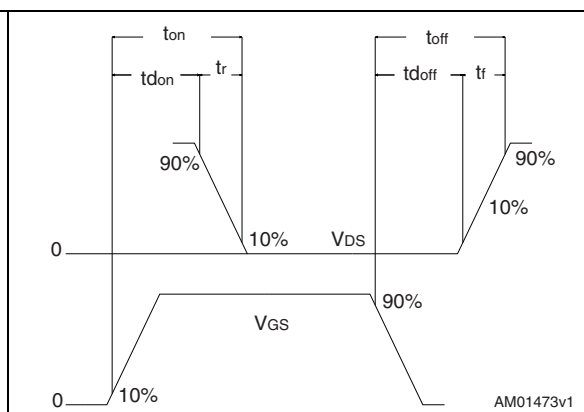


Figure 24. Switching time waveform



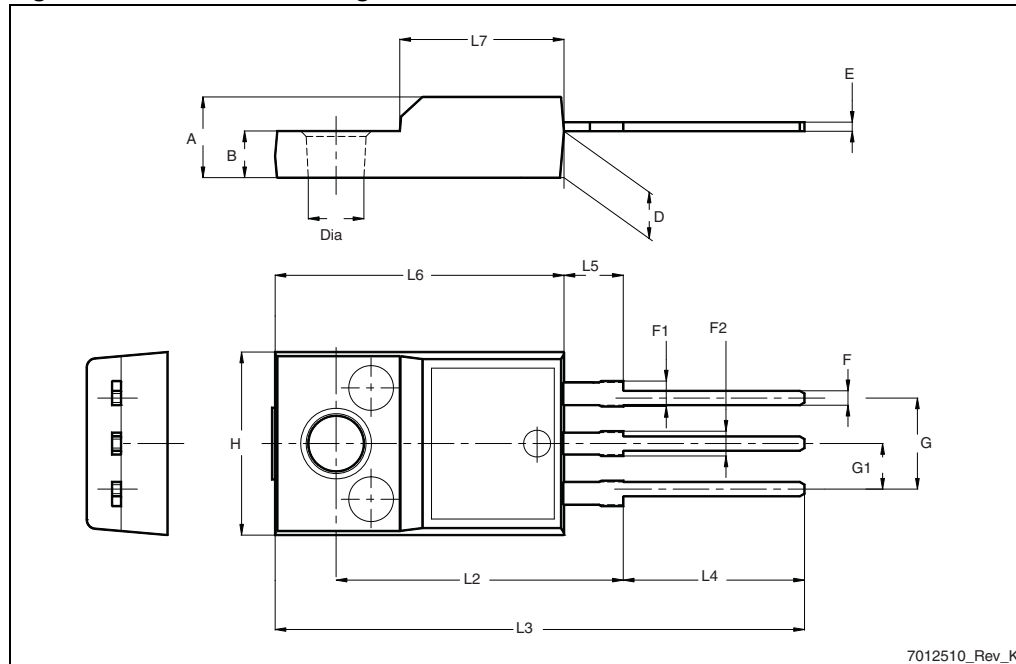
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

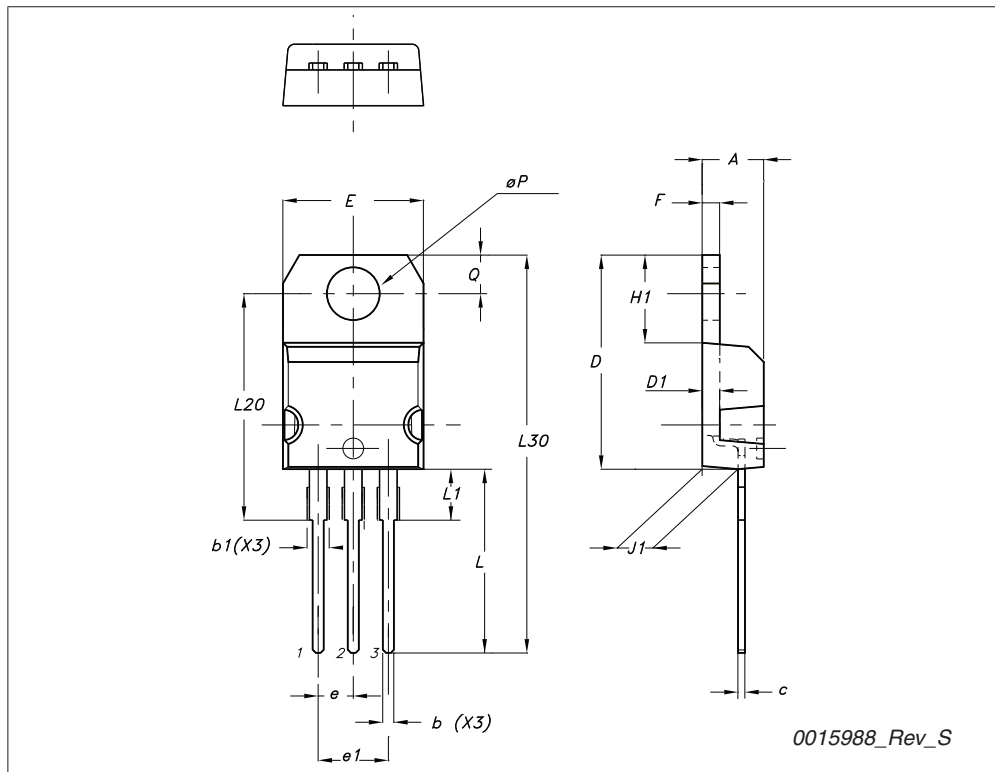
Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 25. TO-220FP drawing



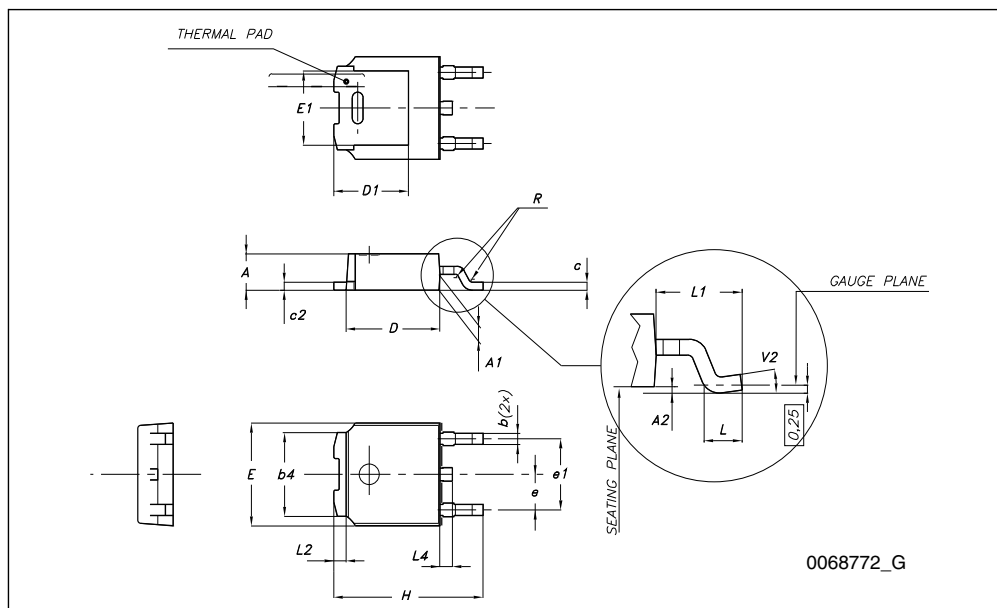
TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95



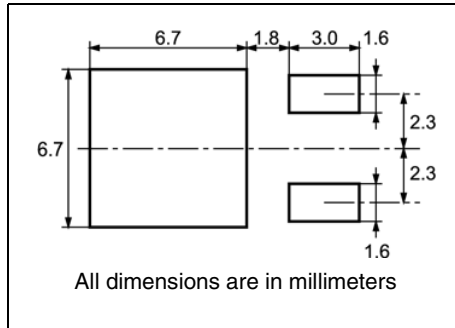
**TO-252 (DPAK) mechanical data**

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

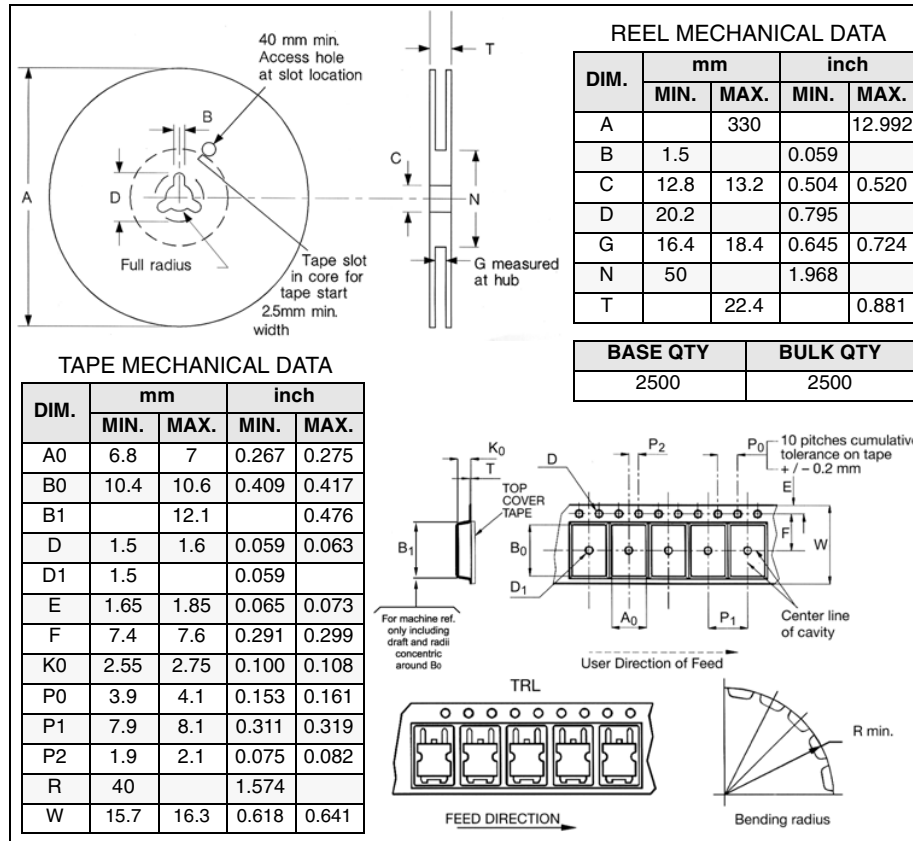


## 5 Package mechanical data

### DPAK FOOTPRINT



### TAPE AND REEL SHIPMENT



## 6 Revision history

Table 10. Document revision history

Date	Revision	Changes
09-Oct-2009	1	First release
20-Oct-2010	2	Document status promoted from preliminary data to datasheet

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