# N-Channel Power MOSFET 620 V, 0.98 $\Omega$ ,

#### **Features**

- Low ON Resistance
- Low Gate Charge
- 100% Avalanche Tested
- These Devices are Pb-Free and RoHS Compliant

#### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	NDF06N62Z	NDP06N62Z	Unit
Drain-to-Source Voltage	$V_{DSS}$	620		V
Continuous Drain Current $R_{\theta JC}$	I <sub>D</sub>	6.0 (Note 1)		Α
Continuous Drain Current $R_{\theta JC}$ , $T_A = 100^{\circ}C$	I <sub>D</sub>	3.8 (Note 1)		Α
Pulsed Drain Current, V <sub>GS</sub> @ 10 V	I <sub>DM</sub>	20 (Note 1)		Α
Power Dissipation $R_{\theta JC}$	$P_{D}$	31	113	W
Gate-to-Source Voltage	V <sub>GS</sub>	±3	30	٧
Single Pulse Avalanche Energy, I <sub>D</sub> = 6.0 A	E <sub>AS</sub>	113		mJ
ESD (HBM) (JESD 22-A114)	V <sub>esd</sub>	3000		٧
RMS Isolation Voltage (t = 0.3 sec., R.H. $\leq$ 30%, T <sub>A</sub> = 25°C) (Figure 14)	V <sub>ISO</sub>	4500	-	٧
Peak Diode Recovery	dv/dt	4.5 (Note 2)		V/ns
Continuous Source Current (Body Diode)	I <sub>S</sub>	6.0		Α
Maximum Temperature for Soldering Leads	T <sub>L</sub>	260		°C
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

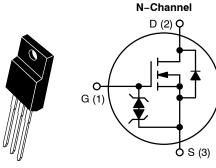
- 1. Limited by maximum junction temperature
- 2.  $I_{SD} = 6.0$  A,  $di/dt \le 100$  A/ $\mu$ s,  $V_{DD} \le BV_{DSS}$ ,  $T_J = +150$ °C



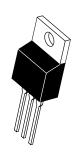
#### ON Semiconductor®

http://onsemi.com

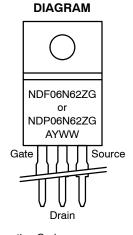
V <sub>DSS</sub>	R <sub>DS(ON)</sub> (TYP) @ 3 A		
620 V	0.98 Ω		



TO-220FP CASE 221D STYLE 1



TO-220AB CASE 221A STYLE 5



**MARKING** 

A = Location Code Y = Year WW = Work Week

## ORDERING INFORMATION

= Pb-Free Package

Device	Package	Shipping
NDF06N62ZG	TO-220FP (Pb-Free)	50 Units/Rail
NDP06N62ZG	TO-220AB (Pb-Free)	50 Units/Rail In Development

1

#### THERMAL RESISTANCE

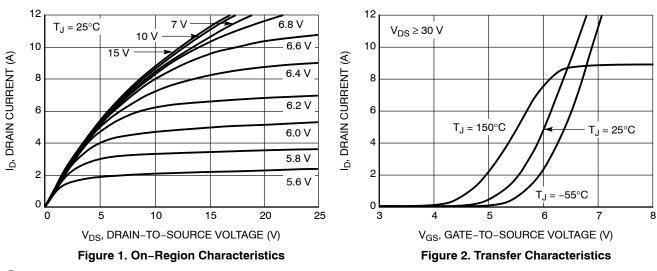
Parameter	Symbol	NDF06N62Z	NDP06N62Z	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	4.0	1.1	°C/W
Junction-to-Ambient Steady State (Note 3)	$R_{\theta JA}$	50	50	

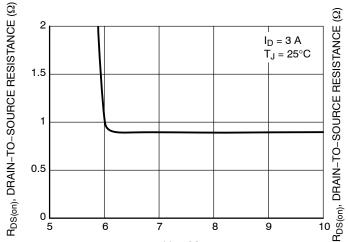
#### FLECTRICAL CHARACTERISTICS (T. - 25°C unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS		•			•	•
Drain-to-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	BV <sub>DSS</sub>	620			V
Breakdown Voltage Temperature Coefficient	Reference to 25°C, I <sub>D</sub> = 1 mA	$\Delta BV_{DSS}/$ $\Delta T_{J}$		0.6		V/°C
Drain-to-Source Leakage Current	$V_{DS} = 620 \text{ V}, V_{GS} = 0 \text{ V}$	°C I <sub>DSS</sub>			1 50	μΑ
Gate-to-Source Forward Leakage	V <sub>GS</sub> = ±20 V	I <sub>GSS</sub>			±10	μΑ
ON CHARACTERISTICS (Note 4)		•		•	•	
Static Drain-to-Source On-Resistance	$V_{GS}$ = 10 V, $I_{D}$ = 3.0 A	R <sub>DS(on)</sub>		0.98	1.2	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 100 \mu A$	V <sub>GS(th)</sub>	3.0		4.5	V
Forward Transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3.0 A	9 <sub>FS</sub>		5.0		S
DYNAMIC CHARACTERISTICS						
Input Capacitance		C <sub>iss</sub>		923		pF
Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0  MHz	C <sub>oss</sub>		106		
Reverse Transfer Capacitance		C <sub>rss</sub>		23		
Total Gate Charge		Qg		32		nC
Gate-to-Source Charge	V <sub>DD</sub> = 310 V, I <sub>D</sub> = 6.0 A,	Q <sub>gs</sub>		6.3		
Gate-to-Drain ("Miller") Charge	V <sub>GS</sub> = 10 V	Q <sub>gd</sub>		17		
Plateau Voltage		V <sub>gp</sub>		6.3		V
Gate Resistance		R <sub>g</sub>		3.2		Ω
RESISTIVE SWITCHING CHARACTER	ISTICS					
Turn-On Delay Time		t <sub>d(on)</sub>		13		ns
Rise Time	$V_{DD} = 310 \text{ V}, I_D = 6.0 \text{ A},$	t <sub>r</sub>		19		
Turn-Off Delay Time	$V_{GS}$ = 10 V, $R_{G}$ = 5 $\Omega$	t <sub>d(off)</sub>		32		
Fall Time		t <sub>f</sub>		28		
SOURCE-DRAIN DIODE CHARACTER	RISTICS (T <sub>C</sub> = 25°C unless otherwis	e noted)				
Diode Forward Voltage	I <sub>S</sub> = 6.0 A, V <sub>GS</sub> = 0 V	V <sub>SD</sub>			1.6	V
Reverse Recovery Time	V <sub>GS</sub> = 0 V, V <sub>DD</sub> = 30 V	t <sub>rr</sub>		338		ns
Reverse Recovery Charge	$I_S = 6.0 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$	Q <sub>rr</sub>		2.0		μC

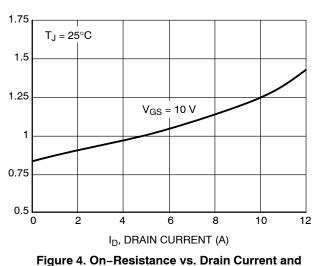
Insertion mounted
 Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%.

#### TYPICAL CHARACTERISTICS





 $V_{GS}(V)$ Figure 3. On-Resistance vs. V<sub>GS</sub>



**Gate Voltage**  $I_D = 1 \text{ mA}$ 

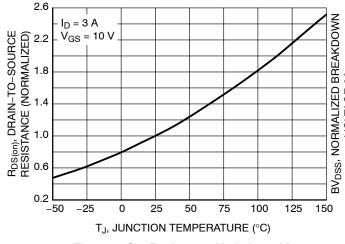


Figure 5. On-Resistance Variation with **Temperature** 

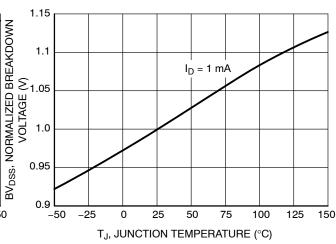


Figure 6. BVDSS Variation with Temperature

#### **TYPICAL CHARACTERISTICS**

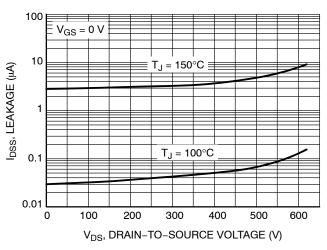


Figure 7. Drain-to-Source Leakage Current vs. Voltage

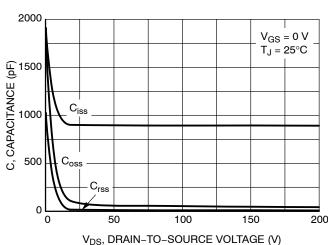


Figure 8. Capacitance Variation

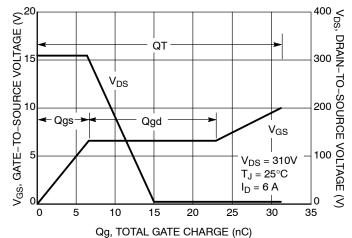


Figure 9. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

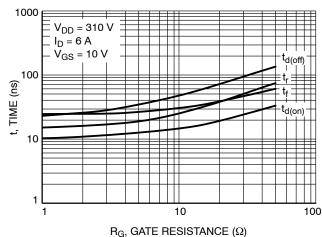


Figure 10. Resistive Switching Time Variation vs. Gate Resistance

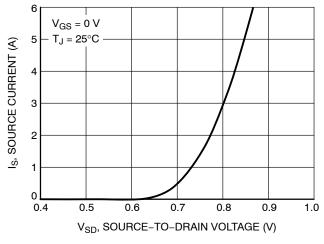


Figure 11. Diode Forward Voltage vs. Current

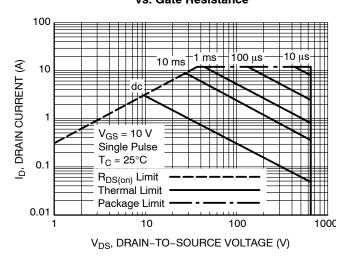


Figure 12. Maximum Rated Forward Biased Safe Operating Area for NDF06N62Z

#### **TYPICAL CHARACTERISTICS**

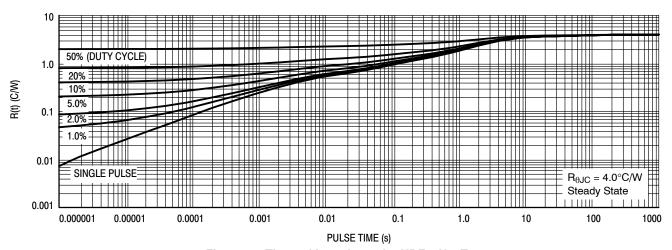


Figure 13. Thermal Impedance for NDF06N62Z

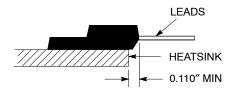


Figure 14. Isolation Test Diagram

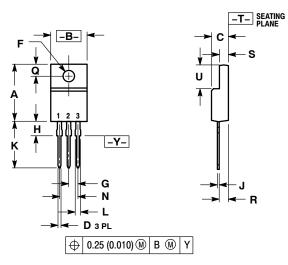
Measurement made between leads and heatsink with all leads shorted together.

\*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

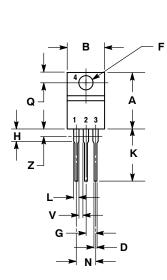
#### PACKAGE DIMENSIONS

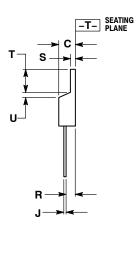
#### TO-220 FULLPAK

CASE 221D-03 **ISSUE J** 



TO-220AB CASE 221A-09 **ISSUE AE** 





#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH
- 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.617	0.635	15.67	16.12
В	0.392	0.419	9.96	10.63
С	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
Н	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200	0.200 BSC		BSC
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

STYLE 1:

PIN 1. GATE 2. DRAIN

SOURCE

- 1. DIMENSIONING AND TOLERANCING PER ANSI
- CONTROLLING DIMENSION: INCH.
  DIMENSION Z DEFINES A ZONE WHERE ALL
  BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
С	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
Н	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
٧	0.045		1.15	
Z		0.080		2.04

STYLE 5: PIN 1.

2.

GATE DRAIN

SOURCE DRAIN

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