



COMPLEMENTARY N-CHANNEL AND P-CHANNEL MOSFET

GENERAL DESCRIPTION

The ALD1115 is a monolithic complementary N-channel and P-channel transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process. It consists of a N-channel MOSFET and a P-channel MOSFET in one package. The ALD1115 is a dual version of the quad complementary ALD1105.

The ALD1115 offers high input impedance and negative current temperature coefficient. The transistor pair is designed for precision signal switching and amplifying applications in +1V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. When connected in parallel with sources, drains and gates connected together, a CMOS analog switch can be constructed. In addition, the ALD1115 is intended as a building block for CMOS inverters, differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1115 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the field effect transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 30pA at room temperature. V+ is connected to the substrate, which is the most positive voltage potential of the ALD1115, usually SP(5). Similarly, V- is connected to the most negative voltage potential of the ALD1115, usually SN (1).

FEATURES

- Thermal tracking between N-channel and P-channel
- Low threshold voltage of 0.7V for both N-channel and P-channel MOSFETs
- Low input capacitance
- High input impedance -- $10^{13}\Omega$ typical
- Low input and output leakage currents
- Negative current (I_{DS}) temperature coefficient
- Enhancement mode (normally off)
- DC current gain 10^9
- Single N-channel MOSFET and single P-channel MOSFET in one package

ORDERING INFORMATION ("L" suffix for lead free version)

Operating Temperature Range*			
-55°C to +125°C	0°C to +70°C	0°C to +70°C	0°C to +70°C
8-Pin CERDIP Package	8-Pin MSOP Package	8-Pin Plastic Dip Package	8-Pin SOIC Package
ALD1115 DA	ALD1115 MAL	ALD1115 PA ALD1115PAL	ALD1115 SA ALD1115 SAL

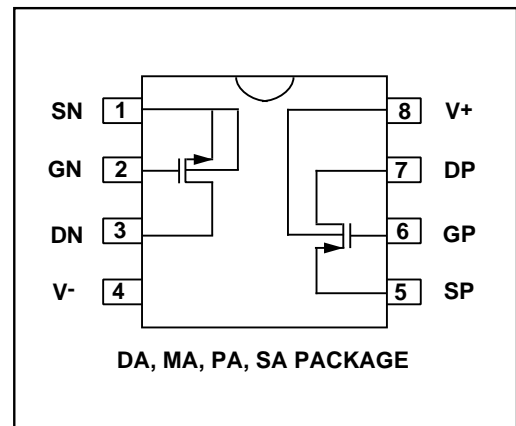
* Contact factory for industrial temperature range.

© 2006 Advanced Linear Devices, Inc. 415 Tasman Drive, Sunnyvale, California 94089 -1706 Tel: (408) 747-1155 Fax: (408) 747-1286 <http://www.aldinc.com>

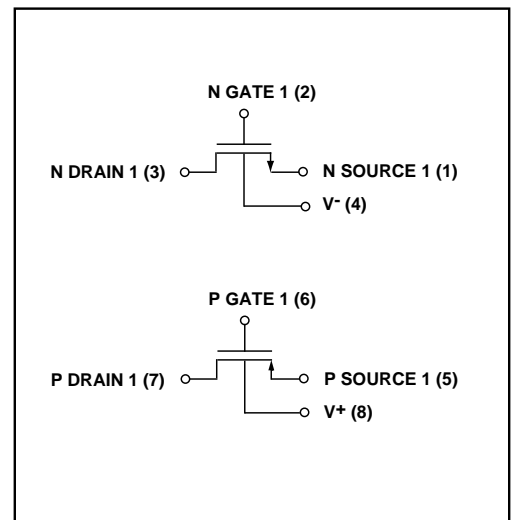
APPLICATIONS

- Precision current mirrors
- Complementary push-pull linear drives
- Discrete analog switches
- Analog signal choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog current inverter
- Precision matched current sources
- CMOS inverter stage
- Diode clamps
- Source followers

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Drain-source voltage, V_{DS}	_____	13.2V
Gate-source voltage, V_{GS}	_____	13.2V
Power dissipation	_____	500 mW
Operating temperature range	PA, SA package _____	0°C to +70°C
	DA package _____	-55°C to +125°C
Storage temperature range	_____	-65°C to +150°C
Lead temperature, 10 seconds	_____	+260°C

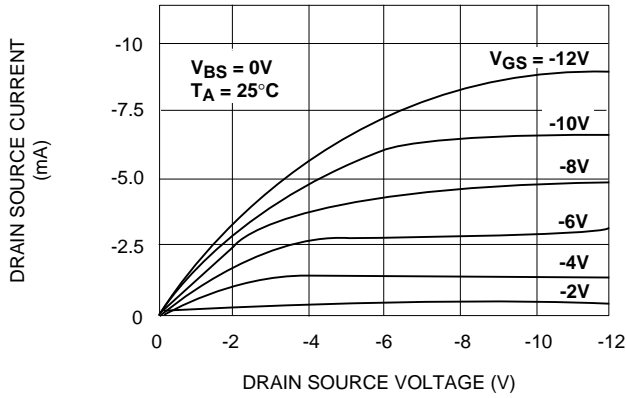
OPERATING ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ unless otherwise specified

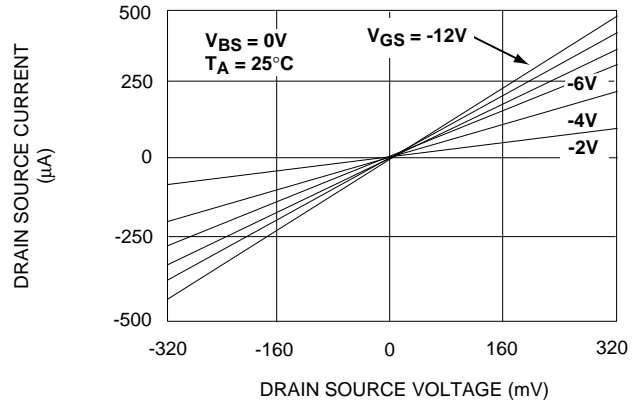
Parameter	Symbol	N - Channel			Unit	Test Conditions	P - Channel			Unit	Test Conditions
		Min	Typ	Max			Min	Typ	Max		
Gate Threshold Voltage	V_T	0.4	0.7	1.0	V	$I_{DS} = 1\mu\text{A}$ $V_{GS} = V_{DS}$	-0.4	-0.7	-1.0	V	$I_{DS} = -1\mu\text{A}$ $V_{GS} = V_{DS}$
Gate Threshold Temperature Drift	TC_{VT}		-1.2		mV/°C			-1.3		mV/°C	
On Drain Current	$I_{DS(ON)}$	3	4.8		mA	$V_{GS} = V_{DS} = 5\text{V}$	-1.3	-2		mA	$V_{GS} = V_{DS} = -5\text{V}$
Trans-conductance	G_{fs}	1	1.8		mmho	$V_{DS} = 5\text{V}$ $I_{DS} = 10\text{mA}$	0.25	0.67		mmho	$V_{DS} = -5\text{V}$ $I_{DS} = -10\text{mA}$
Output Conductance	G_{OS}		200		μmho	$V_{DS} = 5\text{V}$ $I_{DS} = 10\text{mA}$		40		μmho	$V_{DS} = -5\text{V}$ $I_{DS} = -10\text{mA}$
Drain Source ON Resistance	$R_{DS(ON)}$		350	500	Ω	$V_{DS} = 0.1\text{V}$ $V_{GS} = 5\text{V}$		1200	1800	Ω	$V_{DS} = -0.1\text{V}$ $V_{GS} = -5\text{V}$
Drain Source Breakdown Voltage	BV_{DSS}	12			V	$I_{DS} = 1\mu\text{A}$ $V_{GS} = 0\text{V}$	-12			V	$I_{DS} = -1\mu\text{A}$ $V_{GS} = 0\text{V}$
Off Drain Current	$I_{DS(OFF)}$		10	400	pA nA	$V_{DS} = 12\text{V}$ $I_{GS} = 0\text{V}$ $T_A = 125^\circ\text{C}$		10	400	pA nA	$V_{DS} = -12\text{V}$ $V_{GS} = 0\text{V}$ $T_A = 125^\circ\text{C}$
Gate Leakage Current	I_{GSS}		0.1	30	pA nA	$V_{DS} = 0\text{V}$ $V_{GS} = 12\text{V}$ $T_A = 125^\circ\text{C}$		1	30	pA nA	$V_{DS} = 0\text{V}$ $V_{GS} = -12\text{V}$ $T_A = 125^\circ\text{C}$
Input Capacitance	C_{ISS}		1	3	pF			1	3	pF	

P- CHANNEL TYPICAL PERFORMANCE CHARACTERISTICS

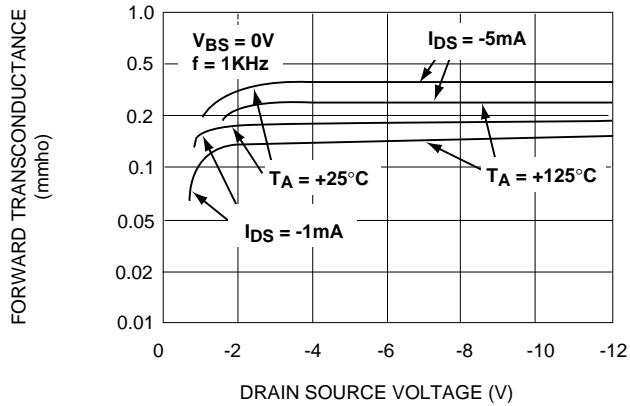
OUTPUT CHARACTERISTICS



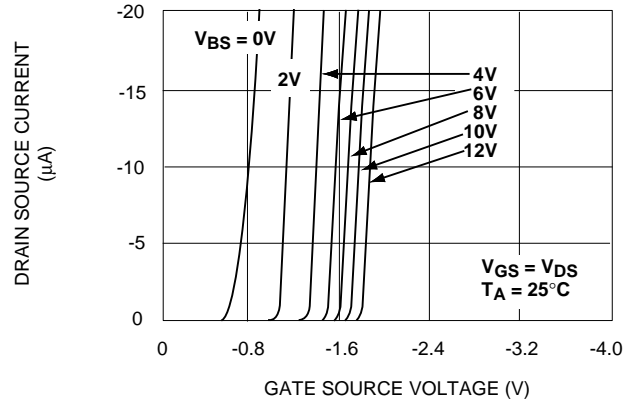
LOW VOLTAGE OUTPUT CHARACTERISTICS



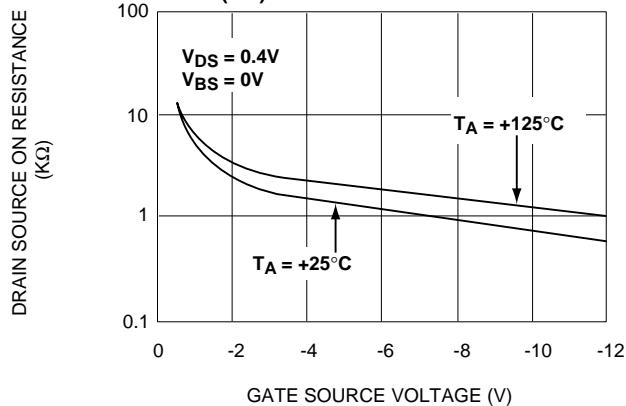
FORWARD TRANSCONDUCTANCE vs. DRAIN SOURCE VOLTAGE



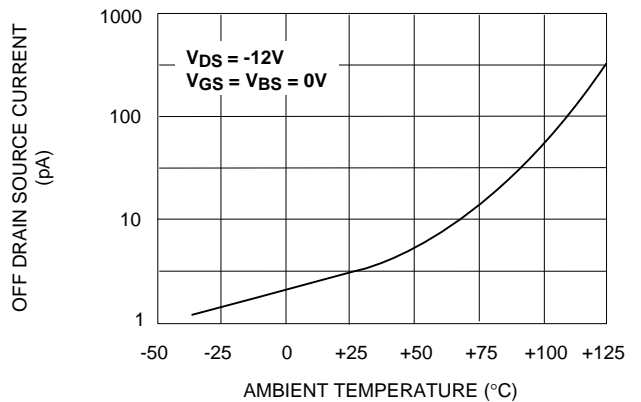
TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



DRAIN SOURCE ON RESISTANCE RDS (ON) vs. GATE SOURCE VOLTAGE

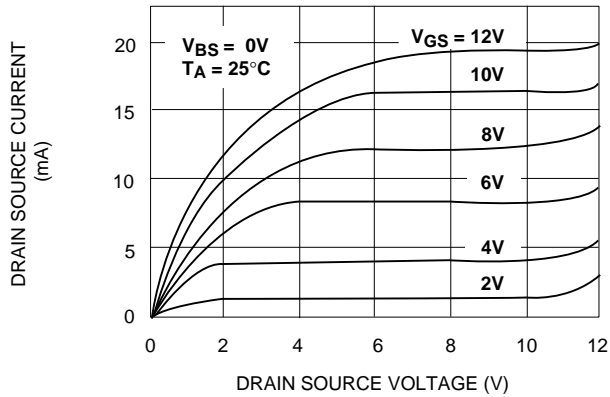


OFF DRAIN CURRENT vs. AMBIENT TEMPERATURE

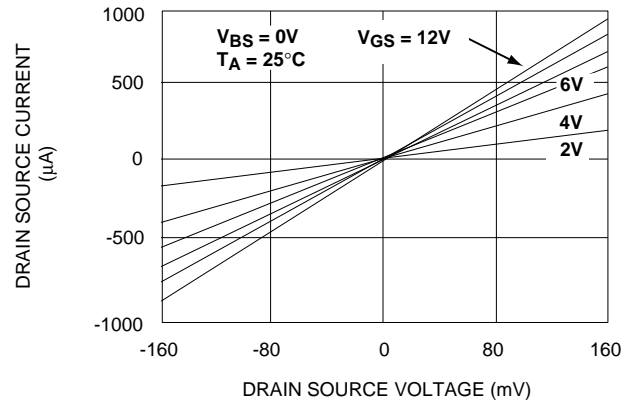


N- CHANNEL TYPICAL PERFORMANCE CHARACTERISTICS

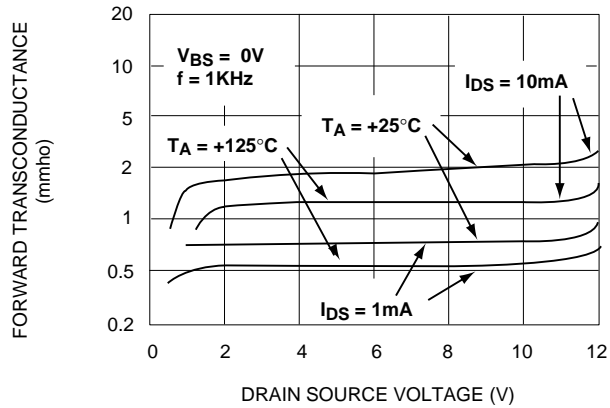
OUTPUT CHARACTERISTICS



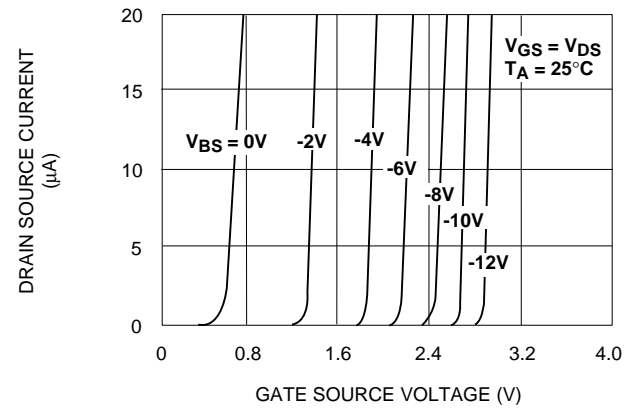
LOW VOLTAGE OUTPUT CHARACTERISTICS



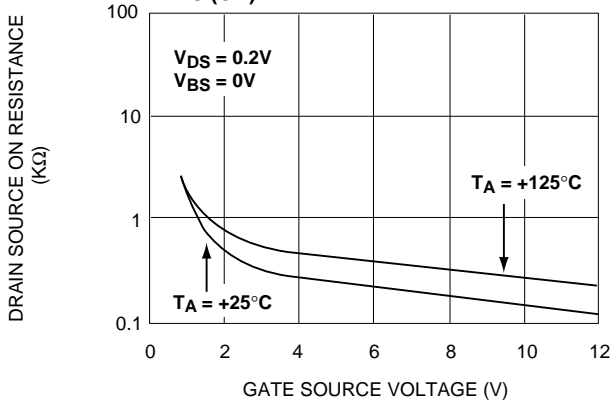
FORWARD TRANSCONDUCTANCE vs. DRAIN SOURCE VOLTAGE



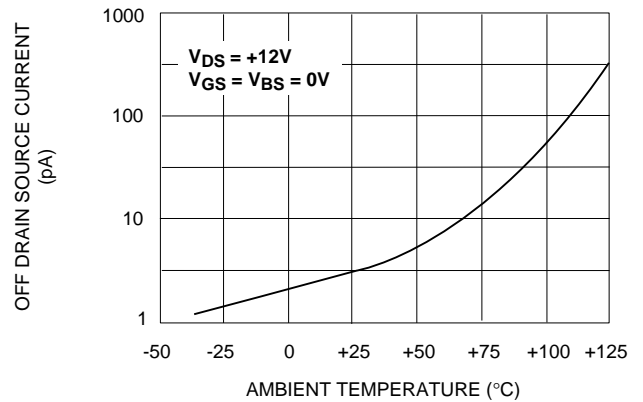
TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



DRAIN SOURCE ON RESISTANCE RDS(ON) vs. GATE SOURCE VOLTAGE

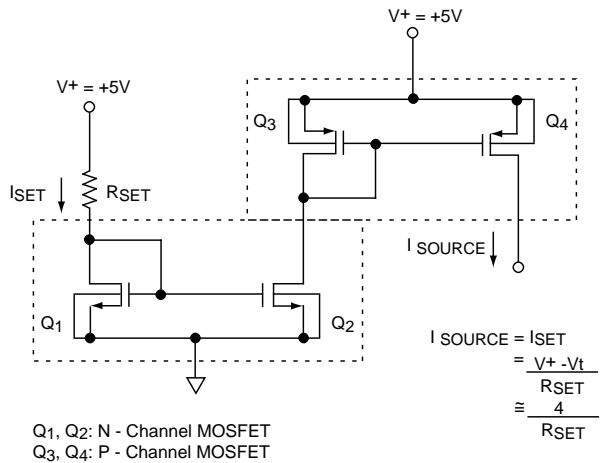


OFF DRAIN CURRENT vs. AMBIENT TEMPERATURE

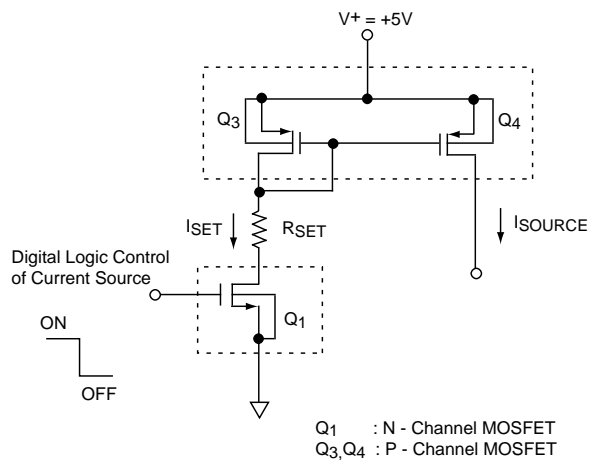


TYPICAL APPLICATIONS

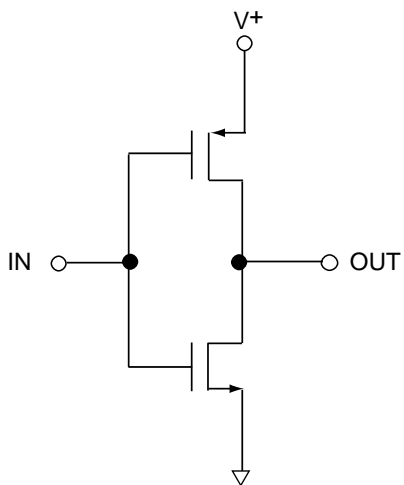
CURRENT SOURCE MIRROR



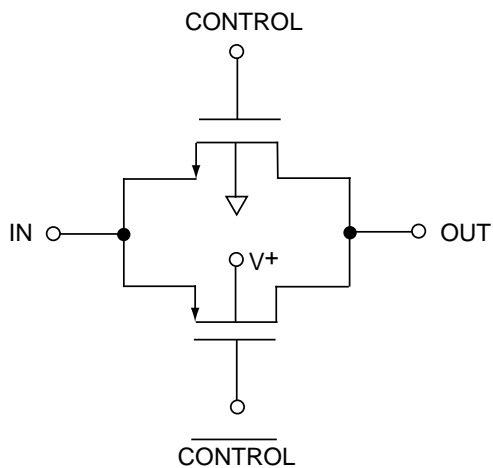
CURRENT SOURCE WITH GATE CONTROL



CMOS INVERTER

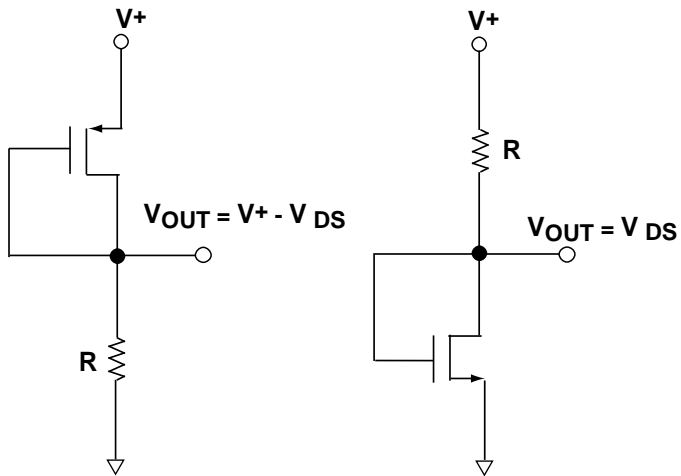


CMOS ANALOG SWITCH

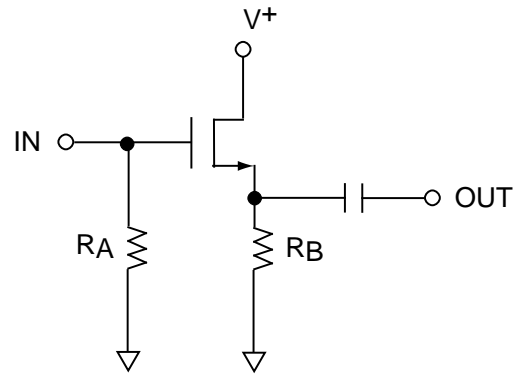


TYPICAL APPLICATIONS

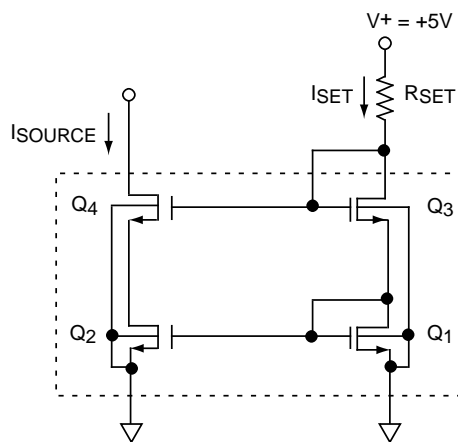
DIODE-CONNECTED CONFIGURATION



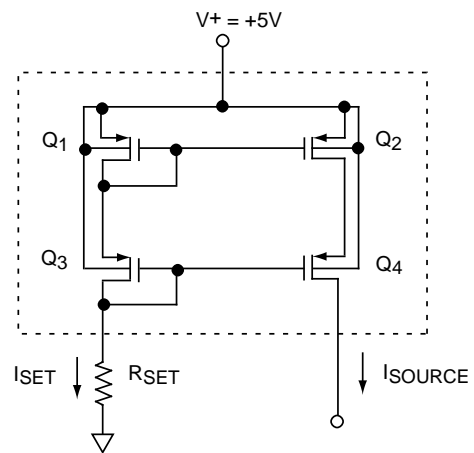
SOURCE FOLLOWER



CASCODE CURRENT SOURCES



Q1, Q2, Q3, Q4: N - Channel MOSFET



$$I_{SOURCE} = I_{SET} = \frac{V^+ - 2V_t}{R_{SET}} \approx \frac{3}{R_{SET}}$$

Q1, Q2, Q3, Q4: P - Channel MOSFET