CPA2512 Series
Chip Power Resistors

Using the Thermal Performance Plots

SUSUMU CO., LTD.

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A thermal performance plot is a detailed derating curve that accounts for the board/heat-sink interface in addition to the ambient/heat-sink temperature. A standard derating curve only accounts for the ambient/heat-sink temperature and therefore must assume a specific rate of heat flow from the chip power resistor (usually an absolute best case scenario), which can be very misleading considering the wide variety of board design and construction limitations that can push the effective thermal resistance of the board/heat-sink interface far from the best case scenario.

The thermal performance plots provide a means of identifying the recommended maximum power rating based on the maximum acceptable peak temperature rise and effective thermal resistance of the board/heat-sink interface. In addition, it provides a board design engineer perspective on the potential for improving the thermal characteristics of an existing board/heat-sink interface to enable higher power handling capability.

If the effective thermal resistance between the chip power resistor and board/heat-sink interface is known, then the recommended maximum power rating would be determined as follows.

1. Calculate the maximum "peak surface temperature rise", $T_{rp} = T_{uc} - T_{ma}$ (°C)

   Where T_{uc} = upper category temperature (generally 155°C) and T_{ma} = maximum ambient/heat-sink temperature at 100% rated power. 155°C is a comfortable limit for the CP series chip power resistors in determining the desired power rating. Though, the CP series chip power resistors can tolerate a continuous 190°C and greater peak surface temperature and still meet the criteria for Life testing as detailed in the environmental performance specifications section of the datasheets. Using a T_{uc} = 155°C for this determination offers a comfortable safeguard against uncertainties.

2. Draw a horizontal line across the plot at the maximum "peak surface temperature rise" determined in step 1.
3. Draw a vertical line up the plot at the known "thermal resistance of board"/heat-sink interface.
4. The intersection of these two lines is the recommended maximum power rating (refer to Plot 1 for example).

If the effective thermal resistance is not known, it can be determined by measuring the peak surface temperature rise of a chip power resistor as a function of power and comparing the result with the corresponding thermal performance plot as follows.

1. Same as step 1 in previous section.
2. With the selected chip power resistor mounted to the intended board/heat-sink interface, record the surface temperature at 0W applied power.

   Use a thermal imaging camera (blacken marking with sharpie pen) or a thermocouple thermally secured to the surface for measuring temperature. The 0W temperature can be room temperature or regulated at T_{ma} to account for slight thermal conductivity reduction of materials with increasing temperature (not to be confused with power vs. T_{rp} non-linearity).

3. Increase the power until the peak surface temperature at equilibrium has been raised by the amount determined in step 1 and record the power level. This would be the power rating determined for you application for that particular board/heat-sink interface.

   Depending on the 0W temperature the target peak surface temperature may be T_{uc} (for 0W regulated at T_{ma}) or room temperature + T_{rp}.

4. Draw a horizontal line across the plot at the maximum "peak surface temperature rise" determined in step 1. Where this line intersects the power level determined in step 3, draw a line straight down to identify the effective thermal resistance of the board/heat-sink interface (refer to Plot 1 for example).

Knowing the effective thermal resistance of the board/heat-sink interface enables identifying the most appropriate part. If the particular part you tested with does not quite meet your needs, consider the BeO or AlN material options, a larger chip size or alternative electrode configuration. Else, this may offer some perspective on the potential for improving, or how much improvement is needed to the thermal characteristics of the board/heat-sink interface.

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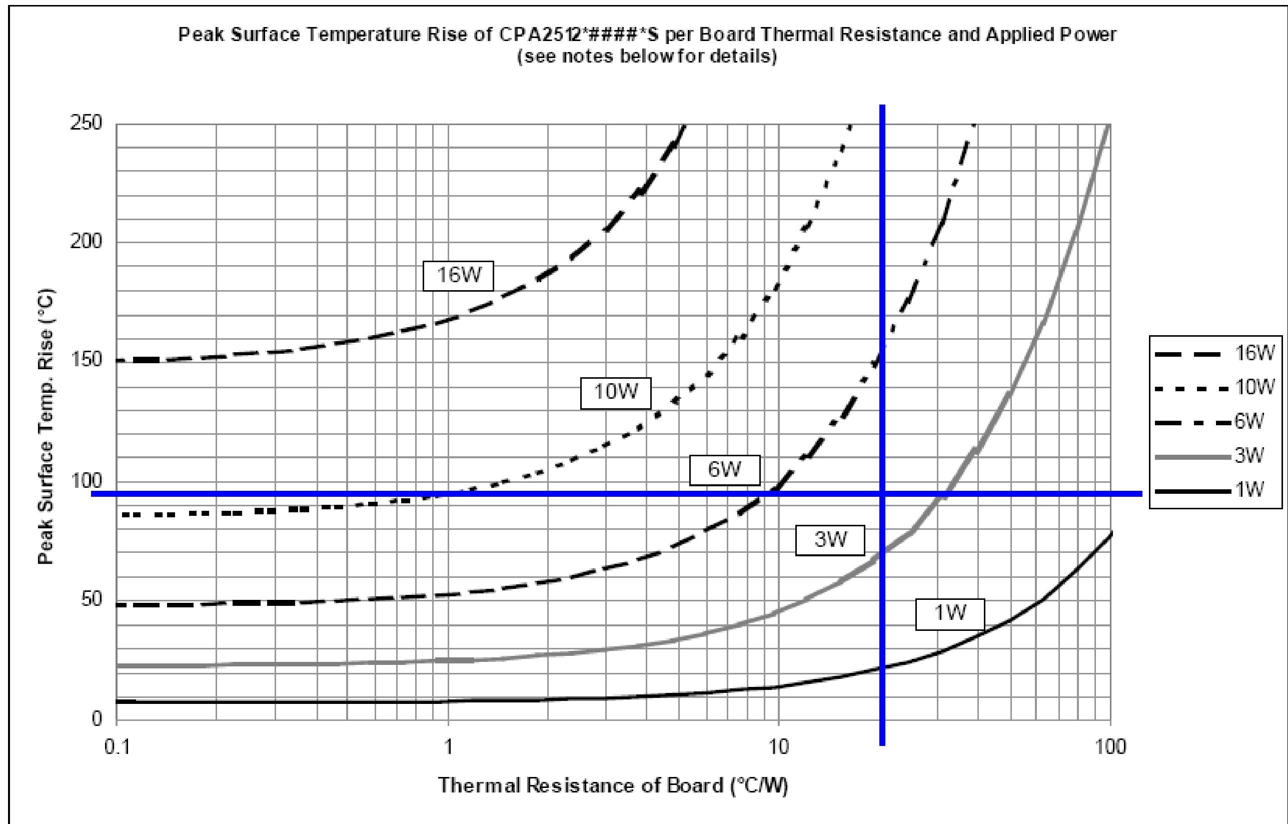
Plot 1: Example thermal performance plot taken from CPA2512*####*S datasheet.



Example Details: $T_{uc} = 155°C$, $T_{ma} = 60°C$, $R_T = 20°C/W$, $P_R = 4W$

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