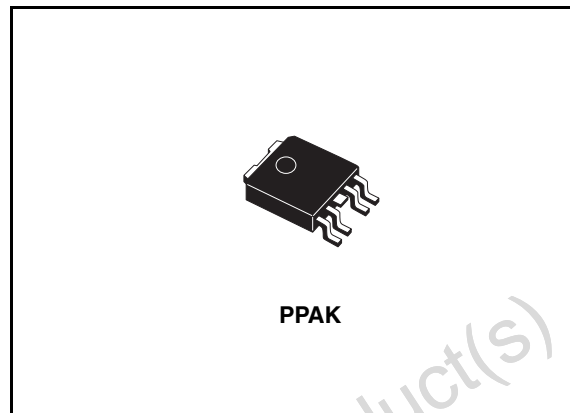


Very low drop dual voltage regulator

**Features**

- Output current 1 up to 500 mA
- Output current 2 up to 1.0 A
- Low dropout voltage 1 (0.3 V @  $I_O = 500$  mA)
- Low dropout voltage 2 (0.4 V @  $I_O = 1$  A)
- Very low supply current (typ. 50  $\mu$ A in OFF mode, 1.6 mA max in ON mode)
- Logic-controlled electronic shutdown output voltage availability for each regulator: 1.8 V, 2.5 V, 3.3 V
- Internal current and thermal limit
- Stable with low value (min. 4.7  $\mu$ F) and low ESR output capacitors
- Supply voltage rejection: 70 dB (typ.)
- Temperature range (- 40 °C to 125 °C)



**Description**

The LDR1833, LDR2533 is a very low drop dual voltage regulator available in PPAK. The very low drop-voltage (0.5 V) and the very low supply current make it particularly suitable for low noise and low power applications such as PDA, Microdrive and other data storage applications while the used high voltage technology makes this device suitable for consumer applications such as Monitors and Set-top-box. For each  $V_O$  a shutdown logic control function is available (TTL compatible) to decrease the total power consumption.

**Table 1. Device summary**

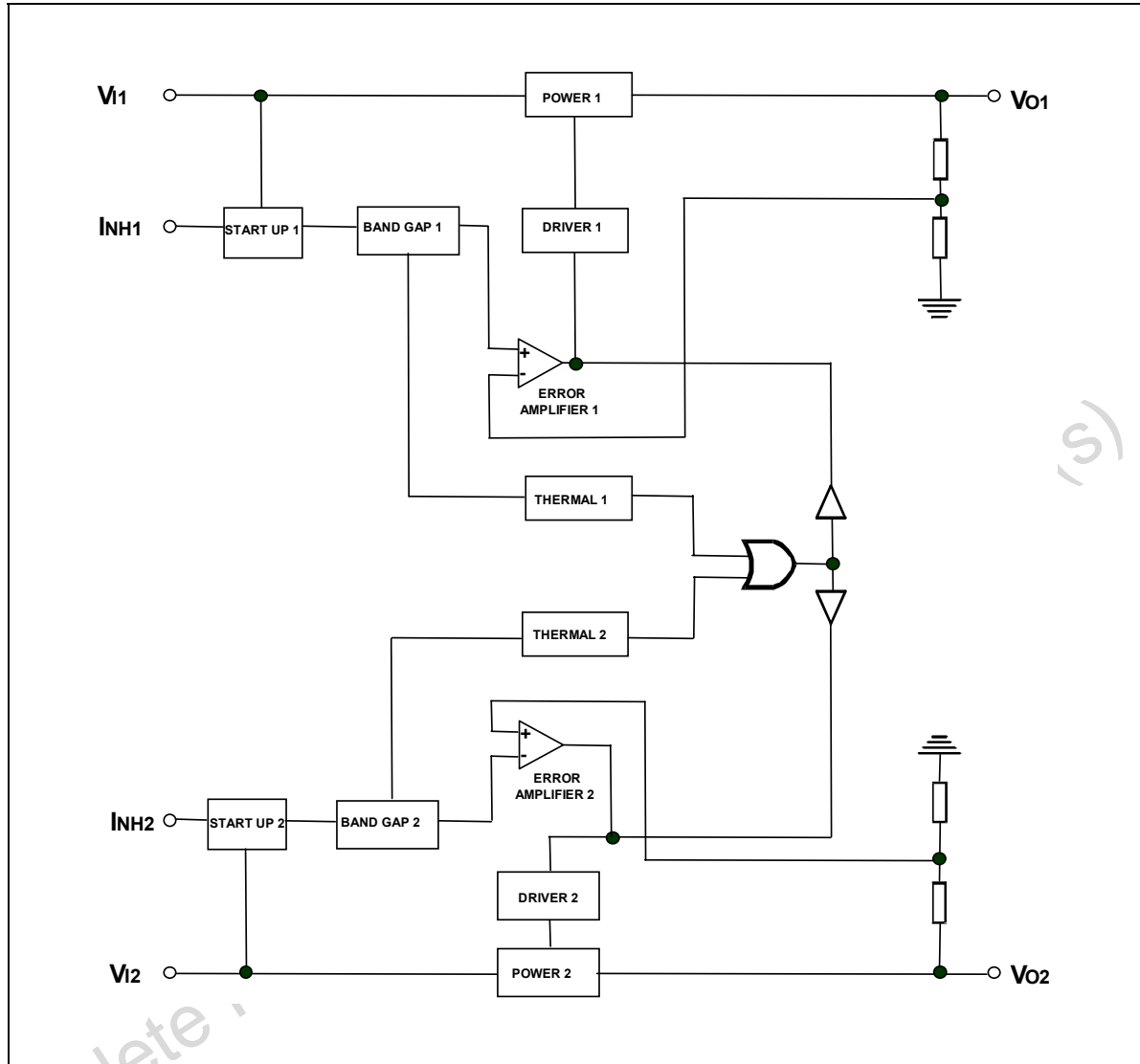
Order codes	Output voltages	
	$V_{O1}$	$V_{O2}$
LDR1833PT-R	1.8 V	3.3 V
LDR2533PT-R	2.5 V	3.3 V

## Contents

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# 1 Diagram

Figure 1. Block diagram



## 2 Pin configuration

Figure 2. Pin connections (top view)

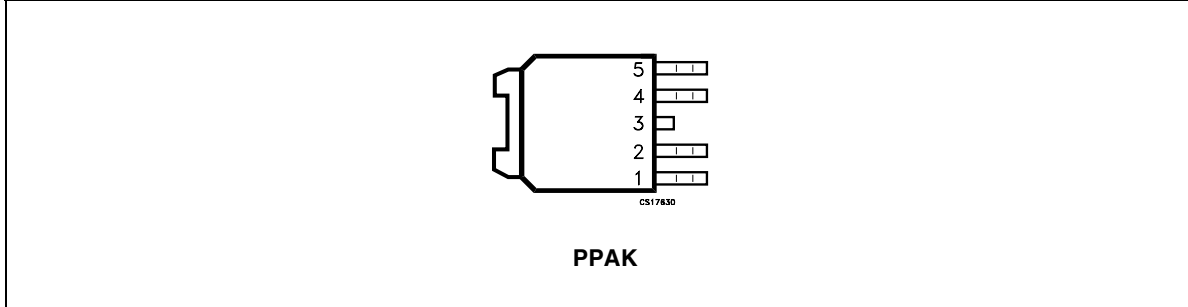


Table 2. Pin description

Pin n°	Symbol	Name and function
3	GND	Ground pin
2	$V_{I1}$	Input 1 supply pin. Bypass with a 2.2 $\mu$ F capacitor to GND
1	$V_{I2}$	Input 2 supply pin. Bypass with a 2.2 $\mu$ F capacitor to GND
4	$V_{O1}$	Output 1 pin. Bypass with a 4.7 $\mu$ F capacitor to GND port
5	$V_{O2}$	Output 2 pin. Bypass with a 4.7 $\mu$ F capacitor to GND port

### 3 Maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{I1}$ & $V_{I2}$	DC input voltage	-0.3 to 15	V
INH	Shutdown voltage	-0.3 to 15	V
$I_O$	Output current	Internally limited	
$P_D$	Power dissipation	Internally limited	
$T_{STG}$	Storage temperature range	-50 to +150	°C
$T_A$	Operating ambient temperature range	-40 to +125	°C

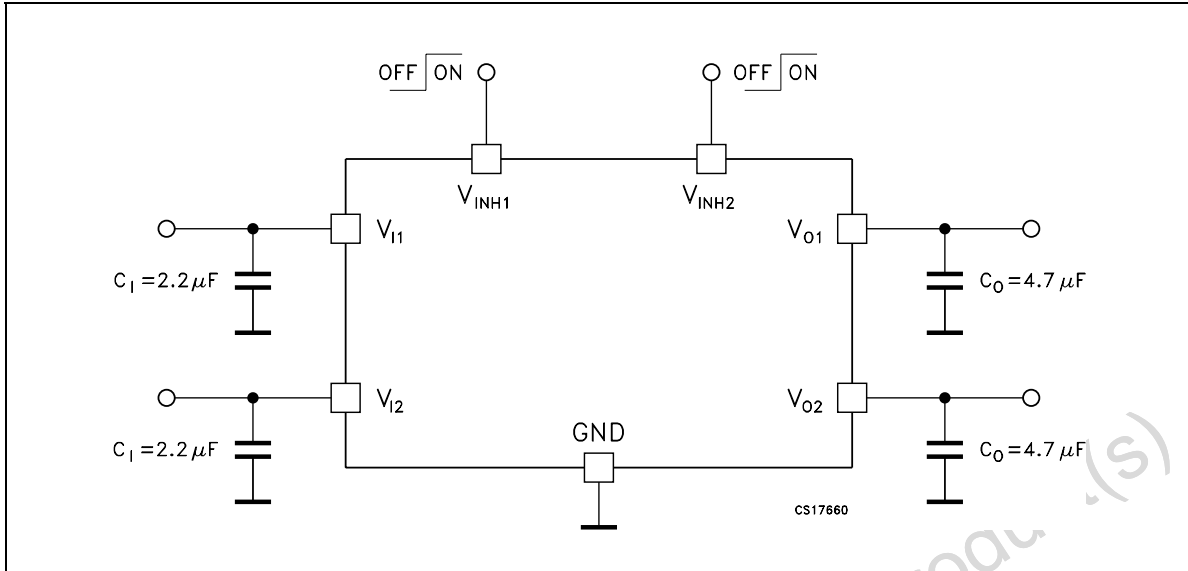
*Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.*

**Table 4. Thermal data**

Symbol	Parameter	PPAK	Unit
$R_{thJC}$	Thermal resistance junction-case	8	°C/W

## 4 Typical application

Figure 3. Typical application circuit



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## 5 Electrical characteristics

**Table 5. Electrical characteristics** ( $V_{I1} = V_{O1} + 2\text{ V}$ ,  $V_{I2} = V_{O2} + 2\text{ V}$ ,  $V_{INH1} = V_{INH2} = 2.5\text{ V}$ ,  $C_{11,2} = 2.2\text{ }\mu\text{F}$ ,  $C_{O1,2} = 4.7\text{ }\mu\text{F}$ ,  $I_{O1} = I_{O2} = 10\text{ mA}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$ , unless otherwise specified. Typical values are referred at  $T_A = 25\text{ }^\circ\text{C}$ )

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{O1}$	Output voltage 1		-5	$V_{NOM1}$	+5	%V
$V_{O2}$	Output voltage 2		-5	$V_{NOM2}$	+5	%V
$V_{DROP1}$	Dropout voltage 1 <sup>(1)</sup>	$I_{O1} = 500\text{ mA}$		0.3	0.7	V
$V_{DROP2}$	Dropout voltage 2 <sup>(1)</sup>	$I_{O2} = 1\text{ A}$		0.4	0.8	V
$\Delta V_{O1}$	Line regulation 1	$V_{I1} = V_{O1} + 2\text{ V}$ to $V_{O1} + 7\text{ V}$ , $I_O = 250\text{ mA}$		15	30	mV
$\Delta V_{O2}$	Line regulation 2	$V_{I2} = V_{O2} + 2\text{ V}$ to $V_{O2} + 7\text{ V}$ , $I_O = 500\text{ mA}$		15	40	mV
$\Delta V_{O1}$	Load regulation 1	$V_{I1} = V_{O1} + 2\text{ V}$ , $I_{O1} = 10$ to $500\text{ mA}$		10		mV
$\Delta V_{O2}$	Load regulation 2	$V_{I2} = V_{O2} + 2\text{ V}$ , $I_{O2} = 10\text{ mA}$ to $1\text{ A}$		60		mV
$I_{STOT}$	Total supply current	$I_{O1} = I_{O2} = \text{NO LOAD}$		2		mA
$I_S$	1 channel supply current	NO LOAD		1		mA
$I_{QMAX}$	Quiescent current	$I_{O1} = 500\text{ mA}$ , $I_{O2} = 1\text{ A}$		30		mA
$I_{SC1}$	Short circuit current 1	$T_A = 25^\circ$	500	800		mA
$I_{SC2}$	Short circuit current 2	$T_A = 25^\circ$	1	1.6		A
$V_{INH-H}$	Enable voltage HIGH		2.4			V
$V_{INH-L}$	Enable voltage LOW				0.8	V
$I_{INH}$	Enable pin current	$V_{INH} = 5\text{ V}$		6		$\mu\text{A}$
SVR	Supply voltage rejection <sup>(2)</sup>	$V_{I1,2} = V_{O1,2} + 3\text{ V} \pm 1\text{ V}$ , $I_{O1,2} = 10\text{ mA}$ , $f = 120\text{ Hz}$		70		dB
$e_N$	RMS output noise <sup>(2)</sup>	Bandwidth of 10Hz to 100kHz		0.003		% $V_O$

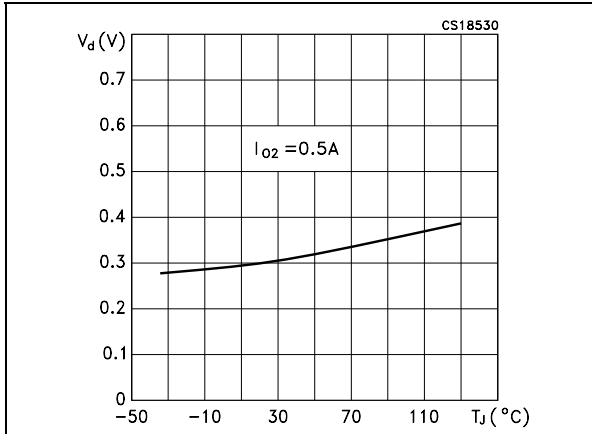
1. This test is not performed for  $V_O < 2.5\text{ V}$ .

2. Guaranteed by design, but not tested in production

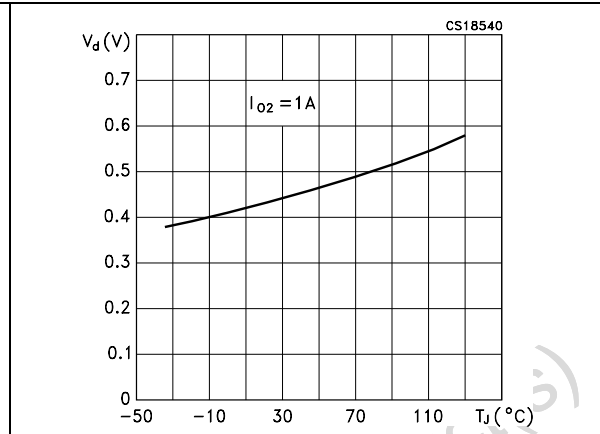
## 6 Typical characteristics

(unless otherwise specified  $T_J = 25\text{ }^\circ\text{C}$ )

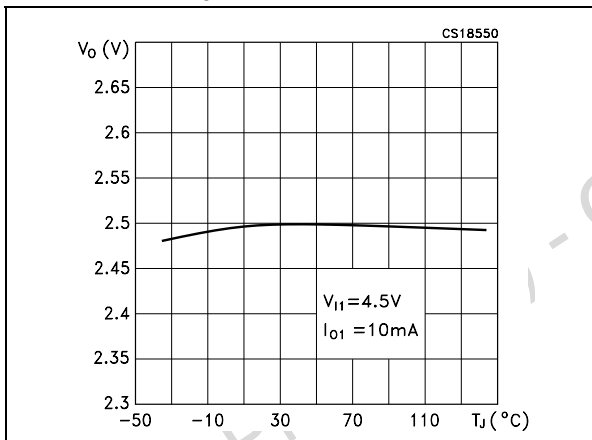
**Figure 4. Dropout voltage ( $V_{O1}$ ) vs temperature**



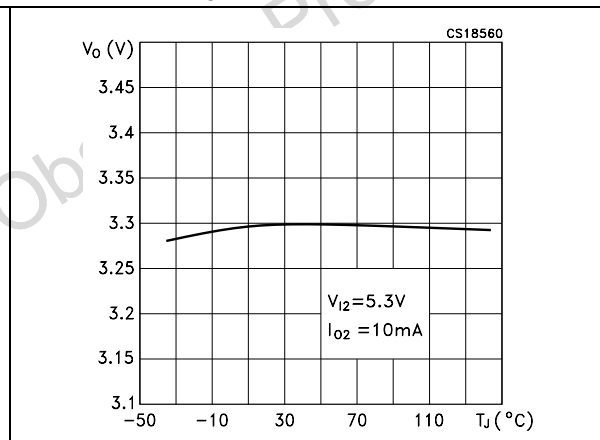
**Figure 5. Dropout voltage ( $V_{O2}$ ) vs temperature**



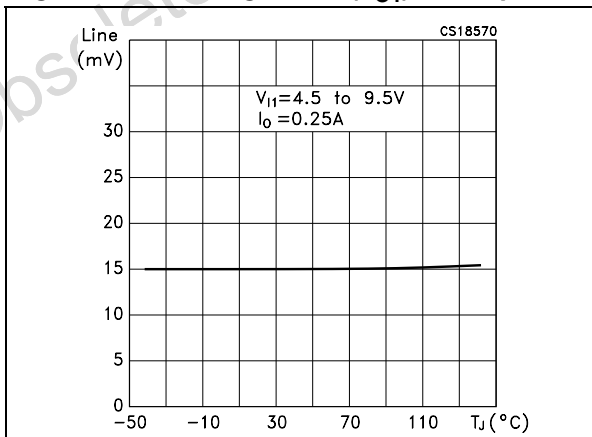
**Figure 6. Dropout voltage ( $V_{O1}$ ) vs temperature**



**Figure 7. Dropout voltage ( $V_{O2}$ ) vs temperature**



**Figure 8. Line regulation ( $V_{O1}$ ) vs temp.**



**Figure 9. Load regulation ( $V_{O1}$ ) vs temp.**

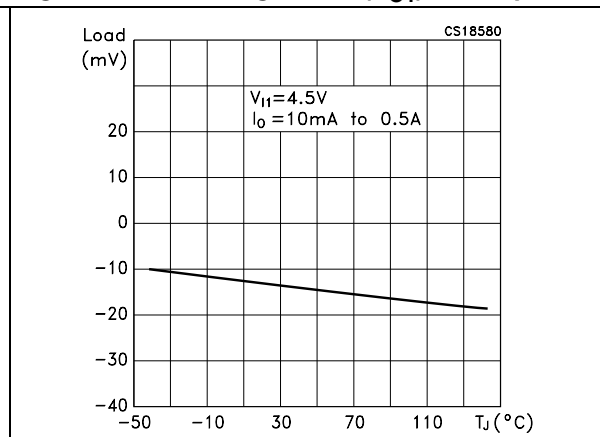




Figure 10. Line regulation ( $V_{O2}$ ) vs temperature

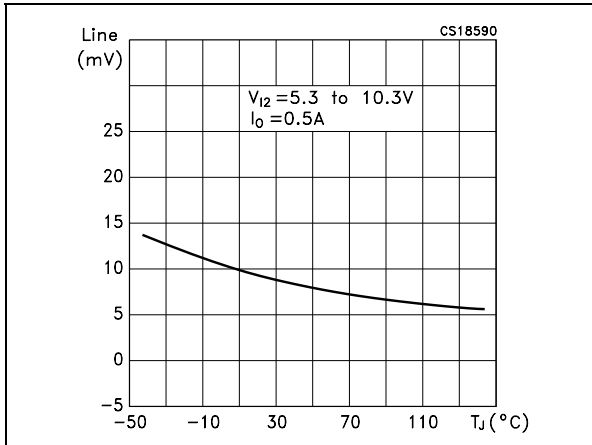


Figure 11. Load regulation ( $V_{O2}$ ) vs temperature

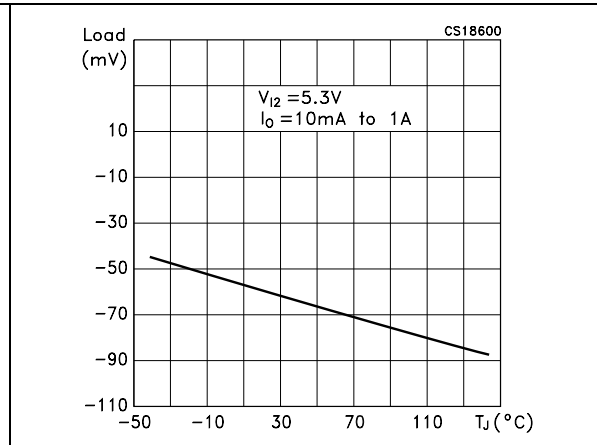


Figure 12. Short circuit current ( $V_{O1}$ ) vs drop voltage

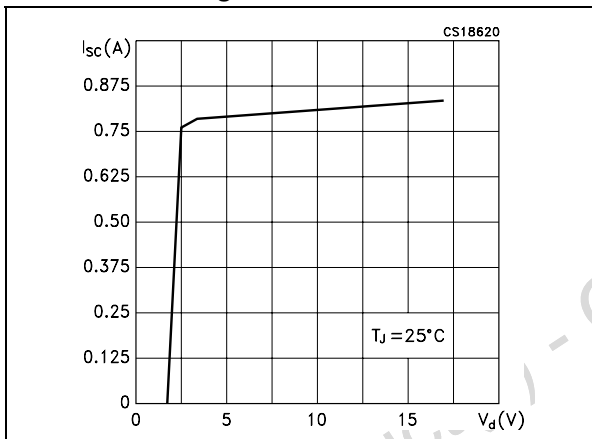


Figure 13. Short circuit current ( $V_{O2}$ ) vs drop voltage

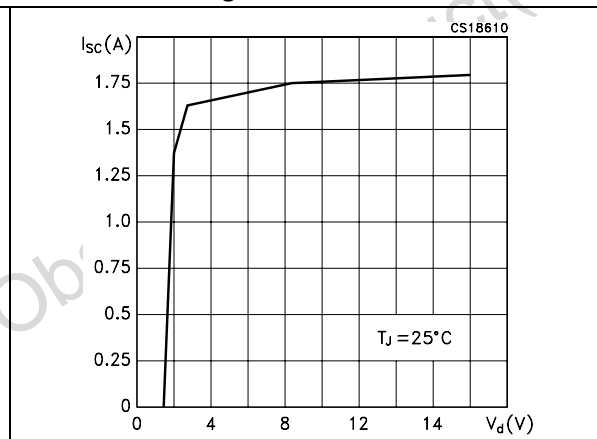


Figure 14. Inhibit voltage vs temperature

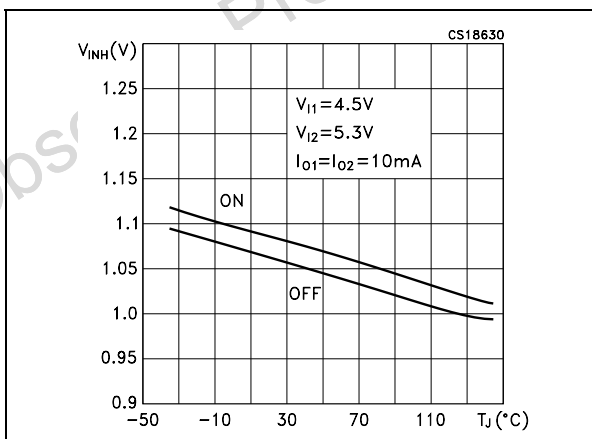


Figure 15. One channel inhibit current vs temperature

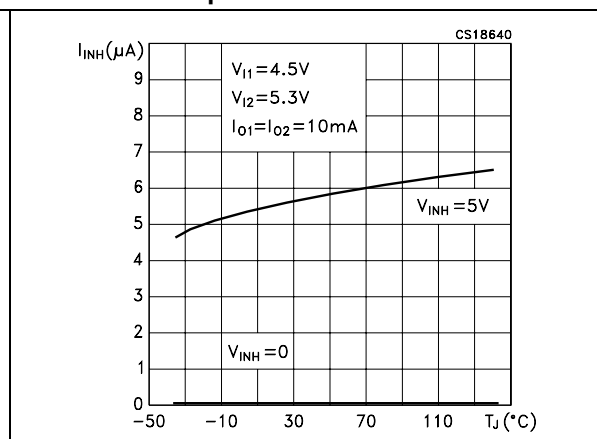


Figure 16. Supply voltage rejection vs ( $V_{O1}$ ) temperature

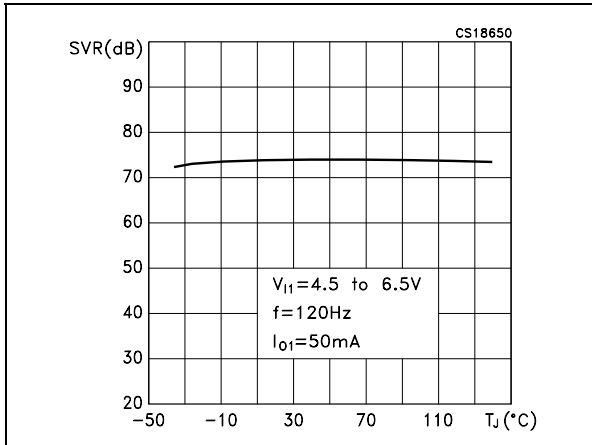


Figure 17. Supply voltage rejection vs ( $V_{O2}$ ) temperature

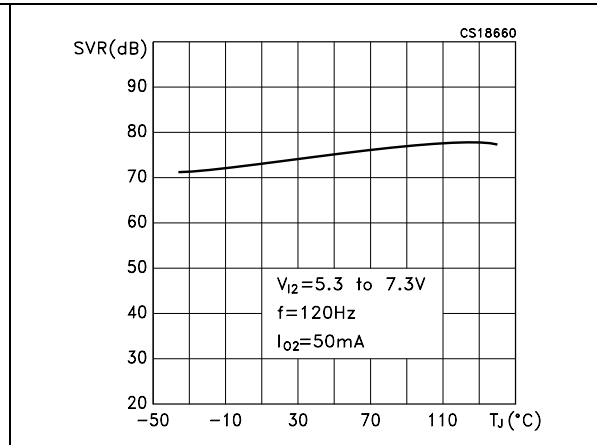


Figure 18. Supply voltage rejection ( $V_{O1}$ ) vs frequency

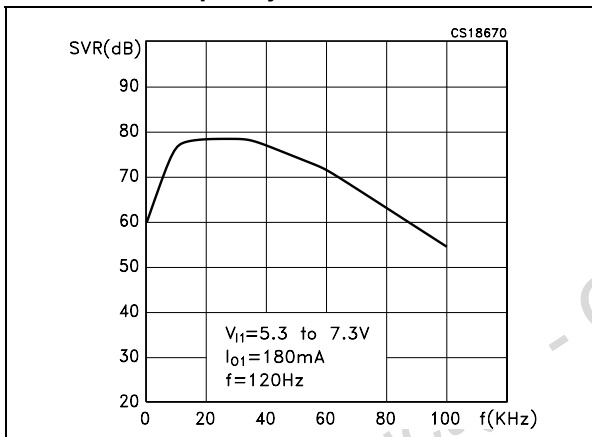


Figure 19. Supply voltage rejection ( $V_{O2}$ ) vs frequency

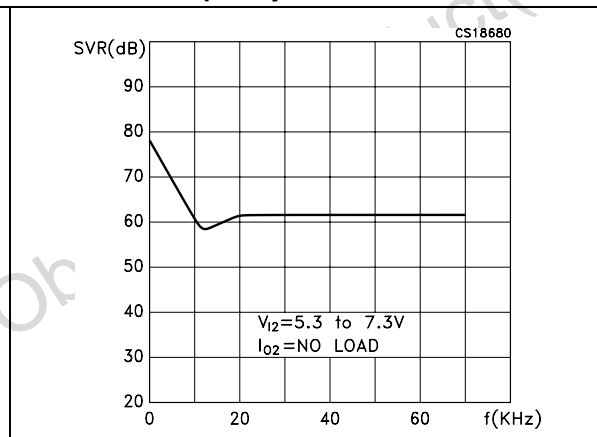


Figure 20. Maximum total quiescent current vs temperature

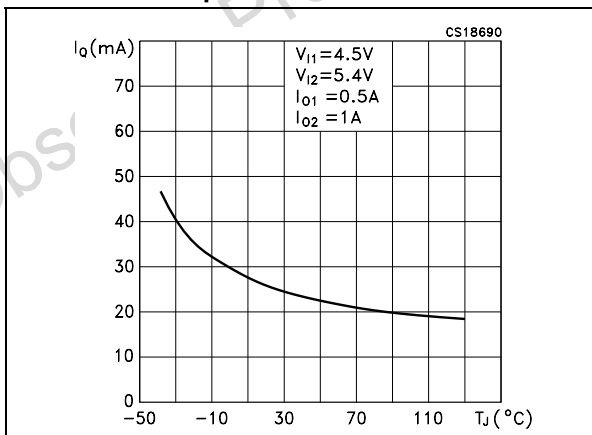


Figure 21. Total supply current vs temperature

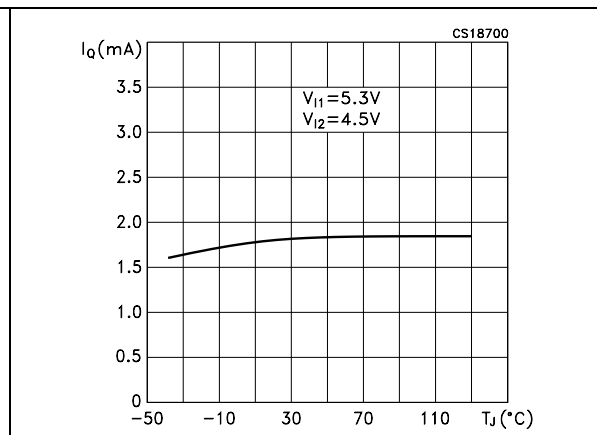


Figure 22. Quiescent current ( $V_{O1}$ ) vs output current

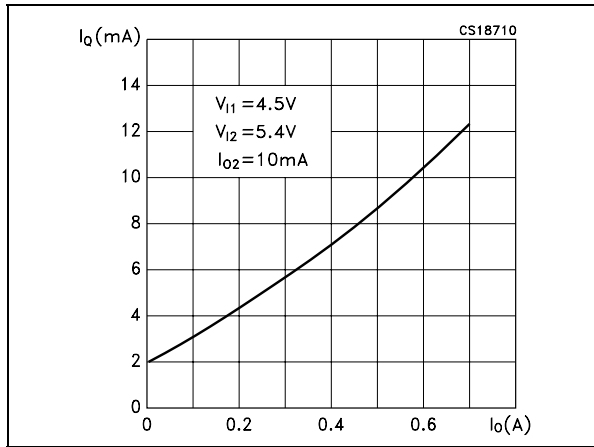


Figure 23. Quiescent current ( $V_{O2}$ ) vs output current

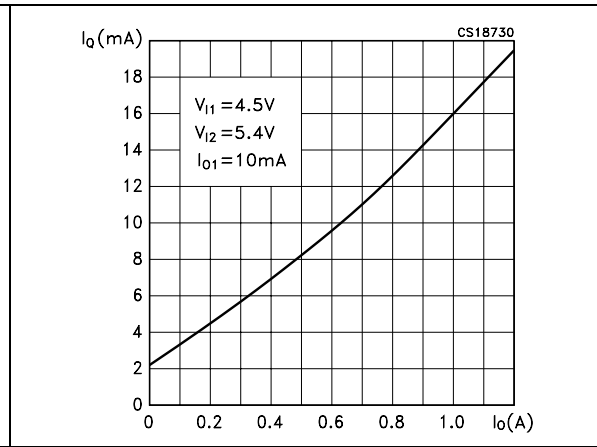


Figure 24. Thermal protection vs  $V_{O1}$

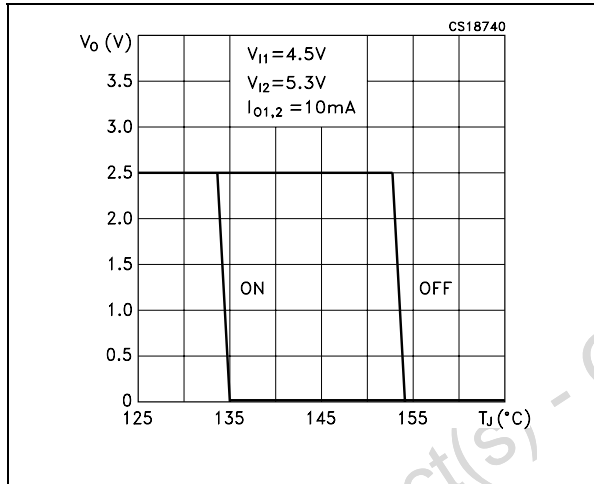


Figure 25. Load transient

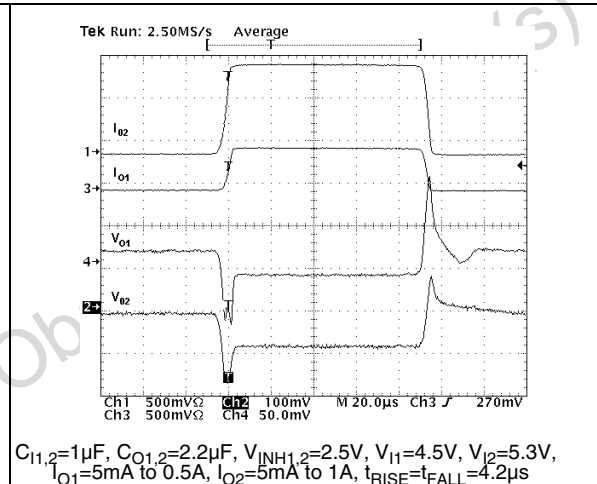


Figure 26. Line transient  $V_{O1,2}$

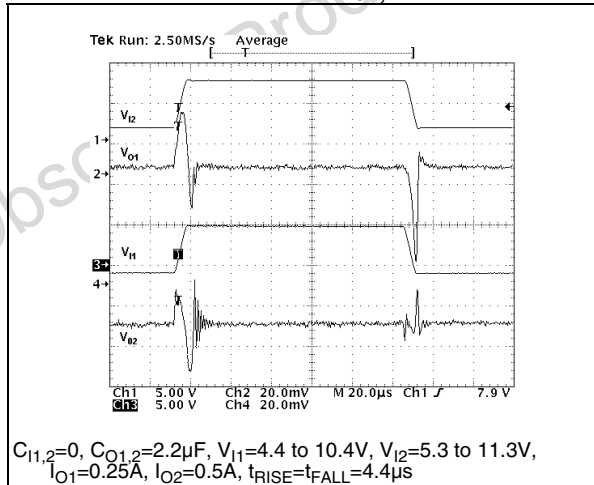
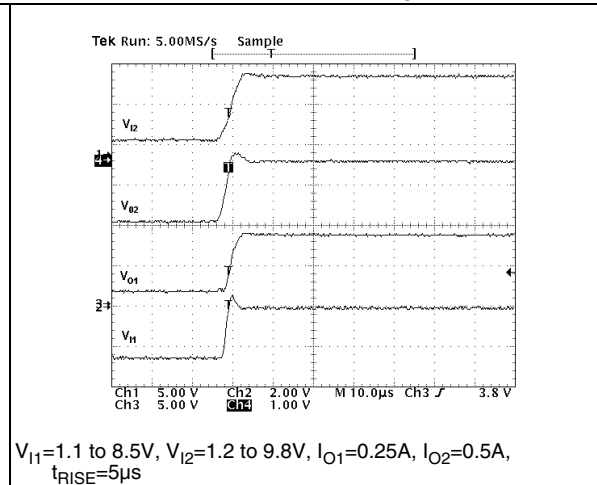


Figure 27. Start up transient  $V_{O1}$



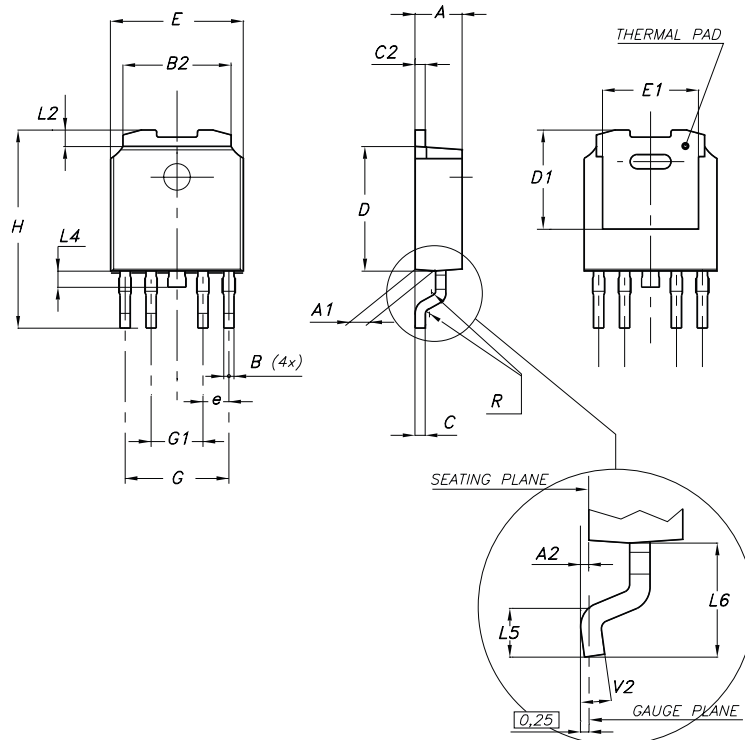
## 7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

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## PPAK mechanical data

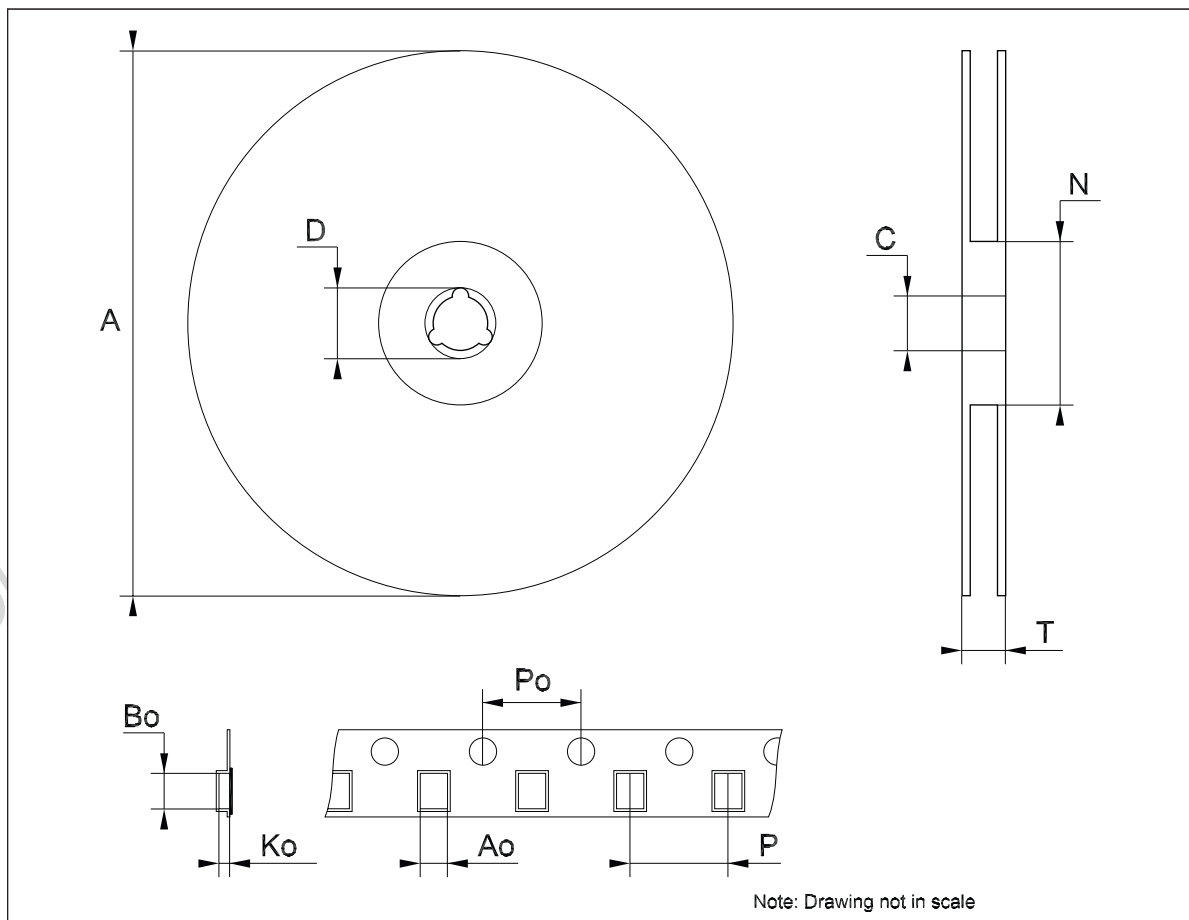
Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.4		0.6	0.015		0.023
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.201	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		1.27			0.050	
G	4.9		5.25	0.193		0.206
G1	2.38		2.7	0.093		0.106
H	9.35		10.1	0.368		0.397
L2		0.8	1		0.031	0.039
L4	0.6		1	0.023		0.039
L5	1			0.039		
L6		2.8			0.110	



0078180-E

**Tape & reel DPAK-PPAK mechanical data**

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.80	6.90	7.00	0.268	0.272	0.276
Bo	10.40	10.50	10.60	0.409	0.413	0.417
Ko	2.55	2.65	2.75	0.100	0.104	0.105
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	7.9	8.0	8.1	0.311	0.315	0.319



## 8 Revision history

Table 6. Document revision history

Date	Revision	Changes
03-Aug-2004	2	Modified: tables 1, 3, 5 and figures 3, 6, 10, 11, 14, 17, 22, 23.
15-Apr-2008	3	Modified: <a href="#">Table 1 on page 1</a> .

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