

5-V Low Drop Fixed Voltage Regulator

TLE 4275

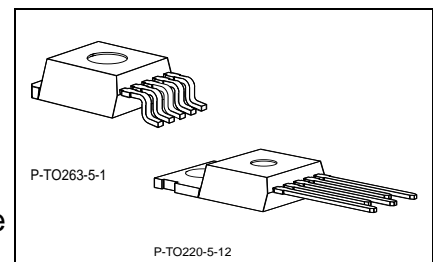
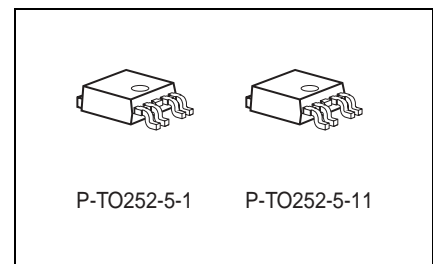
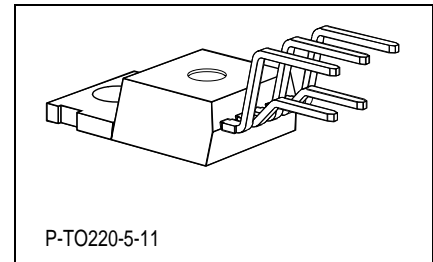
Features

- Output voltage $5\text{ V} \pm 2\%$
- Very low current consumption
- Power-on and undervoltage reset
- Reset low down to $V_Q = 1\text{ V}$
- Very low-drop voltage
- Short-circuit-proof
- Reverse polarity proof
- Suitable for use in automotive electronics
- ESD protection $> 4\text{ kV}$

Functional Description

The TLE 4275 is a monolithic integrated low-drop voltage regulator in a 5-pin TO-package. An input voltage up to 45 V is regulated to $V_{Q,nom} = 5.0\text{ V}$ or 3.3V. The IC is able to drive loads up to 450 mA and is short-circuit proof. At overtemperature the TLE 4275 is turned off by the incorporated temperature protection. A reset signal is generated for an output voltage $V_{Q,rt}$ of typ. 4.65 V. The delay time can be programmed by the external delay capacitor.

*The market versions are PRODUCT PROPOSALS



Type	Ordering Code	Package
TLE 4275	Q67000-A9342	P-TO220-5-11
TLE 4275 D	Q67006-A9354	P-TO252-5-1, P-TO252-5-11
TLE 4275 G	Q67006-A9343	P-TO263-5-1
TLE 4275 S	Q67000-A9442	P-TO220-5-12
TLE 4275 DV33*	on request	P-TO252-5-1, P-TO252-5-11
TLE 4275 GV33*	on request	P-TO263-5-1

Dimensioning Information on External Components

The input capacitor C_1 is necessary for compensation of line influences. Using a resistor of approx. 1Ω in series with C_1 , the oscillating of input inductivity and input capacitance can be damped. The output capacitor C_Q is necessary for the stability of the regulation circuit. Stability is guaranteed at values $C_Q \geq 22 \mu\text{F}$ and an ESR of $\leq 5 \Omega$ within the operating temperature range.

Circuit Description

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The IC also incorporates a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

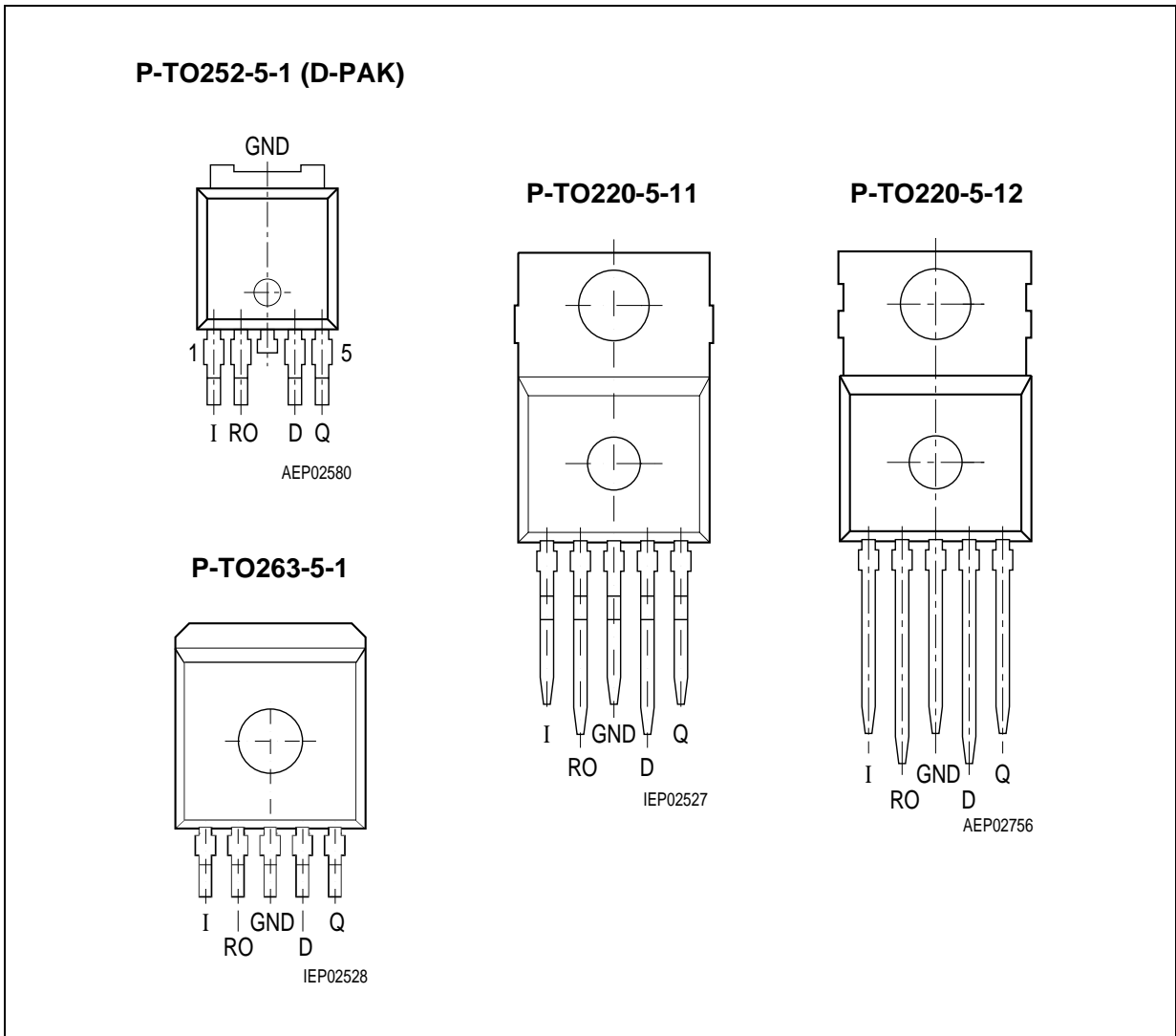


Figure 1 Pin Configuration (top view)

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Function
1	I	Input ; block to ground directly at the IC by a ceramic capacitor.
2	RO	Reset Output ; open collector output
3	GND	Ground ; Pin 3 internally connected to heatsink
4	D	Reset Delay ; connect capacitor to GND for setting delay time
5	Q	Output ; block to ground with a $\geq 22 \mu\text{F}$ capacitor, ESR $< 5 \Omega$ at 10 kHz.

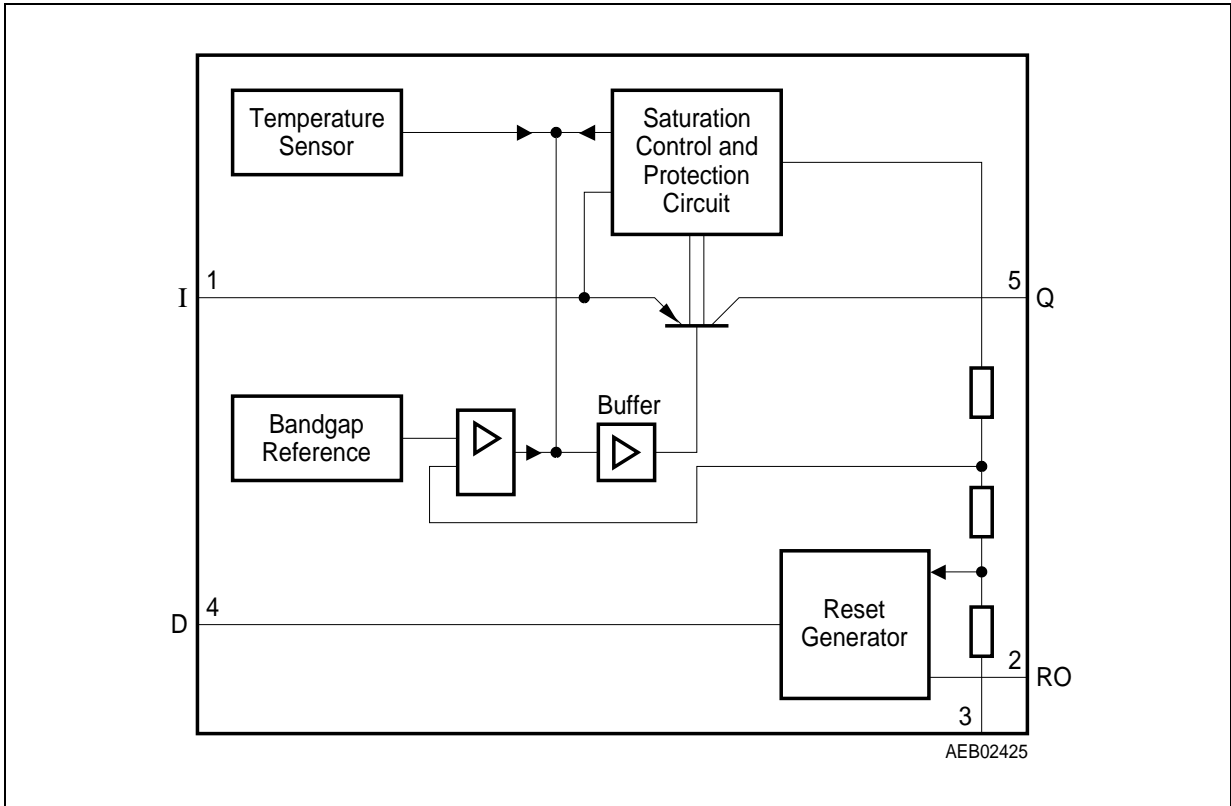


Figure 2 Block Diagram

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Input					
Voltage	V_I	-42	45	V	–
Current	I_I	–	–	–	Internally limited
Output					
Voltage	V_Q	-1.0	16	V	–
Current	I_Q	–	–	–	Internally limited
Reset Output					
Voltage	V_{RO}	-0.3	25	V	–
Current	I_{RO}	– 5	5	mA	–
Reset Delay					
Voltage	V_D	-0.3	7	V	–
Current	I_D	-2	2	mA	–
Temperature					
Junction temperature	T_j	-40	150	°C	–
Storage temperature	T_{stg}	-50	150	°C	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input voltage	V_I	5.5	42	V	5V Version
Input voltage	V_I	4.4	42	V	3.3V Version
Junction temperature	T_j	-40	150	°C	–
Thermal Resistance					
Junction case	R_{thjc}	–	4	K/W	–
Junction ambient	R_{thj-a}	–	53	K/W	TO263 ¹⁾
Junction ambient	R_{thj-a}	–	78	K/W	TO252 ¹⁾
Junction ambient	R_{thj-a}	–	65	K/W	TO220

1) Worst case, regarding peak temperature; zero airflow; mounted on a PCB FR4, $80 \times 80 \times 1.5 \text{ mm}^3$, heat sink area 300 mm^2

Table 4 Characteristics
 $V_I = 13.5 \text{ V}; -40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		Min.	Typ.	Max.		
Output						
Output voltage	V_Q	4.9	5.0	5.1	V	5V Version $5 \text{ mA} < I_Q < 400 \text{ mA}$ $6 \text{ V} < V_I < 28 \text{ V}$
Output voltage	V_Q	4.9	5.0	5.1	V	5V Version $5 \text{ mA} < I_Q < 200 \text{ mA}$ $6 \text{ V} < V_I < 40 \text{ V}$
Output voltage	V_Q	3.23	3.3	3.37	V	3.3V Version $5 \text{ mA} < I_Q < 400 \text{ mA}$ $4.4\text{V} < V_I < 28 \text{ V}$
Output voltage	V_Q	3.23	3.3	3.37	V	3.3V Version $5 \text{ mA} < I_Q < 200 \text{ mA}$ $4.4\text{V} < V_I < 40 \text{ V}$
Output current limitation ¹⁾	I_Q	450	700	–	mA	–
Current consumption; $I_q = I_I - I_Q$	I_q	–	150	200	μA	$I_Q = 1 \text{ mA};$ $T_j = 25 \text{ }^\circ\text{C}$
Current consumption; $I_q = I_I - I_Q$	I_q	–	150	220	μA	$I_Q = 1 \text{ mA};$ $T_j \leq 85 \text{ }^\circ\text{C}$
Current consumption; $I_q = I_I - I_Q$	I_q	–	5	10	mA	$I_Q = 250 \text{ mA}$
Current consumption; $I_q = I_I - I_Q$	I_q	–	12	22	mA	$I_Q = 400 \text{ mA}$
Drop voltage ¹⁾	V_{dr}	–	250	500	mV	$I_Q = 300 \text{ mA};$ $V_{dr} = V_I - V_Q$
Load regulation	ΔV_Q	–	15	30	mV	$I_Q = 5 \text{ mA to } 400 \text{ mA}$
Line regulation	ΔV_Q	-15	5	15	mV	$\Delta V_I = 8 \text{ V to } 32 \text{ V}$ $I_Q = 5 \text{ mA}$
Power supply ripple rejection	$PSRR$	–	60	–	dB	$f_r = 100 \text{ Hz};$ $V_r = 0.5 \text{ Vpp}$

Table 4 Characteristics (cont'd)
 $V_I = 13.5 \text{ V}; -40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		Min.	Typ.	Max.		
Temperature output voltage drift	dV_Q/dT	–	0.5	–	mV/K	–

Reset Timing D and Output RO

Reset switching threshold	$V_{Q,rt}$	4.5	4.65	4.8	V	5V Version
Reset switching threshold	$V_{Q,rt}$	3.0	3.1	3.2	V	3.3V Version
Reset output low voltage	V_{ROL}	–	0.2	0.4	V	$R_{ext} \geq 5 \text{ k}\Omega;$ $V_Q > 1 \text{ V}$
Reset output leakage current	I_{ROH}	–	0	10	μA	$V_{ROH} = 5 \text{ V}$
Reset charging current	$I_{D,c}$	3.0	5.5	9.0	μA	$V_D = 1 \text{ V}, 5\text{V Version}$
Upper timing threshold	V_{DU}	1.5	1.8	2.2	V	5V Version
Reset charging current	$I_{D,c}$	3.0	7.0	11	μA	$V_D = 1 \text{ V}, 3.3\text{V Ver.}$
Upper timing threshold	V_{DU}	0.7	1.1	1.6	V	3.3V Version
Lower timing threshold	V_{DRL}	0.2	0.4	0.7	V	–
Reset delay time	t_{rd}	10	16	22	ms	$C_D = 47 \text{ nF}$
Reset reaction time	t_{rr}	–	0.5	2	μs	$C_D = 47 \text{ nF}$

 1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at $V_I = 13.5 \text{ V}$.

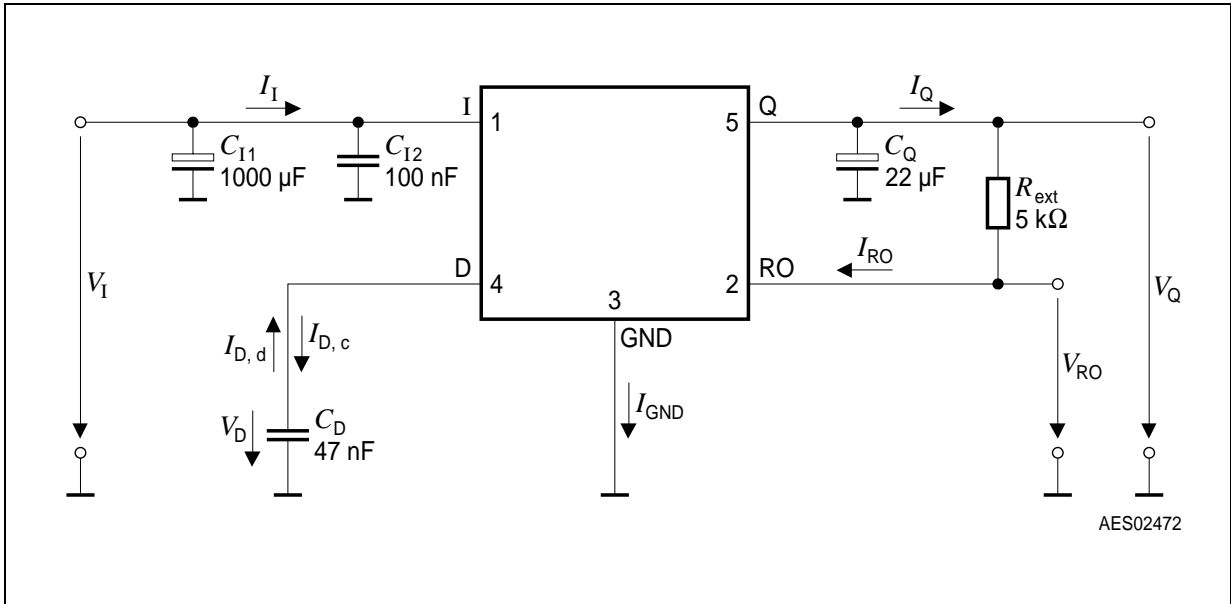


Figure 3 Test Circuit

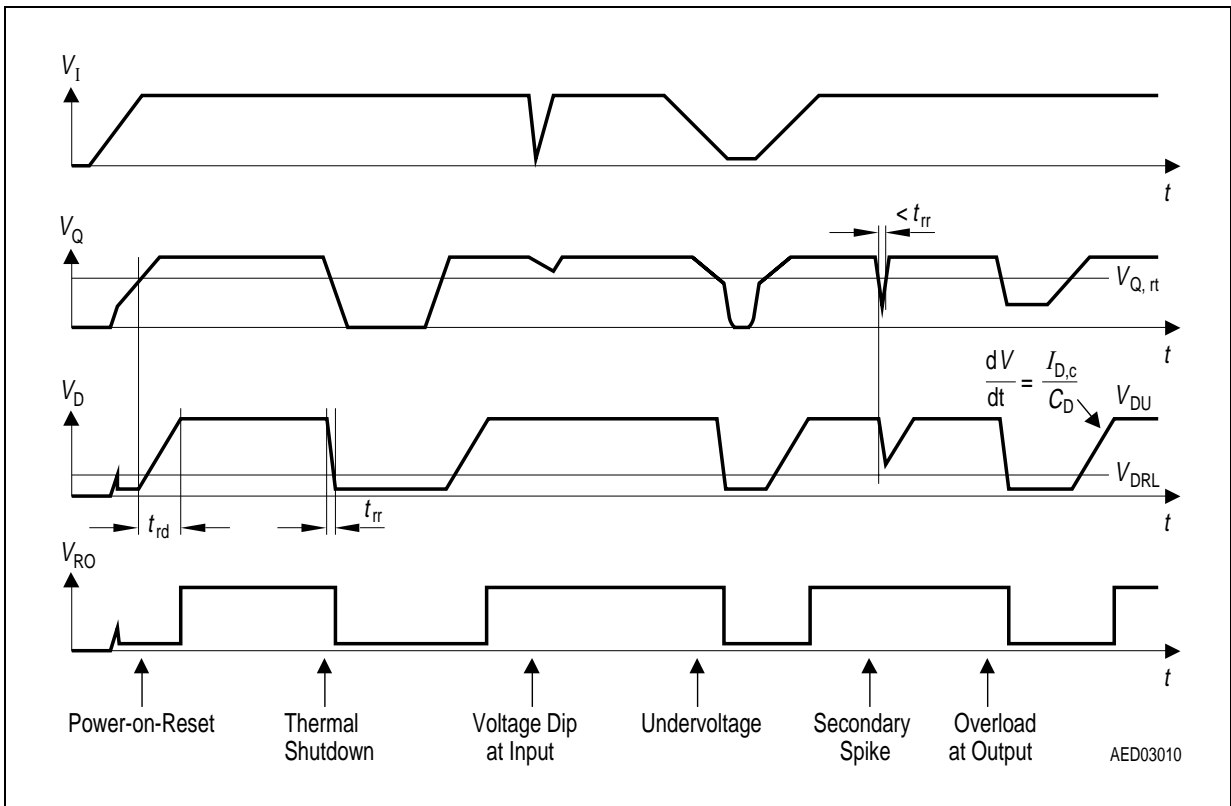
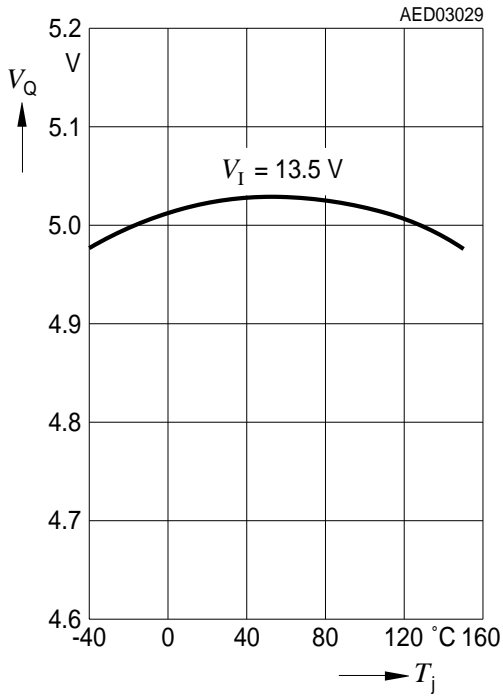
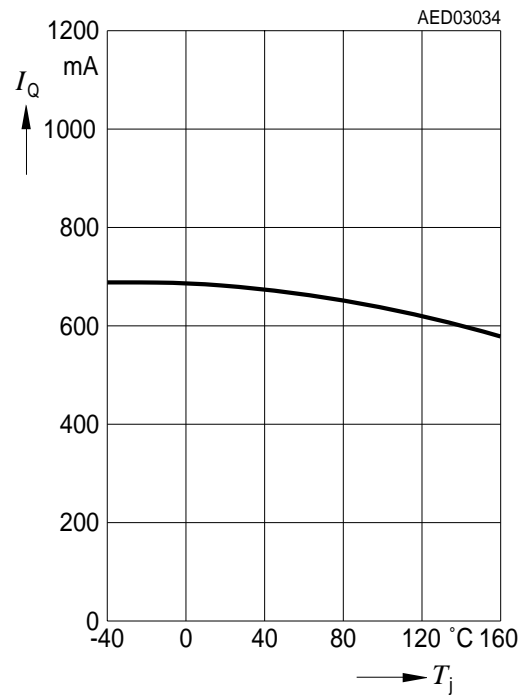


Figure 4 Reset Timing

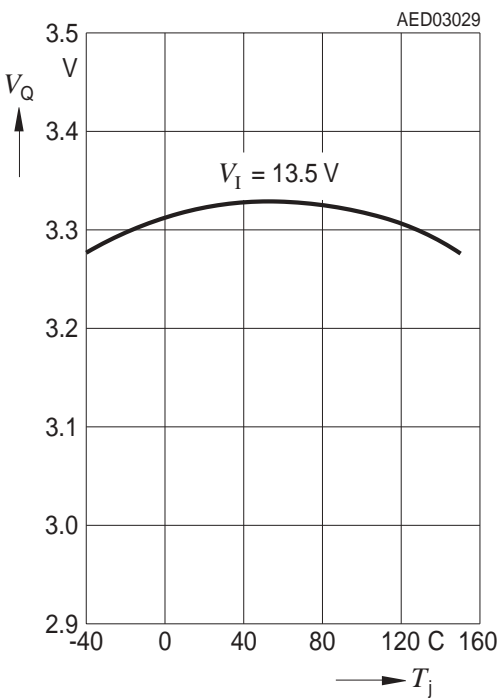
Output Voltage V_Q versus Temperature T_j



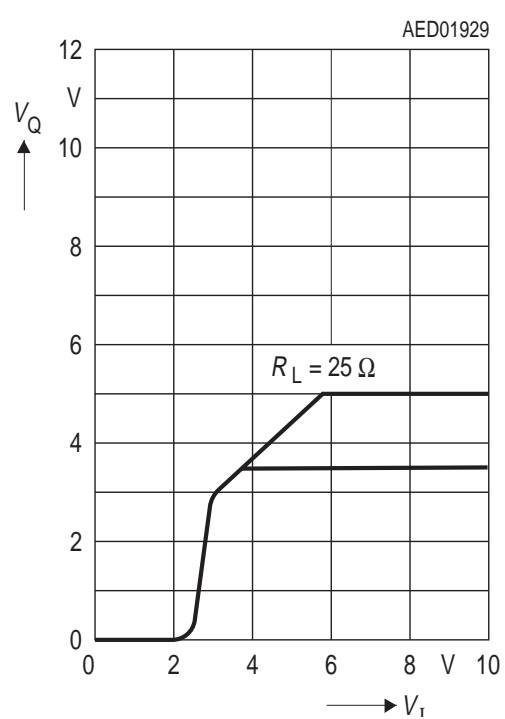
Output Current I_Q versus Temperature T_j



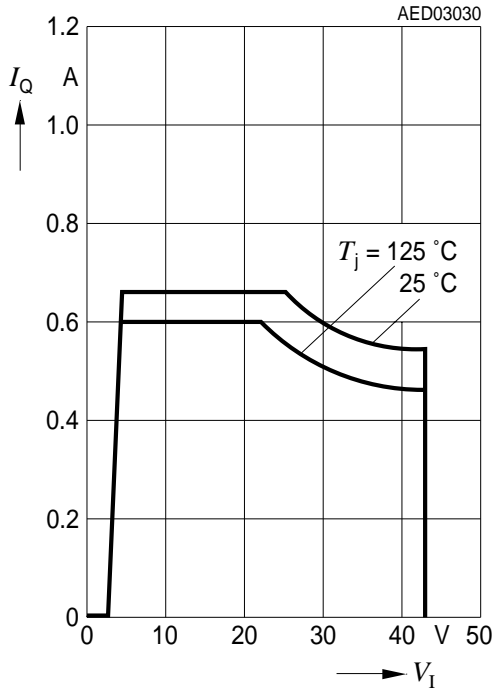
Output Voltage V_Q versus Temperature T_j



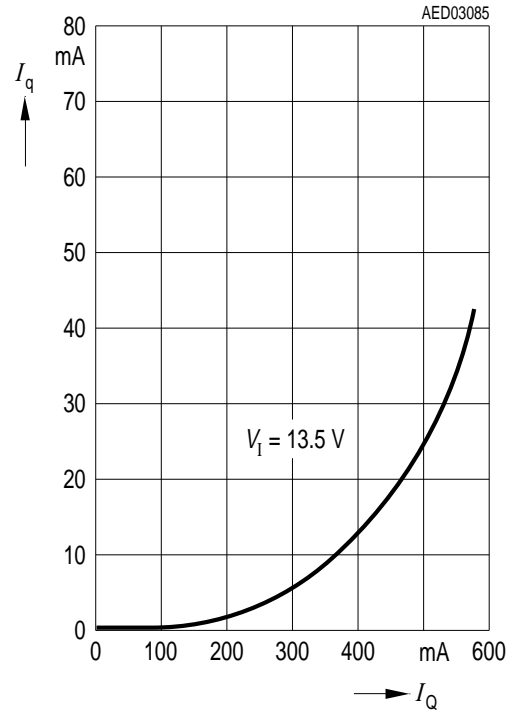
Output Voltage V_Q versus Input Voltage V_I



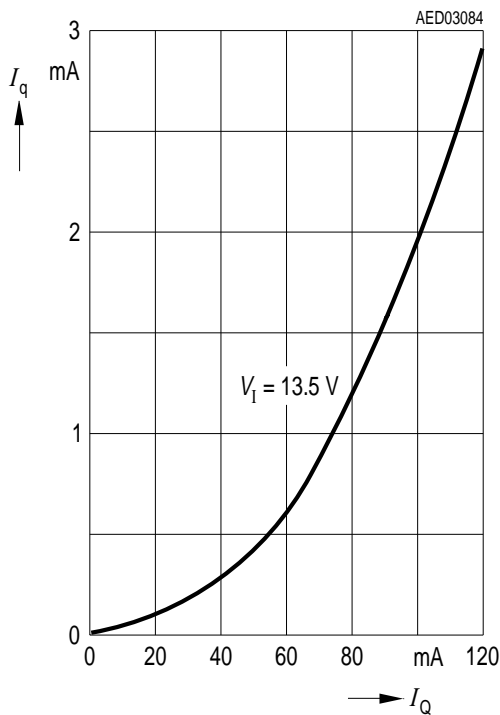
Output Current I_Q versus Input Voltage V_I



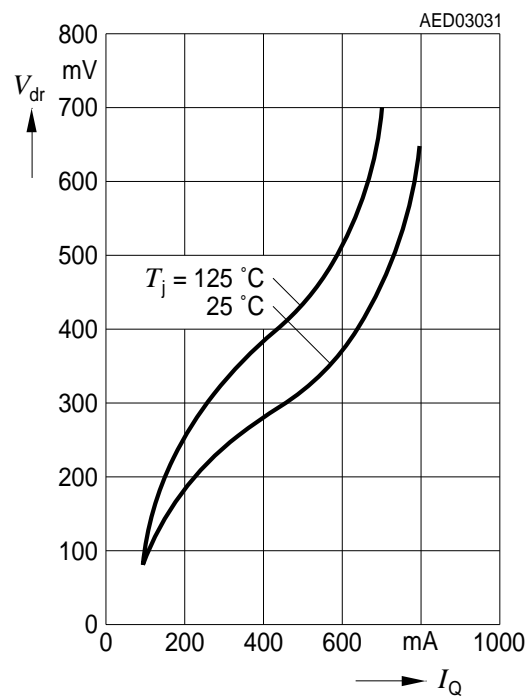
Current Consumption I_q versus Output Current I_Q



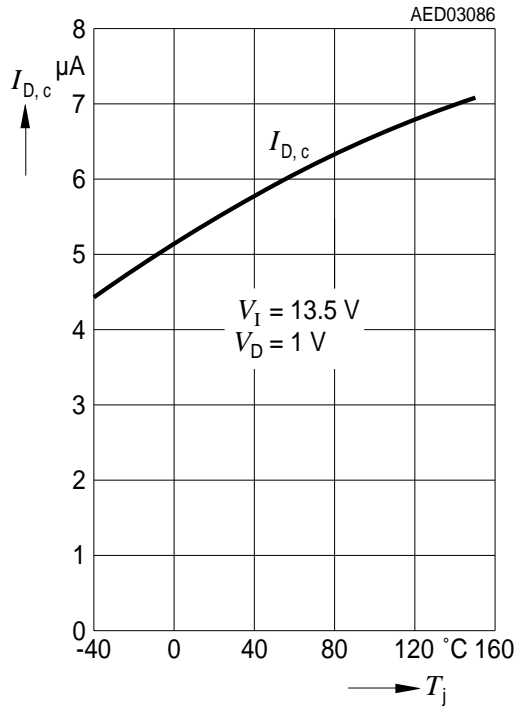
Current Consumption I_q versus Output Current I_Q



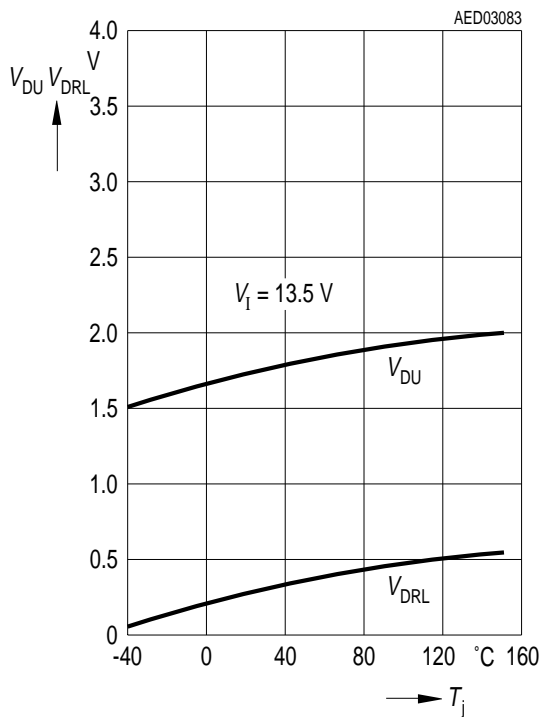
Drop Voltage V_{dr} versus Output Current I_Q



**Charge Current $I_{D,c}$
versus Temperature T_j**



**Delay Switching Threshold V_{DU} , V_{DRL}
versus Temperature T_j**



Package Outlines

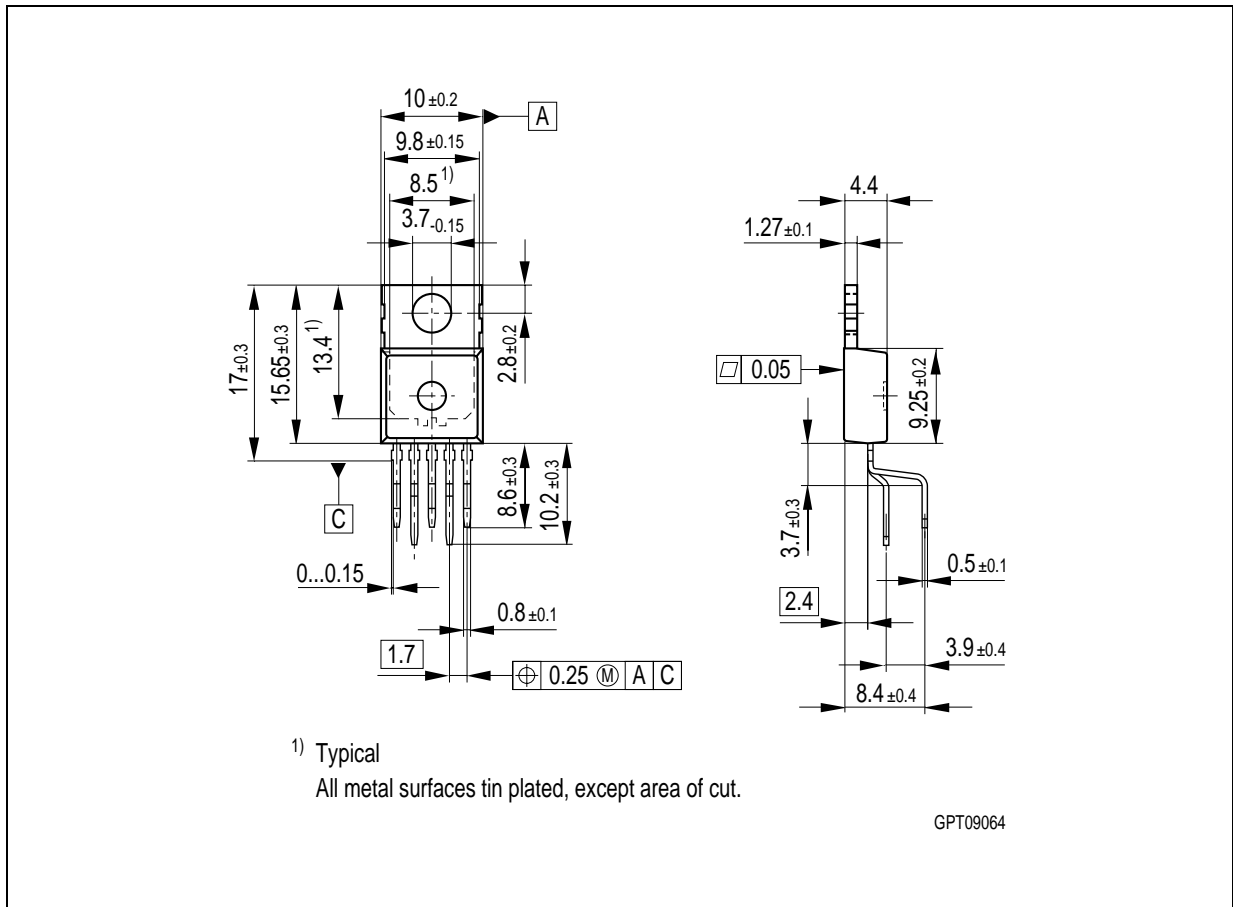


Figure 5 P-TO220-5-11 (Plastic Transistor Single Outline)

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SMD = Surface Mounted Device

Dimensions in mm

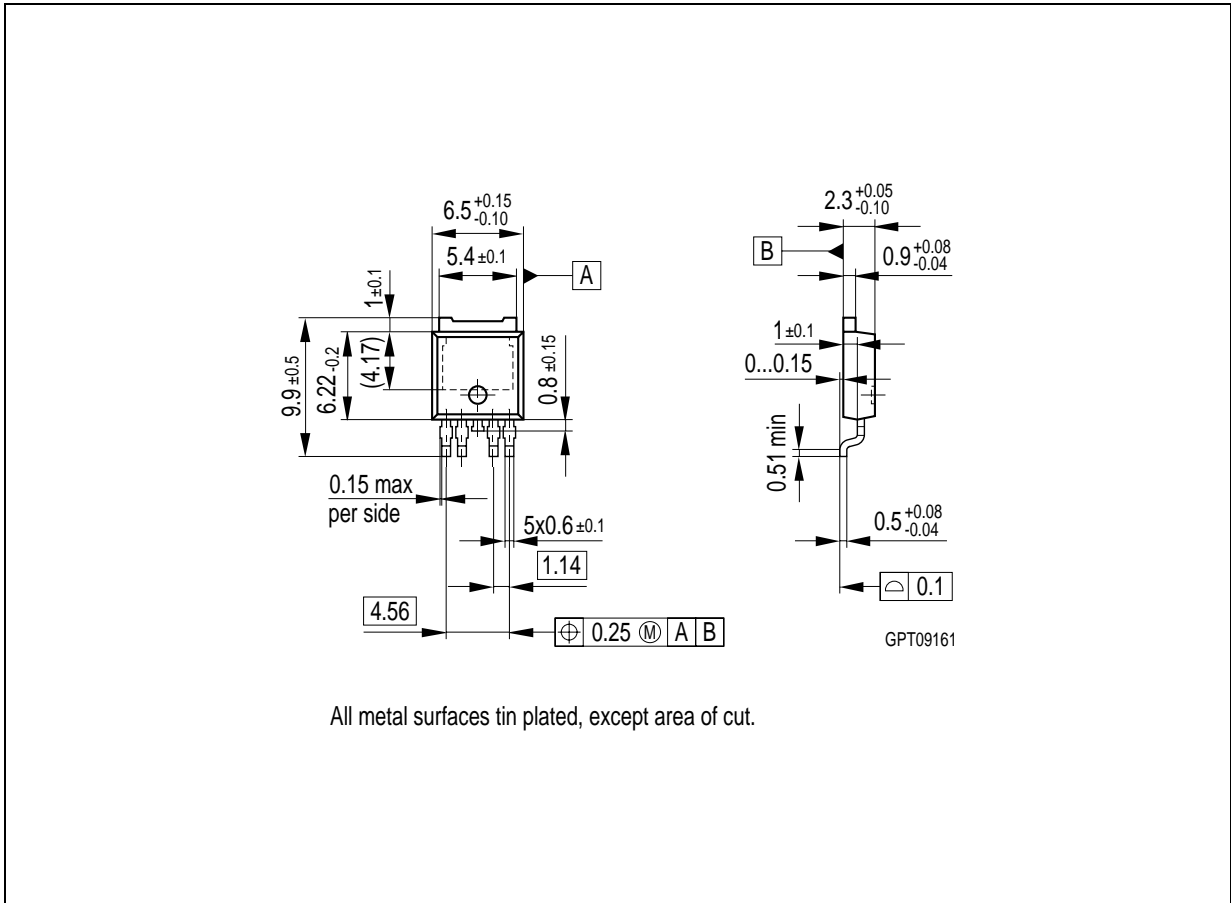


Figure 6 P-TO252-5-1 (Plastic Transistor Single Outline)

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SMD = Surface Mounted Device

Dimensions in mm

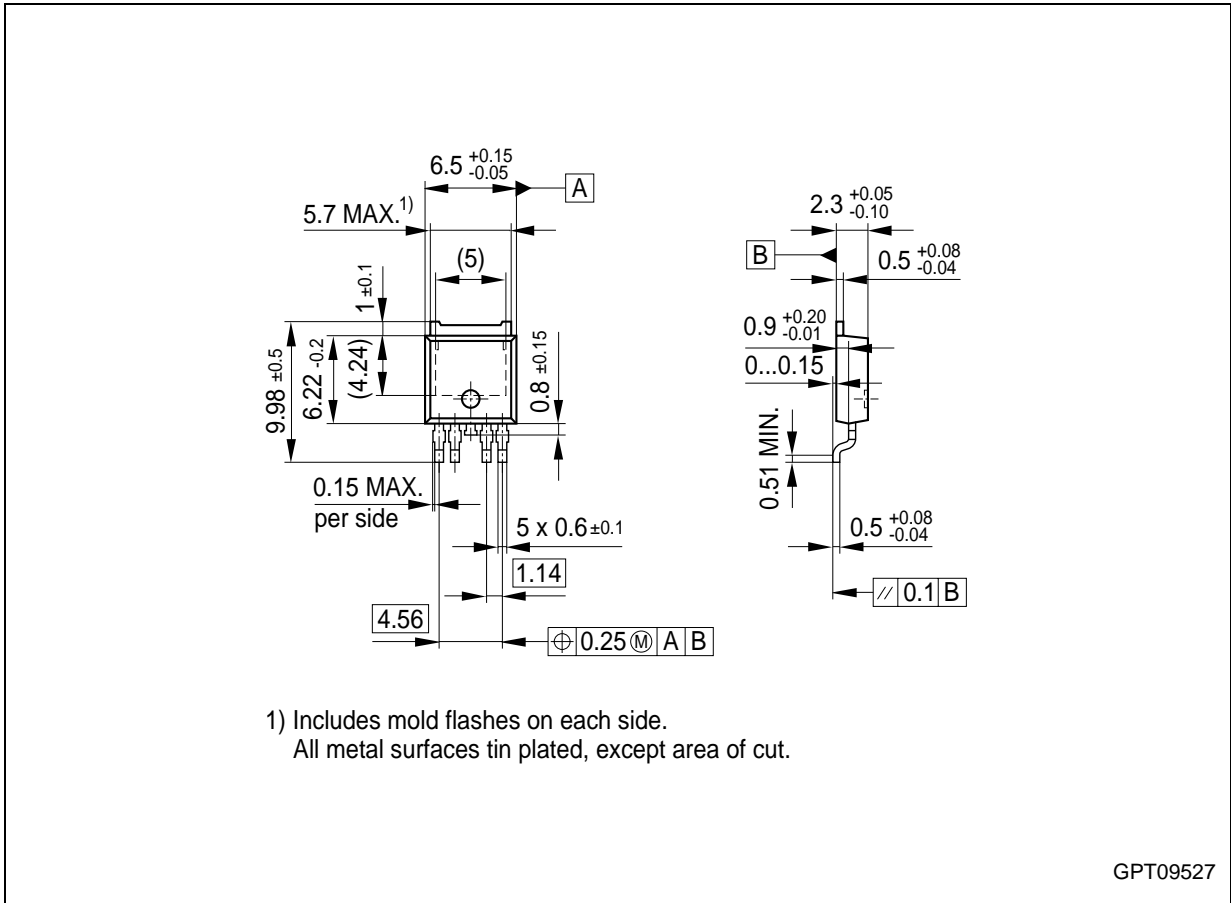


Figure 7 P-TO252-5-11 (Plastic Transistor Single Outline)

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SMD = Surface Mounted Device

Dimensions in mm

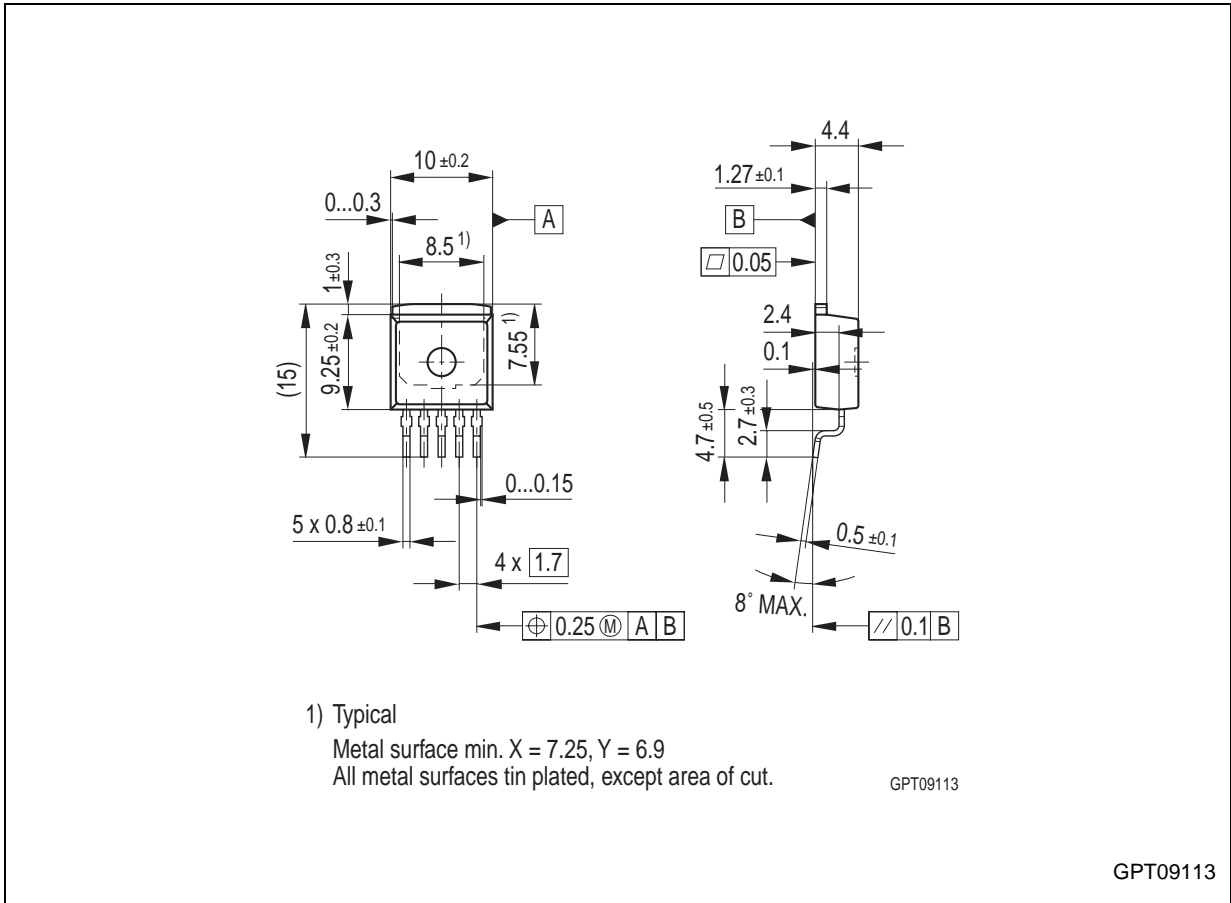


Figure 8 P-TO263-5-1 (Plastic Transistor Single Outline)

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SMD = Surface Mounted Device

Dimensions in mm

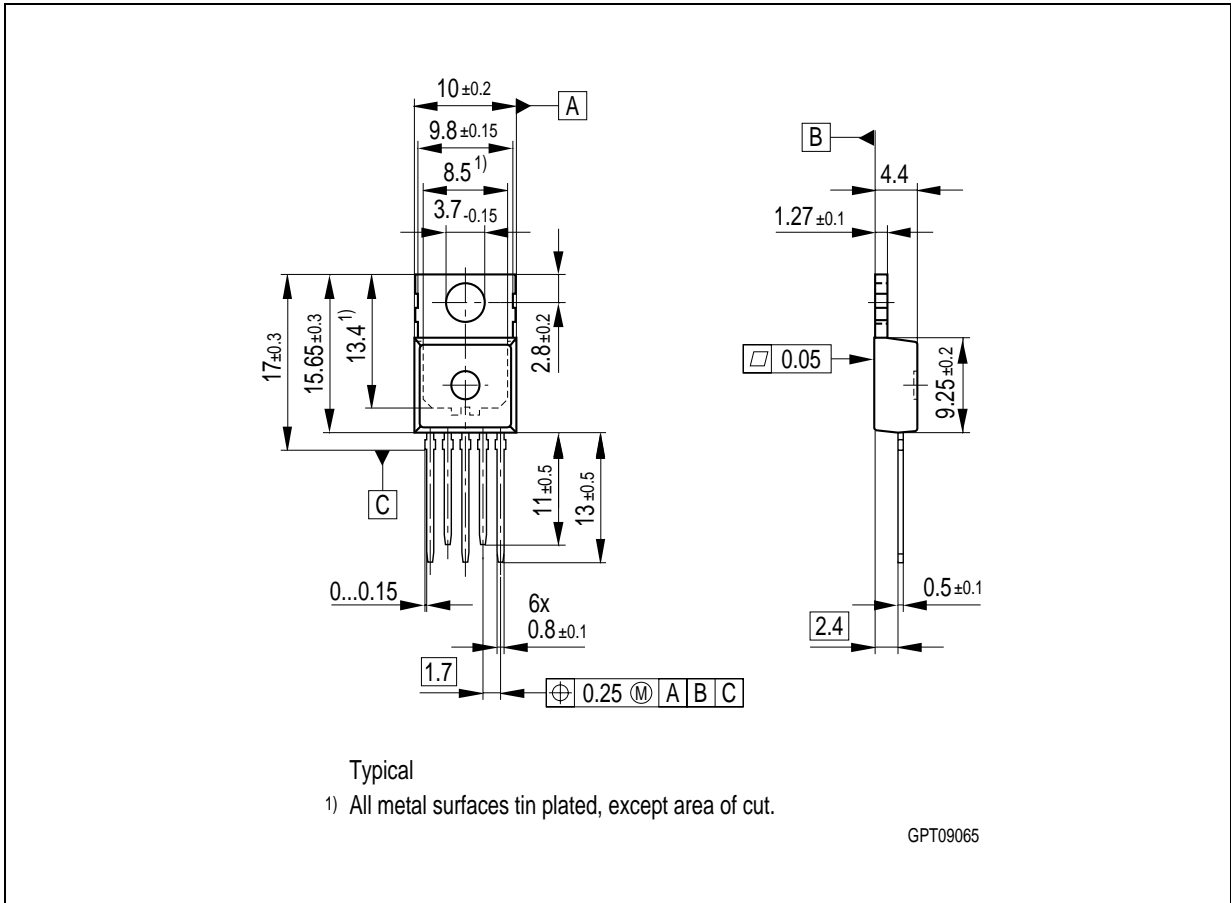


Figure 9 P-TO220-5-12 (Plastic Transistor Single Outline)

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SMD = Surface Mounted Device

Dimensions in mm

Remarks

Edition 2005-08-09

**Published by Infineon Technologies AG,
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