

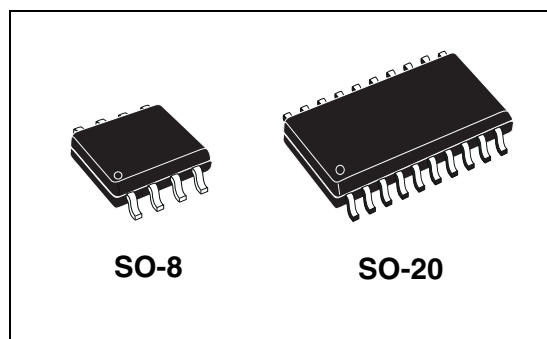
## Low drop voltage regulator

### Features

Max DC supply voltage	$V_S$	40V
Max output voltage tolerance	$\Delta V_O$	+/-2%
Max dropout voltage	$V_{dp}$	500 mV
Output current	$I_O$	200 mA
Quiescent current	$I_{qn}$	75 $\mu A^{(1)}$

1. Typical value with watchdog disabled.

- Operating DC supply voltage range 5.6V to 31V
- Reset circuit sensing the output voltage down to 1V
- Programmable reset pulse delay with external capacitor
- Watchdog
- Programmable watchdog timer with external capacitor
- Enable input for enabling/disabling the watchdog functionality
- Thermal shutdown and short circuit protection
- Wide temperature range ( $T_j = -40^\circ C$  to  $150^\circ C$ )



### Description

The L4988 is a monolithic integrated 5V voltage regulator with a low drop voltage at currents up to 200mA. The output voltage regulating element consists in a p-channel MOS and the regulation is performed regardless of input voltage transients up to 40V. The high precision of the output voltage is obtained with a pre-trimmed reference voltage. The L4988 is protected against short circuit and an over-temperature protection switches off the device in case of extremely high power dissipation. The L4988 is active when the Enable is high. State of the art features like reset and watchdog make this device particularly suitable to supply microprocessor systems in automotive applications.

**Table 1. Device summary**

Package	Order codes	
	Tube	Tape & reel
SO8	L4988D	L4988DTR
SO20 (16+2+2)	L4988MD	L4988MDTR

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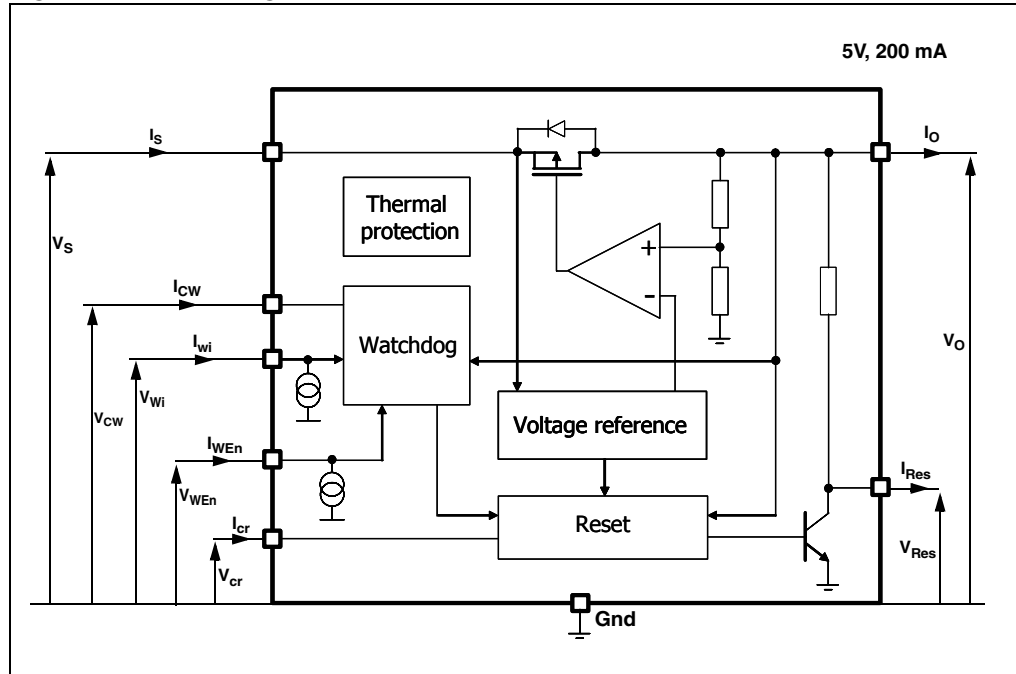
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# 1 Block diagram and pin configuration

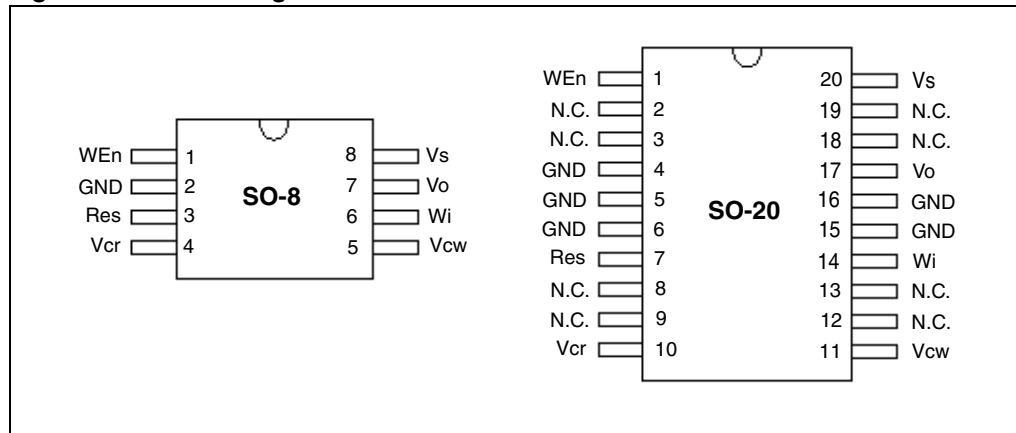
Figure 1. Block diagram



**Table 2. Pins description**

Pin name	SO8(D)	S020(MD)	Function
WEn	1	1	Watchdog Enable input If high watchdog functionality is active
Gnd	2	4	Ground reference
Gnd		5, 6, 15, 16	Ground. Connected these pins to a heat spreader ground
Res	3	7	Reset output. It is pulled down when output voltage goes below Vo_th or frequency at Wi is too low.
Vcr	4	10	Reset timing adjust. A capacitor between Vcr pin and gnd, sets the reset delay time (trd)
Vcw	5	11	Watchdog timer adjust A capacitor between Vcw pin and gnd, sets the time response of the watchdog monitor.
Wi	6	14	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated.
Vo	7	17	Voltage regulator output Block to ground with a capacitor >100nF (needed for regulator stability)
Vs	8	20	Supply voltage Block to ground directly at IC pin with a capacitor
N.C.		2, 3, 8, 9, 12, 13, 18, 19	Not connected

**Figure 2. Pins configuration**



## 2 Electrical specifications

### 2.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{VSDC}$	DC supply voltage	-0.3 to 40	V
$I_{VSDC}$	Input current	Internally limited	
$V_{VO}$	DC output voltage	-0.3 to 6	V
$I_{VO}$	DC output current	Internally limited	
$V_{Wi}$	Watchdog input voltage	-0.3 to $V_{VO} + 0.3$	V
$V_{od}$	Open Drain output voltage	-0.3 to $V_{VO} + 0.3$	V
$I_{od}$	Open Drain output current	Internally limited	
$V_{cr}$	Reset delay voltage	-0.3 to $V_{VO} + 0.3$	V
$V_{cw}$	Watchdog delay voltage	-0.3 to $V_{VO} + 0.3$	V
$V_{WEn}$	Watchdog Enable input voltage	-0.3 to $V_{VO} + 0.3$	V
$T_j$	Junction temperature	-40 to 150	°C
$V_{ESD}$	ESD voltage level (HBM-MIL STD 883C)	±2	kV
$V_{ESD}$	ESD voltage level (CDM AEC-Q100-011)	750	V

*Note:* Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

### 2.2 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	S08	S016+2+2	Unit
$R_{th-jamb}$	Thermal resistance junction to ambient	130 <sup>(1)</sup>	51 <sup>(2)</sup>	°C/W

1. With copper area 2 cm<sup>2</sup>; for details see [Figure 29](#).

2. With copper area 6 cm<sup>2</sup>; for details see [Figure 33](#).

## 2.3 Electrical characteristics

$V_s = 5.6V$  to  $31V$ ,  $T_j = -40^\circ C$  to  $+150^\circ C$  unless otherwise specified.

**Table 5. General**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Vo	$V_{o\_ref}$	Output voltage	$V_s = 6$ to $31V$ $I_o = 1$ to $200mA$	4.9	5.0	5.1	V
Vo	$I_{short}$	Short circuit current	$V_s = 13.5V^{(1)}$	200	280	500	mA
Vo	$I_{lim}^{(2)}$	Output current limitation	$V_s = 13.5V^{(1)}$	200	350	600	mA
$V_s, V_o$	$V_{line}$	Line regulation voltage	$V_s = 6$ to $31V$ $I_o = 1$ to $200mA$			25	mV
Vo	$V_{load}$	Load regulation voltage	$I_o = 1$ to $200mA$			25	mV
$V_s, V_o$	$V_{dp}^{(3)}$	Drop voltage	$I_o = 200mA$		270	500	mV
$V_s, V_o$	$V_{dp}^{(3)}$	Drop voltage	$I_o = 150mA$		200	400	mV
$V_s, V_o$	SVR	Ripple rejection	$f_r = 100 Hz^{(4)}$		60		dB
$V_s, V_o$	$I_{qn\_200}$	Quiescent current	$V_s=13.5V$ , $I_o=200mA$ , $WEn = high$		1.9	2.5	mA
$V_s, V_o$	$I_{qn\_50}$	Quiescent current	$V_s=13.5V$ , $I_o= 50mA$ , $WEn = high$		500	700	$\mu A$
$V_s, V_o$	$I_{q\_1\_we}$	Quiescent current	$V_s=13.5V$ , $I_o < 1mA$ , $WEn = high$		93	200	$\mu A$
$V_s, V_o$	$I_{q\_1\_wd}$	Quiescent current	$V_s=13.5V$ , $I_o < 1mA$ , $WEn = low$		75	150	$\mu A$
	$T_w$	Thermal protection temperature		150		190	$^\circ C$
	$T_w\_hy$	Thermal protection temperature hysteresis			10		$^\circ C$

1. See [Figure 3](#).
2. Measured output current when the output voltage has dropped 100mV from its nominal value obtained at  $V_s=13.5V$  and  $I_o= 75mA$ .
3.  $V_s-V_o$  measured when the output voltage has dropped 100mV from its nominal value obtained at  $V_s=13.5V$  and  $I_o= 75mA$ .
4. Guaranteed by design.



Table 6. Reset

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Res	Vres_l	Reset output low voltage	$R_{ext} = 5k\Omega$ to $V_o$ , $V_o > 1V$			0.4	V
Res	I <sub>Res_h</sub>	Reset output high leakage current	$V_{Res} = 5V$			1	$\mu A$
Res	R_p_u	Pull up internal resistance	With respect to $V_o$	12	25	50	$k\Omega$
Res	V <sub>o_th</sub>	$V_o$ out of regulation threshold	$V_s = 6$ to $31V$ , $I_o = 1$ to $200mA$	6%	8%	10%	Below $V_{o\_ref}$
Vcr	Vr <sub>lth</sub>	Reset timing low threshold	$V_s = 13.5V$	10%	13%	16%	$V_{o\_ref}$
Vcr	Vr <sub>hth</sub>	Reset timing high threshold	$V_s = 13.5V$	44%	47%	50%	$V_{o\_ref}$
Vcr	I <sub>cr</sub>	Charge current	$V_s = 13.5V$	8	17.6	30	$\mu A$
Vcr	I <sub>dr</sub>	Discharge current	$V_s = 13.5V$	8	17.6	30	$\mu A$
Res	Trr_2	Reset reaction time <sup>(1)</sup>	$V_o = V_{o\_th} - 100mV$	100	275	1000	$\mu s$
Res	Trd	Reset delay time	$V_s = 13.5V$ , $C_{tr} = 1nF$	65		150	ms

1. When  $V_o$  becomes lower than 4V, the reset reaction time decreases down to 2 $\mu s$  assuring a faster reset condition in this particular case.

Table 7. Watchdog

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Wi	V <sub>ih</sub>	Input high voltage	$V_s = 13.5V$	3.5			V
Wi	V <sub>il</sub>	Input low voltage	$V_s = 13.5V$			1.5	V
Wi	V <sub>ih</sub>	Input hysteresis	$V_s = 13.5V$		500		mV
Wi	I <sub>i</sub>	Pull down current	$V_s = 13.5V$		10	20	$\mu A$
Vcw	V <sub>whth</sub>	High threshold	$V_s = 13.5V$	44%	47%	50%	$V_{o\_ref}$
Vcw	V <sub>wlth</sub>	Low threshold	$V_s = 13.5V$	10%	13%	16%	$V_{o\_ref}$
Vcw	I <sub>cwc</sub>	Charge current	$V_s = 13.5V$ , $V_{cw} = 0.1V$	4	8	14	$\mu A$
Vcw	I <sub>cwd</sub>	Discharge current	$V_s = 13.5V$ , $V_{cw} = 2.5V$	1.0	2.1	4.5	$\mu A$
Vcw	T <sub>wop</sub>	Watchdog period	$V_s = 13.5V$ , $C_{tw} = 47nF$	25	50	90	ms
Res	twol	Watchdog output low time	$V_s = 13.5V$ , $C_{tw} = 47nF$	6	10.5	22	ms

**Table 8. Watchdog Enable**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
WEn	V <sub>En_l</sub>	Enable input low voltage				1	V
WEn	V <sub>En_h</sub>	Enable input high voltage		3			V
WEn	V <sub>En_hy</sub>	Enable input hysteresis		500	800	1100	mV
WEn	I <sub>leak</sub>	Pull down current	WEn = 5V	2	8	20	μA

## 2.4 Electrical characteristics curves

Figure 3. Output voltage vs. Tj

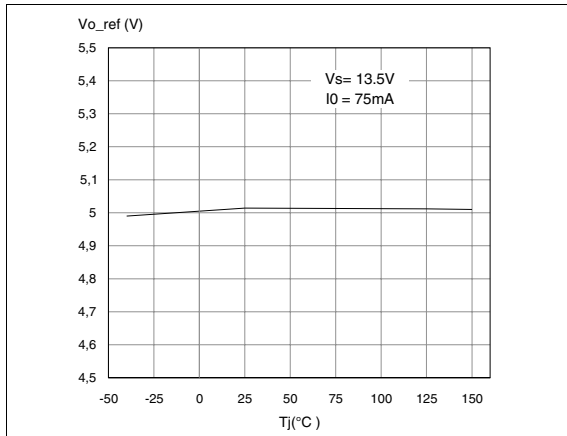


Figure 4. Output voltage vs. Vs

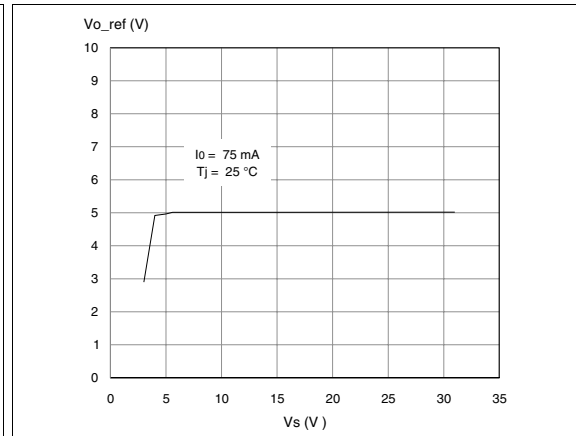


Figure 5. Drop Voltage vs. Output Current

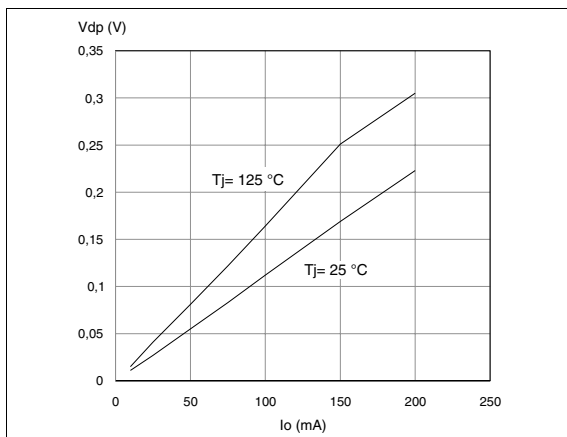


Figure 6. Current consumption vs. Output Current

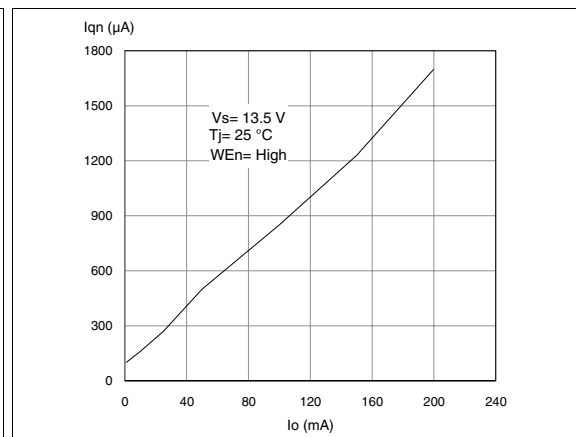


Figure 7. Current consumption vs. Input Voltage

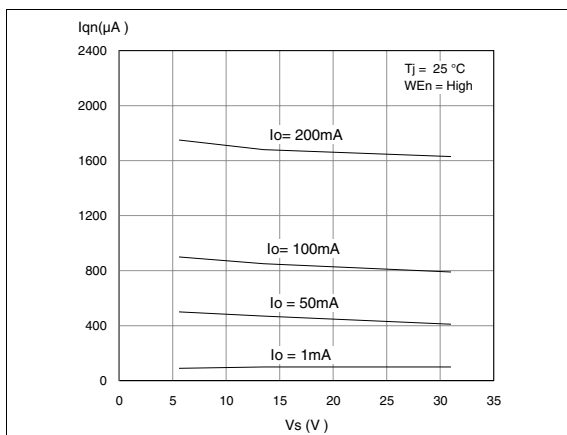


Figure 8. Current limitation vs. Tj

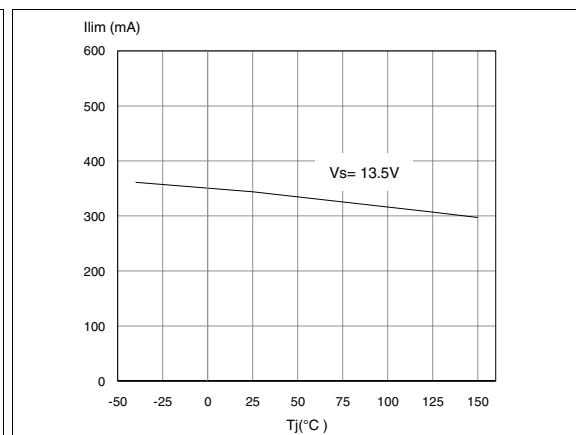


Figure 9. Current limitation vs. Input Voltage      Figure 10. Short Circuit Current vs. Tj

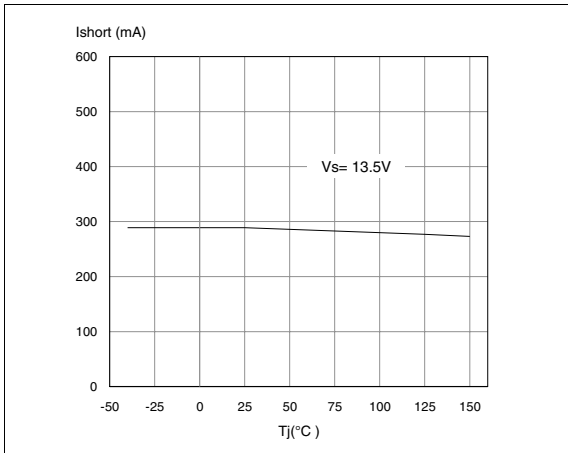
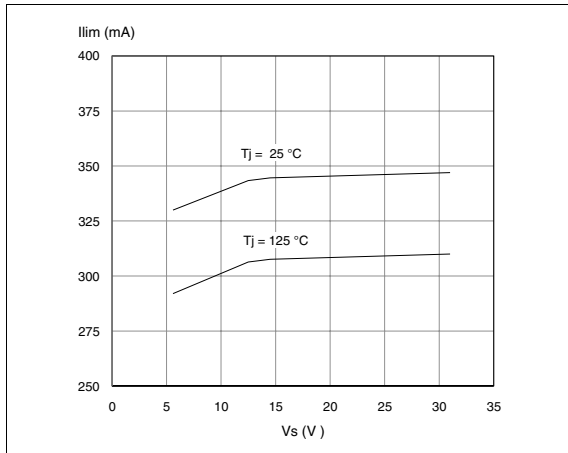


Figure 11. Short Circuit Current vs. Input Voltage

Figure 12. VwEn\_high vs. Tj

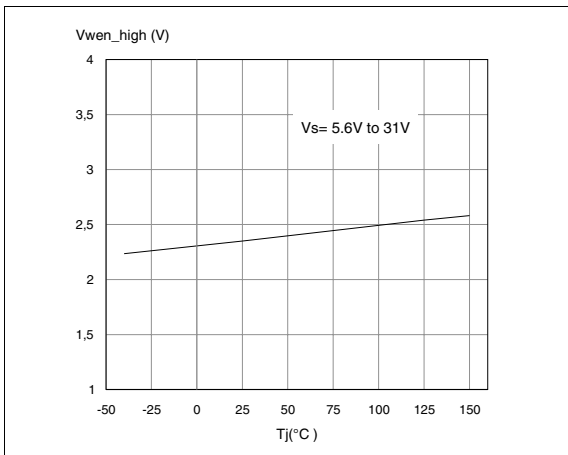
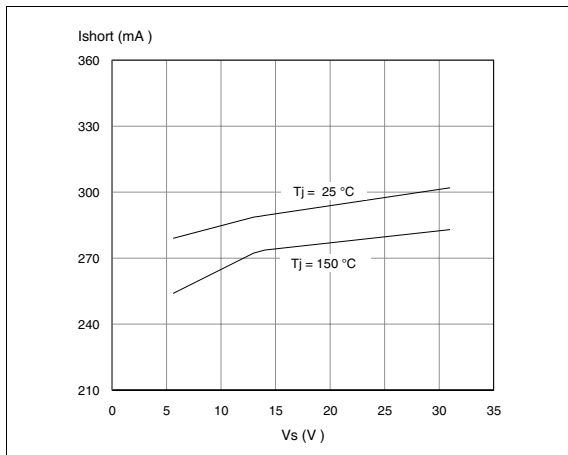


Figure 13. VwEN\_LOW vs. Tj

Figure 14. Vrhth vs. Tj

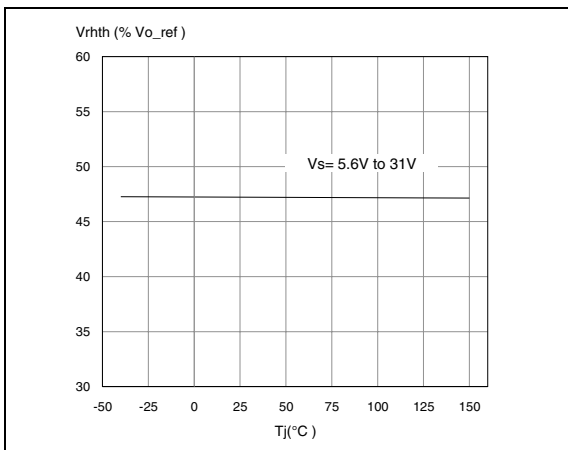
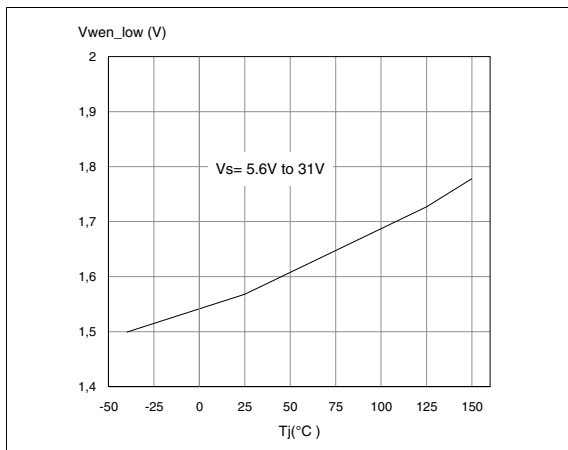


Figure 15. Vrth vs. Tj

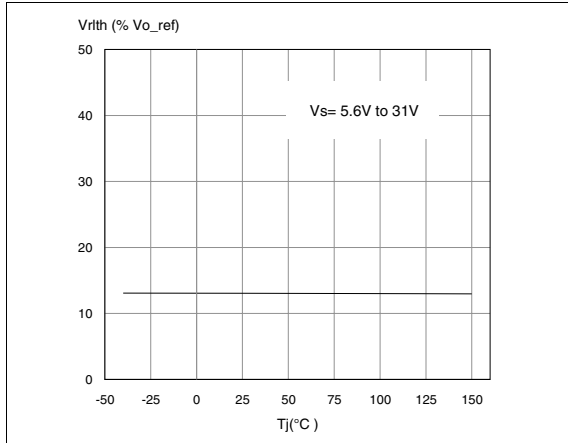


Figure 16. Vwth vs. Tj

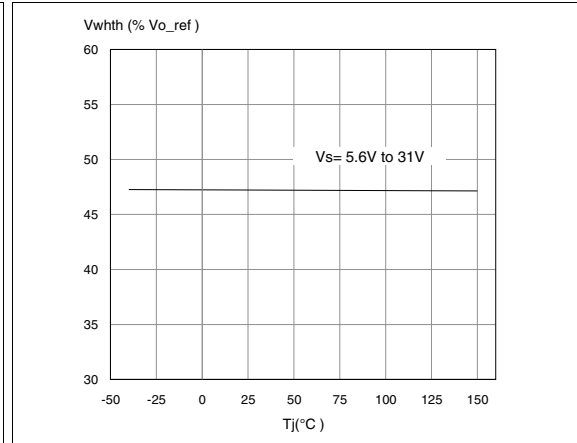


Figure 17. Vwth vs. Tj

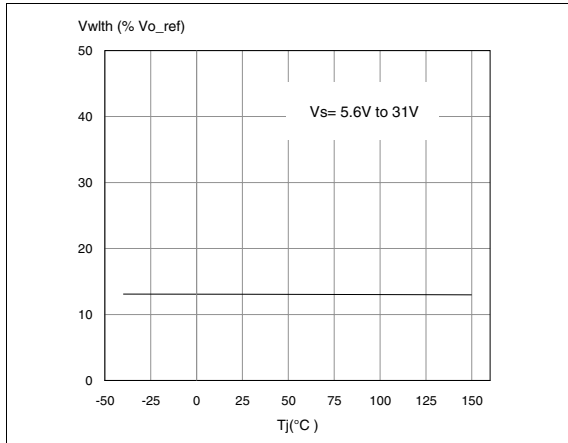


Figure 18. Icr & Icw vs. Tj

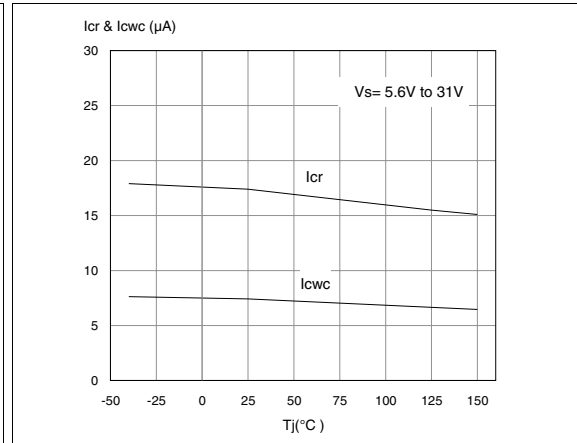


Figure 19. Idr & Icwd vs. Tj

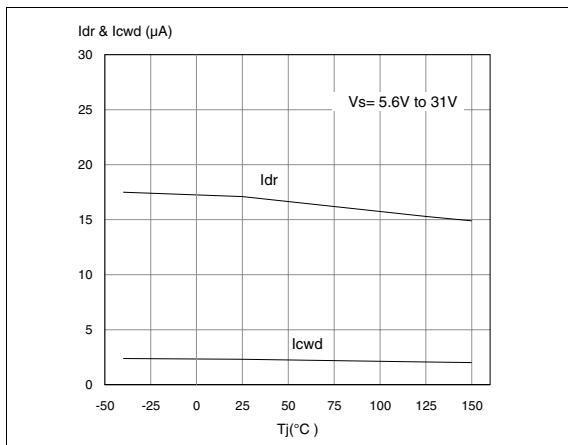


Figure 20. Twop vs. Tj

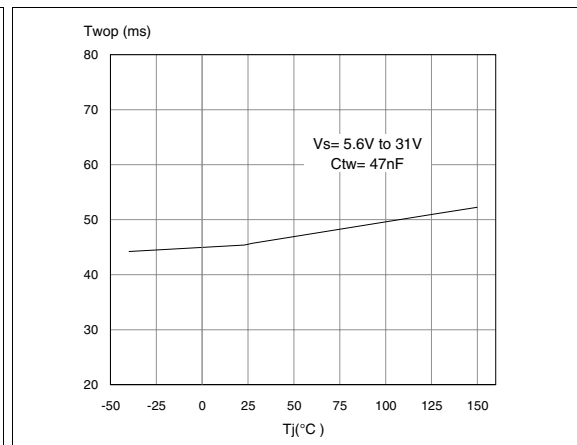
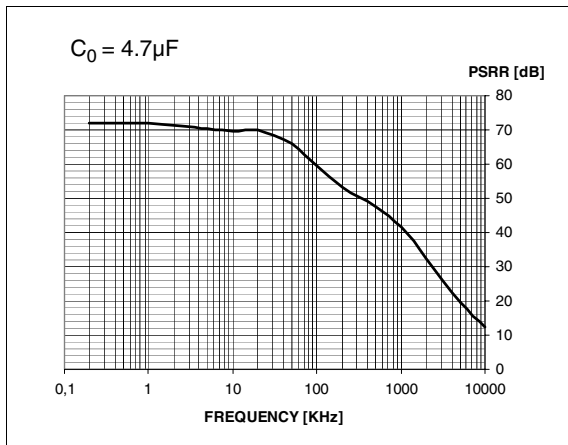


Figure 21. PSRR



## 2.5 Test circuit and waveforms plot

### 2.5.1 Load regulation

Figure 22. Load regulation test circuit

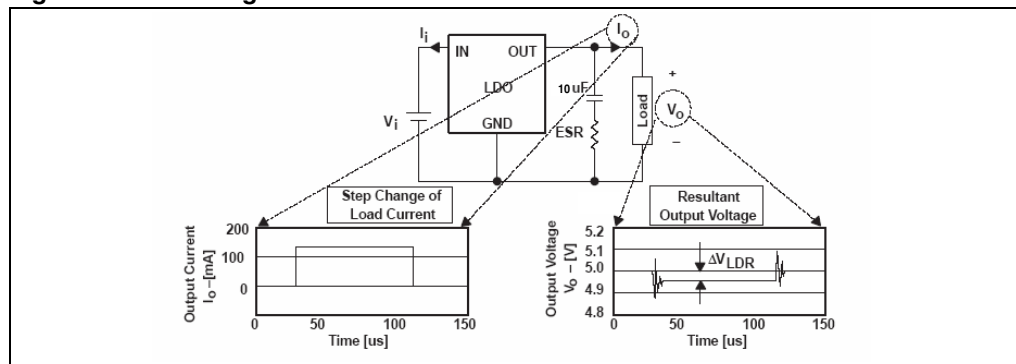
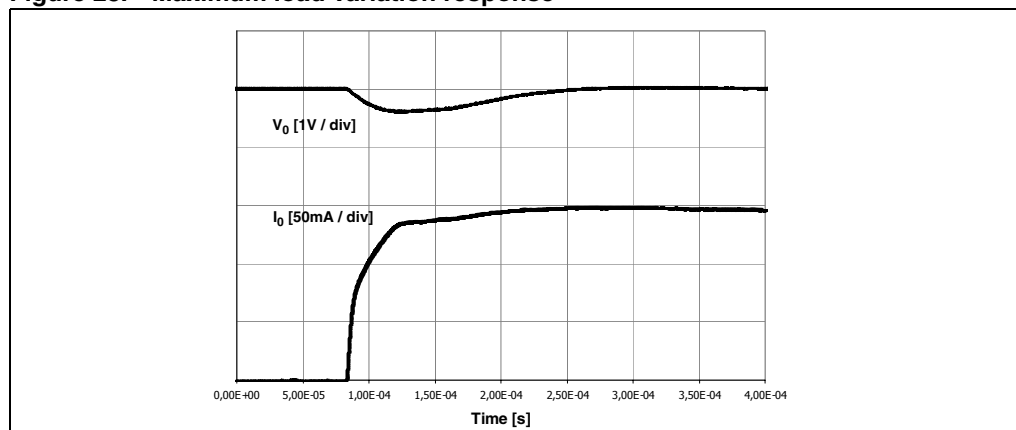
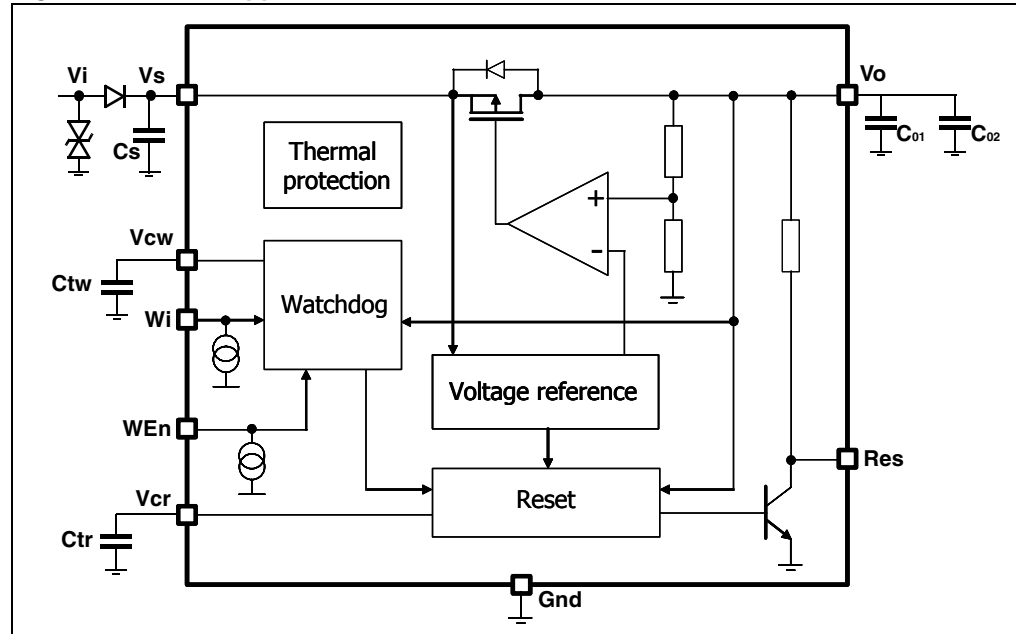


Figure 23. Maximum load variation response



### 3 Application information

Figure 24. L4988 application schematic

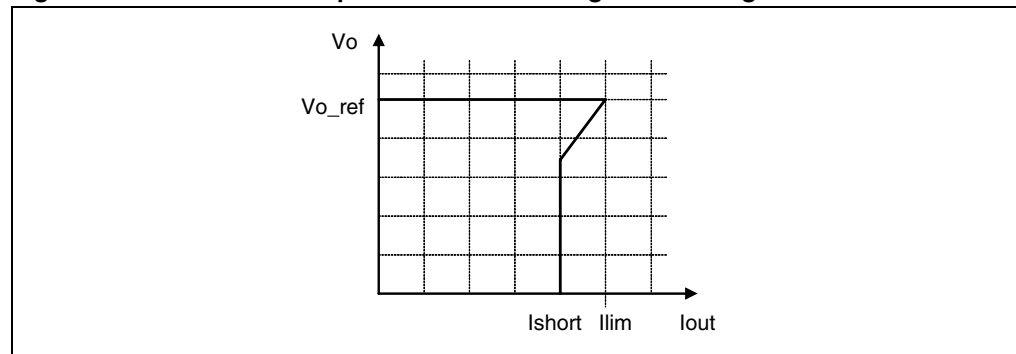


Note: The input capacitor  $C_s > 200\text{nF}$  is necessary for the smoothing of line disturbances. The output capacitor  $C_{01} > 100\text{nF}$  is necessary for the stability of the regulation loop. In order to damp output voltage oscillations during high load current surges, it is recommended to put an additional electrolytic capacitor  $C_{02} > 10\mu\text{F}$  at the output pin.

#### 3.1 Voltage regulator

Voltage regulator uses a p-channel mos transistor as a regulating element. With this structure a very low dropout voltage at currents up to 200mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated. A short circuit protection to GND is provided. The high precision of the output voltage is obtained with a pre-trimmed reference voltage.

Figure 25. Behavior of output current versus regulated voltage  $V_o$



## 3.2 Reset

The reset circuit supervises the output voltage  $V_o$ . The  $V_{o\_th}$  reset threshold is defined with the in-internal reference voltage and a resistor output divider. If the output voltage becomes lower than  $V_{o\_th}$  then Res goes low with a reaction time  $t_{rr}$ . The reset low signal is guaranteed for an output voltage  $V_o$  greater than 1V.

When the output voltage becomes higher than  $V_{o\_th}$  then Res goes high with a delay  $t_{rd}$ . This delay is obtained by an internal oscillator.

The oscillator period is given by:

$$T_{osc} = [(V_{rhth} - V_{rlth}) \times C_{tr}] / I_{cr} + [(V_{rhth} - V_{rlth}) \times C_{tr}] / I_{dr}$$

where:

$I_{cr}$ : is an internally generated charge current

$I_{dr}$ : is an internally generated discharge current

$V_{rhth}$ ,  $V_{rlth}$ : are two voltages defined with the output voltage and a resistor output divider

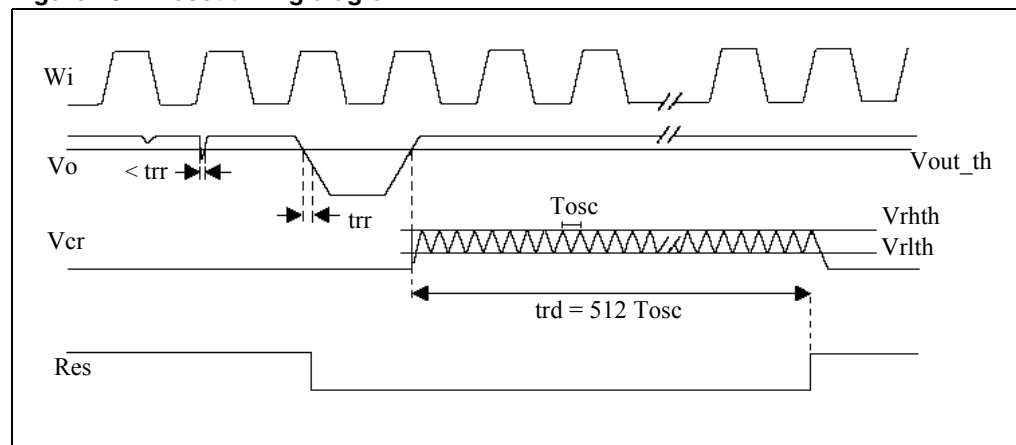
$C_{tr}$ : is an external capacitance.

$t_{rd}$  is given by:

$$t_{rd} = 512 \times T_{osc}$$

Reset is active when  $En$  is high.

**Figure 26. Reset timing diagram**





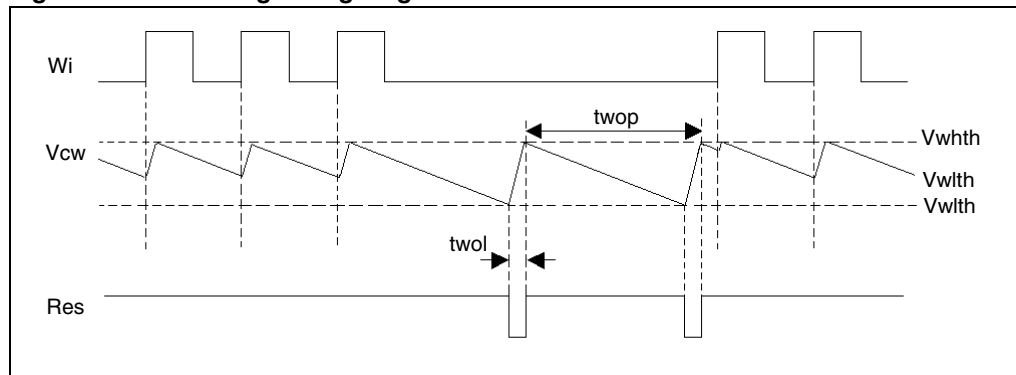
### 3.3 Watchdog

A connected microcontroller is monitored by the watchdog input  $W_i$ . If pulses are missing, the Reset output pin is set to low. The pulse sequence time can be set within a wide range with the external capacitor,  $C_{tw}$ . The watchdog circuit discharges the capacitor  $C_{tw}$ , with the constant current  $I_{cwd}$ . If the lower threshold  $V_{wlth}$  is reached, a watchdog reset is generated. To prevent this the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold  $V_{wlth}$ . In order to calculate the minimum time  $t$ , during which the micro-controller must output the positive edge, the following equation can be used:

$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{cwd} \times t$$

Every  $W_i$  positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold,  $V_{whth}$ , the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor  $C_{tw}$ .

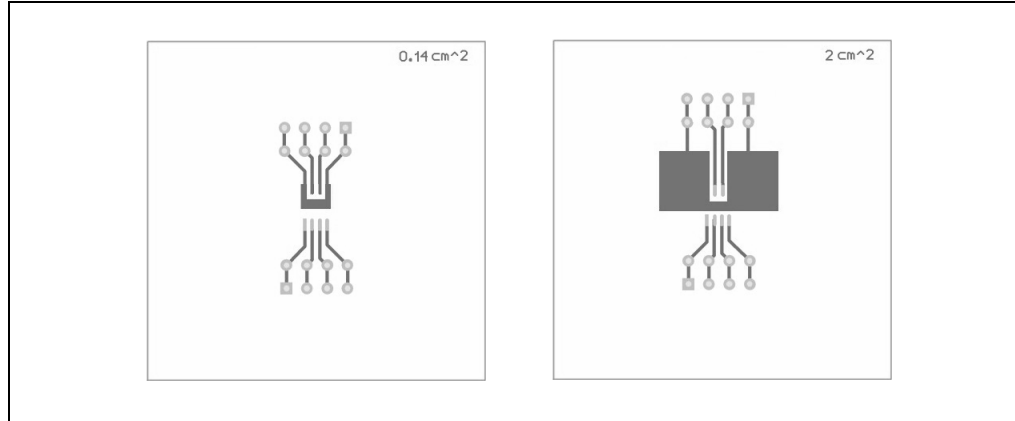
**Figure 27. Watchdog timing diagram**



## 4 Package and PCB thermal data

### 4.1 SO-8 thermal data

Figure 28. SO-8 PC board



Note: *Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area= 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35 $\mu$ m, Copper areas: from minimum pad lay-out to 8cm<sup>2</sup>)*

Figure 29. SO-8  $R_{thj-amb}$  Vs. PCB copper area in open box free air condition

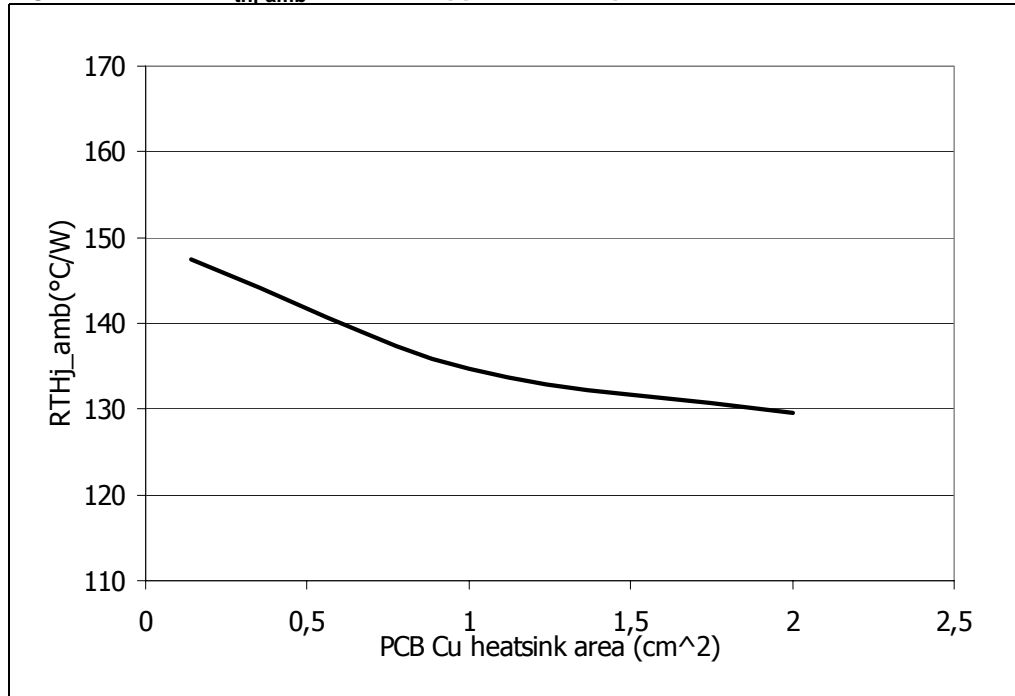
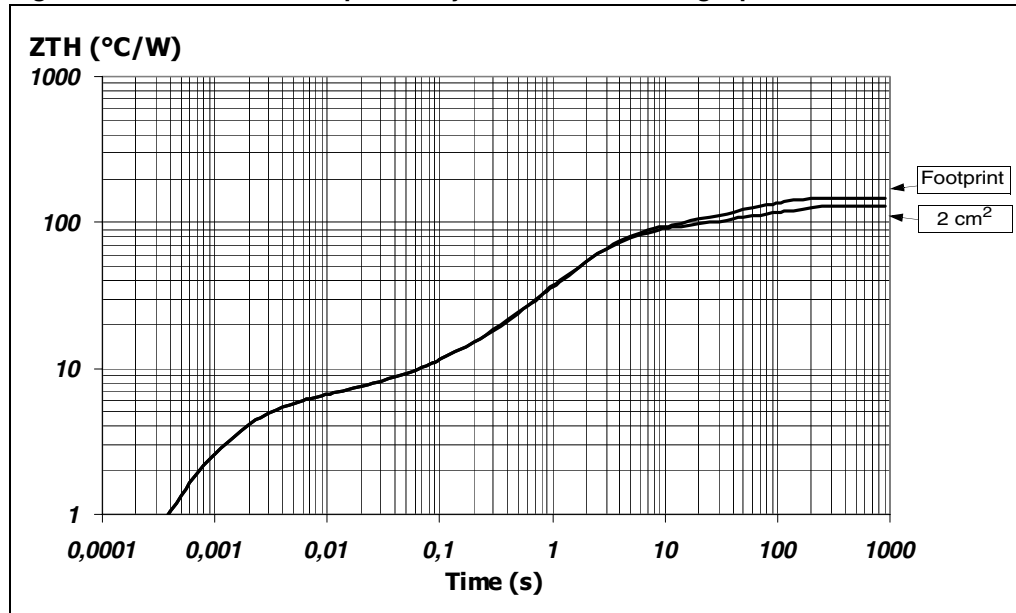


Figure 30. SO-8 thermal impedance junction ambient single pulse

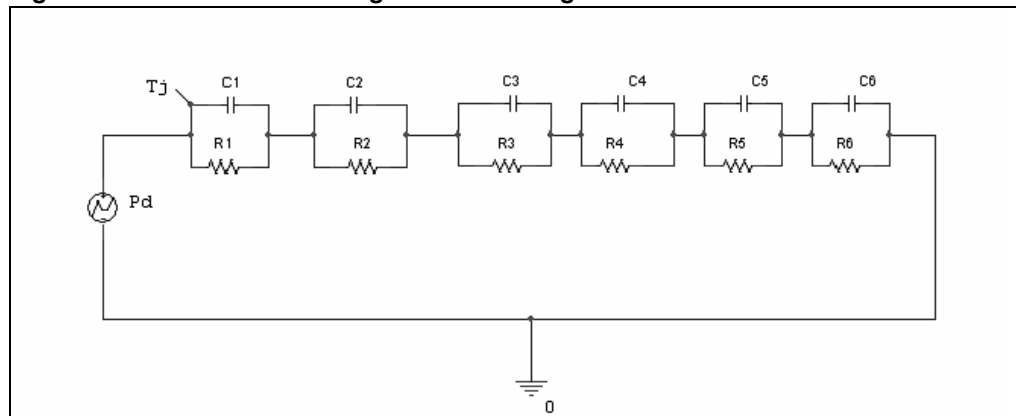


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 31. SO-8 thermal fitting model of a single channel

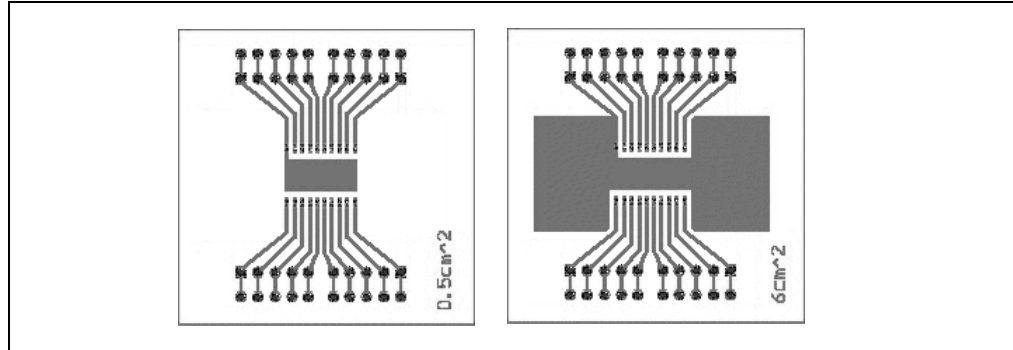


**Table 9. SO-8 thermal parameter**

Area/island (cm <sup>2</sup> )	Footprint	2
R1 (°C/W)	4.21	
R2 (°C/W)	2.11	
R3 (°C/W)	2	
R4 (°C/W)	41	
R5 (°C/W)	40	
R6 (°C/W)	58	40
C1 (W.s/°C)	0.00029	
C2 (W.s/°C)	0.0024	
C3 (W.s/°C)	0.03	
C4 (W.s/°C)	0.04	
C5 (W.s/°C)	0.1	
C6 (W.s/°C)	1.05	2

## 4.2 SO-20 thermal data

Figure 32. SO-20 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area= 58mm x 58mm, PCB thickness = 2mm, Cu thickness=35 $\mu$ m, Copper areas: from minimum pad lay-out to 8cm<sup>2</sup>).

Figure 33. SO-20  $R_{thj-amb}$  Vs. PCB copper area in open box free air condition

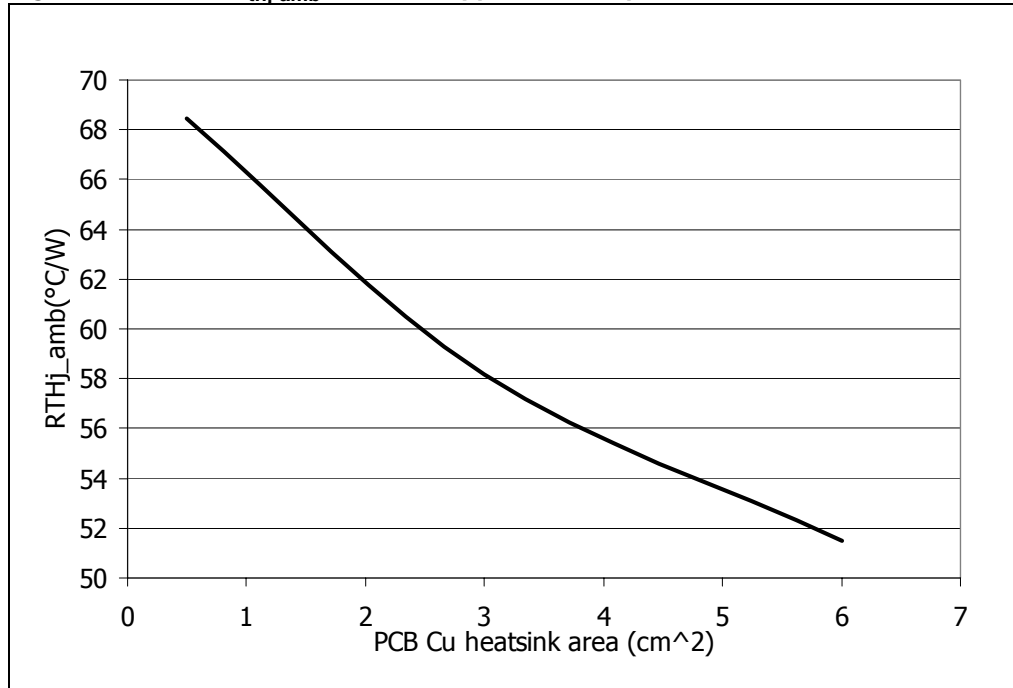
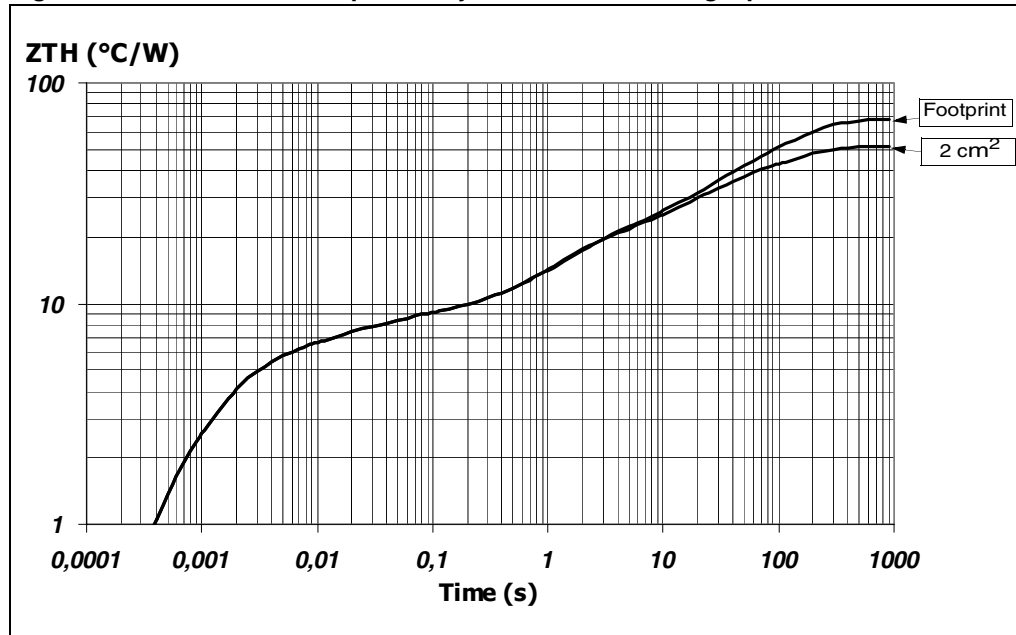


Figure 34. SO-20 thermal impedance junction ambient single pulse

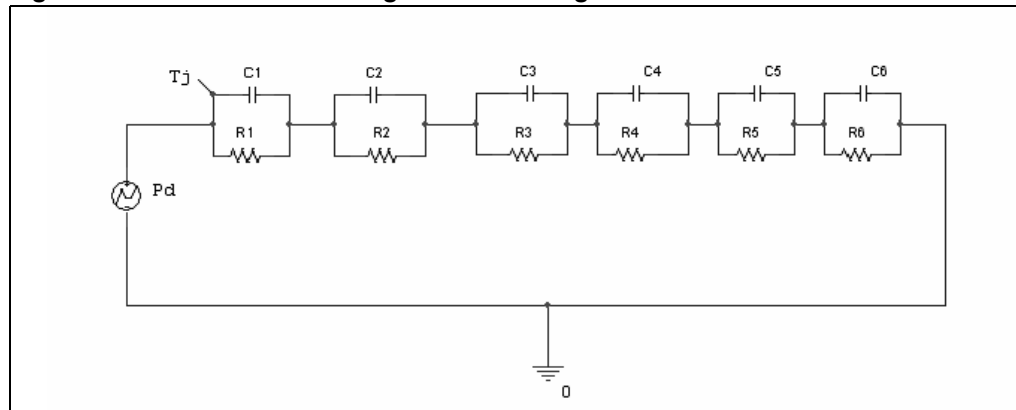


Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 35. SO-20 thermal fitting model of a single channel



**Table 10. SO-20 thermal parameter**

Area/island (cm <sup>2</sup> )	Footprint	2
R1 (°C/W)	4.21	
R2 (°C/W)	2.11	
R3 (°C/W)	2.2	
R4 (°C/W)	10	
R5 (°C/W)	15	
R6 (°C/W)	35	18
C1 (W.s/°C)	0.00029	
C2 (W.s/°C)	0.0024	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.15	
C5 (W.s/°C)	1.5	
C6 (W.s/°C)	4	7

## 5 Package and packing information

### 5.1 ECOPACK<sup>®</sup> packages

In order to meet environmental requirements, ST offers these devices in ECOPACK<sup>®</sup> packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

### 5.2 SO-8 package information

Figure 36. SO-8 package dimensions

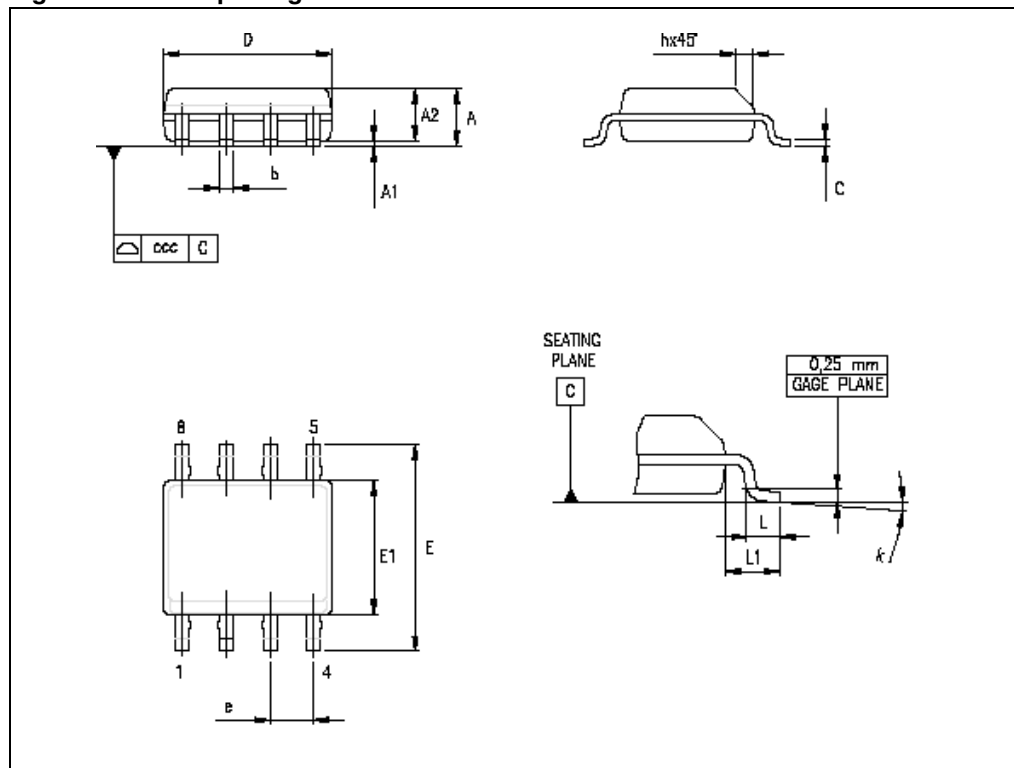




Table 11. SO-8 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D <sup>(1)</sup>	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 <sup>(2)</sup>	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

### 5.3 SO-20 package information

Figure 37. SO-20 package dimensions

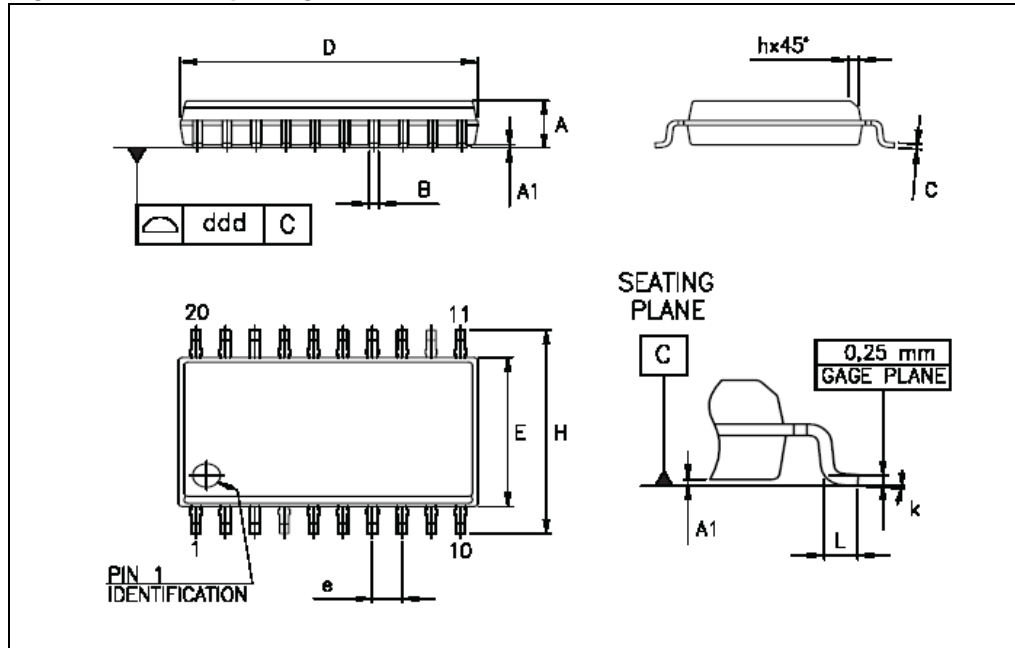


Table 12. SO-20 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D <sup>(1)</sup>	12.60		13.00
E	7.40		7.60
e		1.27	
H	10.0		10.65
h	0.25		0.75
L	0.40		1.27
k	0°		8°
ddd			0.10

1. "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

### 5.4 SO-8 packing information

Figure 38. SO-8 tube shipment (no suffix)

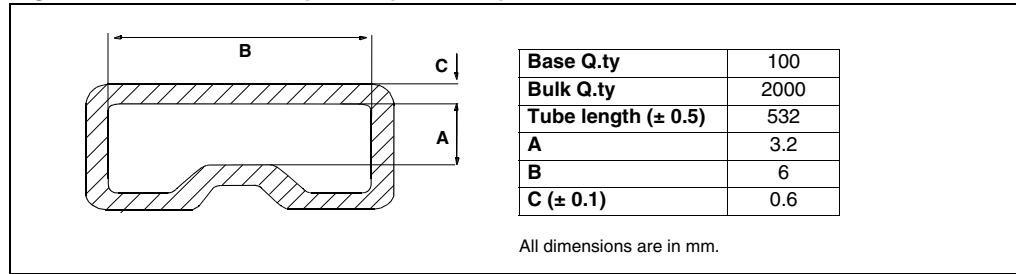
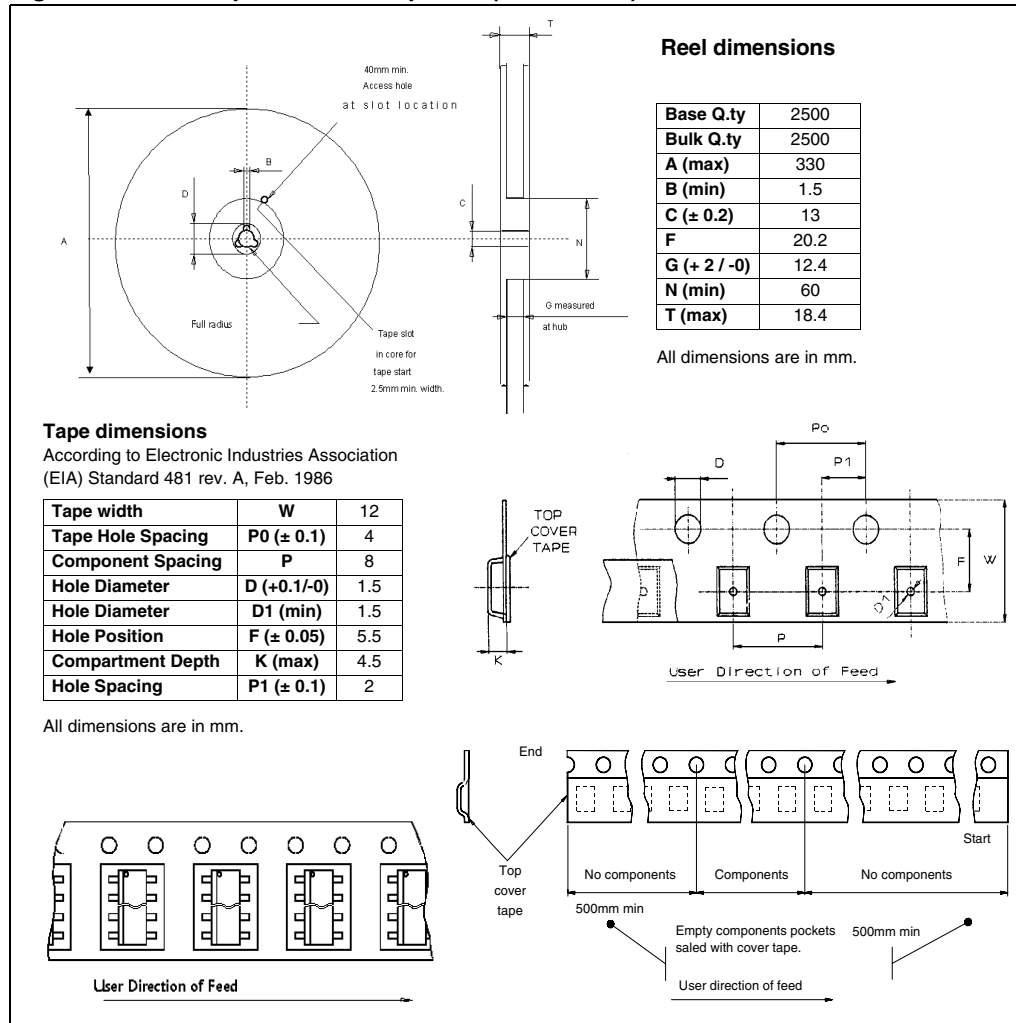


Figure 39. SO-8 tape and reel shipment (suffix "TR")



### 5.5 SO-20 packing information

Figure 40. SO-20 tube shipment (no suffix)

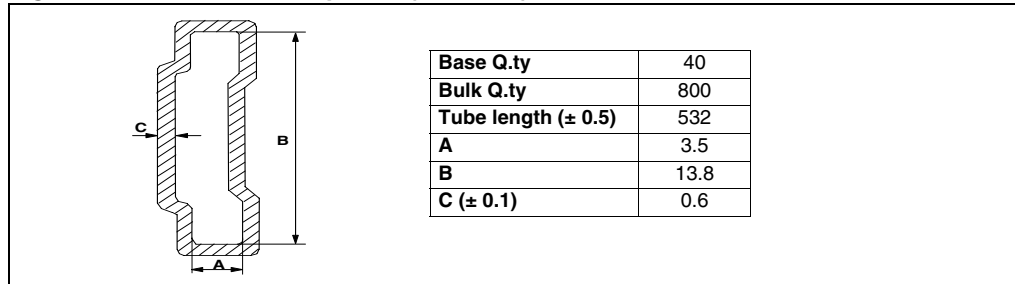
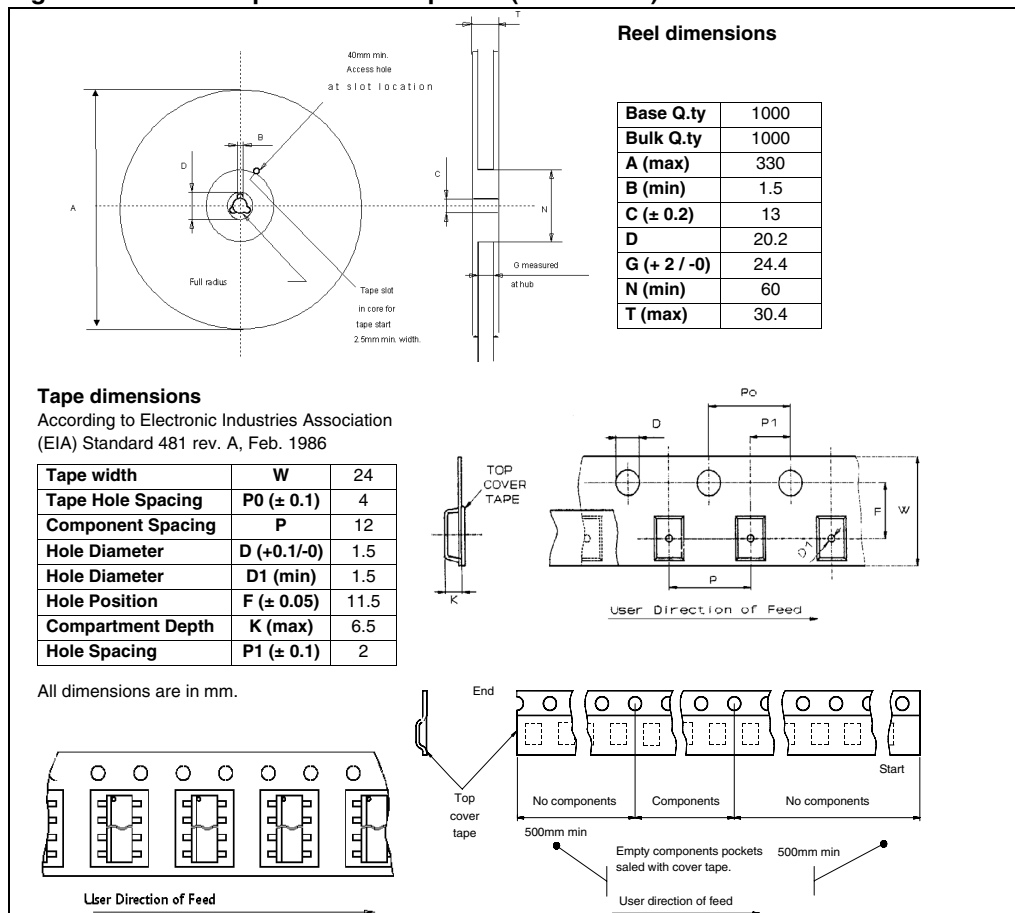


Figure 41. SO-20 tape and reel shipment (suffix “TR”)



## 6 Revision history

Table 13. Document revision history

Date	Revision	Changes
01-Jun-2007	1	Initial release
30-Aug-2007	2	Added features table. Added list of tables and figures. Updated <a href="#">Section 2.3: Electrical characteristics</a> . Added <a href="#">Section 4: Package and PCB thermal data</a> . Added <a href="#">SO-8 packing information</a> and <a href="#">SO-20 packing information</a> .
13-Feb-2008	3	Update <a href="#">Section 2.3: Electrical characteristics</a> .
04-Jun-2008	4	Document restructured. Changed <a href="#">Figure 1: Block diagram</a> . Updated features table on cover page: changed quiescent current value from 80 to 75 $\mu$ A. Updated <a href="#">Table 5: General</a> : <ul style="list-style-type: none"> <li>– changed <math>I_{short}</math> typical value from 250 to 280 mA</li> <li>– changed <math>I_{qn\_50}</math> typical value from 550 to 500 <math>\mu</math>A</li> <li>– changed <math>I_{q\_1\_we}</math> typical value from 130 to 93 <math>\mu</math>A</li> <li>– changed <math>I_{q\_1\_wd}</math> typical value from 80 to 75 <math>\mu</math>A.</li> </ul> Updated <a href="#">Table 7: Watchdog</a> : <ul style="list-style-type: none"> <li>– changed <math>V_{wlth}</math> values in <math>V_{o\_ref}</math> percentages</li> <li>– changed <math>V_{whth}</math> values in <math>V_{o\_ref}</math> percentages.</li> </ul> Added <a href="#">Figure 24: L4988 application schematic</a> . Added <a href="#">Section 2.4: Electrical characteristics curves</a> . Added <a href="#">Section 2.5: Test circuit and waveforms plot</a> .

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