National Semiconductor

May 2004

# LP3984
# Micropower, 150mA Ultra Low-Dropout CMOS Voltage Regulator in Subminiature 4-I/O micro SMD Package

## General Description

The LP3984 is designed for portable and wireless applications with demanding performance and space requirements.

The LP3984's performance is optimized for battery powered systems to deliver extremely low dropout voltage and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life.

Power supply rejection is better than 60 dB at low frequencies and starts to roll off at 10 kHz. High power supply rejection is maintained down to low input voltage levels common to battery operated circuits.

The device is ideal for mobile phone and similar battery powered wireless applications. It provides up to 150 mA from a 2.5V to 6V input. The LP3984 consumes less than 1.2µA in disable mode and has fast turn-on time less than 20µs.

The LP3984 is available in a 4 bump micro SMD and 5 pin SOT-23 package. Performance is specified for −40˚C to +125˚C temperature range and is available in 1.5V, 1.8V, 2.0V, 2.9V and 3.1V output voltages. For other output voltage options from 1.5V to 3.5V, please contact National Semiconductor sales office.

## Key Specifications

- 2.5 to 6.0V input range
- 150mA guaranteed output
- 60dB PSRR at 1kHz, 40dB at 10kHz @ $3.1V_{IN}$
- ≤1.2µA quiescent current when shut down
- Fast Turn-On time: 20 µs (typ.)
- 75mV typ dropout with 150mA load
- −40 to +125˚C junction temperature range for operation
- 1.5V, 1.8V, 2.0V, 2.9V and 3.1V

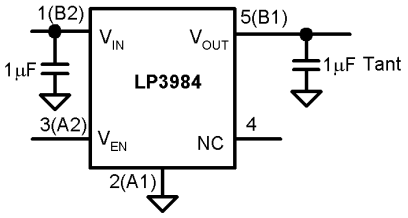
## Features

- Miniature 4-I/O micro SMD and SOT-23-5 package
- Logic controlled enable
- Stable with tantalum capacitors
- 1 µF Tantalum output capacitor
- Fast turn-on
- Thermal shutdown and short-circuit current limit

## Applications

- CDMA cellular handsets
- Wideband CDMA cellular handsets
- GSM cellular handsets
- Portable information appliances

## Typical Application Circuit

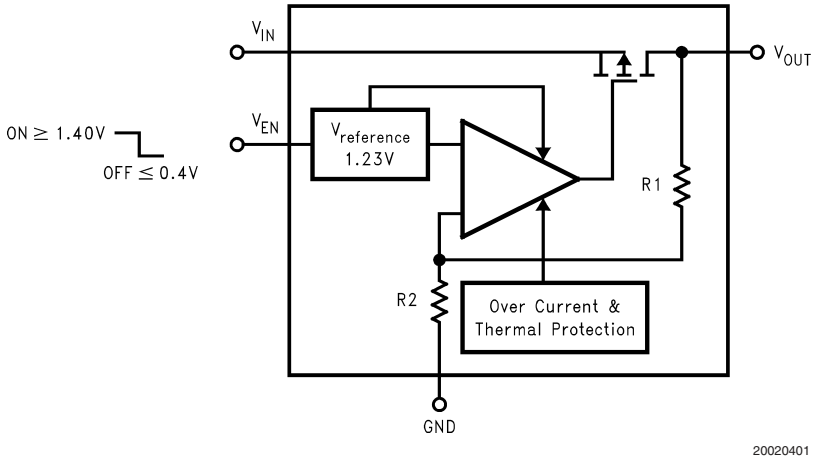



20020402

Note: Pin Numbers in parenthesis indicate micro SMD package.

## Block Diagram



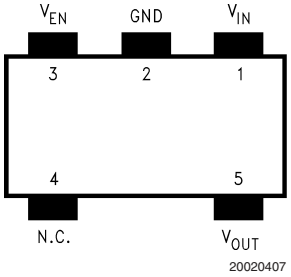

## Pin Descriptions

| Name | * micro SMD | SOT | Function |
|---|---|---|---|
| $V_{EN}$ | A2 | 3 | Enable Input Logic, Enable High |
| GND | A1 | 2 | Common Ground |
| $V_{OUT}$ | B1 | 5 | Output Voltage of the LDO |
| $V_{IN}$ | B2 | 1 | Input Voltage of the LDO |
| N.C. | | 4 | No Connection |

* Note: The pin numbering scheme for the micro SMD package was revised in April, 2002 to conform to JEDEC standard. Only the pin numbers were revised. No hcanges to the physical locations of the inputs/outputs wre made. For reference purposes, the obsolete numbering scheme had GND as pin 1, $V_{OUT}$ as pin 2, $V_{IN}$ as pin 3 and $V_{EN}$ as pin 4.

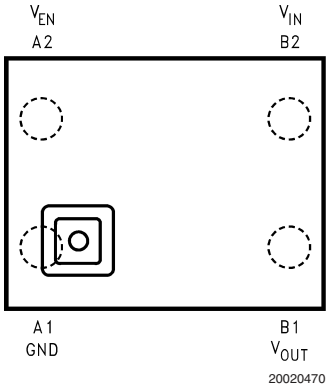
## Connection Diagrams

**SOT-23-5 Package**




**Top View**
**See NS Package Number MF05A**

**micro SMD, 4 Bump Package**




**Top View**
**See NS Package Number BPA04**

## Ordering Information

**For thin micro SMD Package (0.500mm height)**

| Output Voltage (V) | Grade | LP3984 Supplied as 250 Units, Tape and Reel | LP3984 Supplied as 3000 Units, Tape and Reel |
|---|---|---|---|
| 1.8 | STD | LP3984ITP-1.8 | LP3984ITPX-1.8 |
| 2.9 | STD | LP3984ITP-2.9 | LP3984ITPX-2.9 |

**For micro SMD Package (0.995mm height)**

| Output Voltage (V) | Grade | LP3984 Supplied as 250 Units, Tape and Reel | LP3984 Supplied as 3000 Units, Tape and Reel |
|---|---|---|---|
| 1.5 | STD | LP3984IBP-1.5 | LP3984IBPX-1.5 |
| 1.8 | STD | LP3984IBP-1.8 | LP3984IBPX-1.8 |
| 2.0 | STD | LP3984IBP-2.0 | LP3984IBPX-2.0 |
| 3.1 | STD | LP3984IBP-3.1 | LP3984IBPX-3.1 |

**For SOT Package**

| Output Voltage (V) | Grade | LP3984 Supplied as 1000 Units, Tape and Reel | LP3984 Supplied as 3000 Units, Tape and Reel | Package Marking |
|---|---|---|---|---|
| 1.5 | STD | LP3984IMF-1.5 | LP3984IMFX-1.5 | LEAB |
| 1.8 | STD | LP3984IMF-1.8 | LP3984IMFX-1.8 | LEBB |
| 2.0 | STD | LP3984IMF-2.0 | LP3984IMFX-2.0 | LECB |
| 3.1 | STD | LP3984IMF-3.1 | LP3984IMFX-3.1 | LEDB |

## Absolute Maximum Ratings (Notes 1, 2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| $V_{IN}$, $V_{EN}$ | −0.3 to 6.5V |
| $V_{OUT}$ | -0.3 to ($V_{IN}$+0.3) ≤ 6.5V |
| Junction Temperature | 150˚C |
| Storage Temperature | −65˚C to +150˚C |
| Lead Temp. | 235˚C |
| Pad Temp. (Note 3) | 235˚C |
| Maximum Power Dissipation(Note 4) | |
| SOT23-5 | 364mW |
| Micro SMD | 235mW |
| ESD Rating(Note 5) | |
| Human Body Model | 2kV |
| Machine Model | 200V |

## Operating Ratings (Notes 1, 2)

| | |
|---|---|
| $V_{IN}$ | 2.5 to 6V |
| $V_{EN}$ | 0 to ($V_{IN}$+0.3V) ≤ 6V |
| Junction Temperature | −40˚C to +125˚C |
| Thermal Resistance | |
| $\theta_{JA}$ (SOT23-5) | 220˚C/W |
| $\theta_{JA}$ (micro SMD) | 340˚C/W |
| Maximum Power Dissipation (Note 6) | |
| SOT23-5 | 250mW |
| micro SMD | 160mW |

## Electrical Characteristics

Unless otherwise specified: $V_{IN}$ = 2.5V for 1.5, 1.8, & 2.0V options, $V_{IN}$ = $V_{OUT}$ + 0.5 for output options higher than 2.5V, $C_{IN}$ = 1 µF, $I_{OUT}$ = 1mA, $C_{OUT}$ = 1 µF, tantalum. Typical values and limits appearing in standard typeface are for $T_J$ = 25˚C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40˚C to +125˚C. (Note 7) (Note 8)

| Symbol | Parameter | Conditions | Typ | Limit | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $\Delta V_{OUT}$ | Output Voltage Tolerance | | | −1.2<br>**−2.0** | 1.2<br>**2.0** | % of $V_{OUT(nom)}$ |
| | Line Regulation Error | $V_{IN}$ = 2.5V to 4.5V for 1.5, 1.8, 2.0V options<br>$V_{IN}$ = ($V_{OUT}$ + 0.5V) to 4.5V for Voltage options higher than 2.5V | 0.05 | **−0.15** | **0.15** | %/V |
| | Load Regulation Error (Note 9) | $I_{OUT}$ = 1 mA to 150 mA<br>LP3984IM5 (SOT23-5) | 0.002 | | **0.005** | %/mA |
| | | LP3984IBP (micro SMD) | 0.0009 | | **0.002** | |
| PSRR | Power Supply Rejection Ratio | $V_{IN}$ = $V_{OUT(nom)}$ + 0.2V,<br>f = 1 kHz,<br>$I_{OUT}$ = 50 mA (*Figure 2*) | 60 | | | dB |
| | | $V_{IN}$ = $V_{OUT(nom)}$ + 0.2V,<br>f = 10 kHz,<br>$I_{OUT}$ = 50 mA (*Figure 2*) | 40 | | | |
| $I_Q$ | Quiescent Current | $V_{EN}$ = 1.4V, $I_{OUT}$ = 0 mA | 80 | | **125** | µA |
| | | $V_{EN}$ = 1.4V, $I_{OUT}$ = 0 to 150 mA | 110 | | **150** | |
| | | $V_{EN}$ = 0.4V | 0.005 | | **1.2** | |
| | Dropout Voltage (Note 10) | $I_{OUT}$ = 1 mA | 0.6 | | **2.5** | mV |
| | | $I_{OUT}$ = 50 mA | 25 | | **40** | |
| | | $I_{OUT}$ = 100 mA | 50 | | **80** | |
| | | $I_{OUT}$ = 150 mA | 75 | | **120** | |
| $I_{SC}$ | Short Circuit Current Limit | Output Grounded (Steady State) | 600 | | | mA |
| $I_{OUT(PK)}$ | Peak Output Current | $V_{OUT}$ ≥ $V_{OUT(nom)}$ - 5% | 600 | **300** | | mA |
| $T_{ON}$ | Turn-On Time (Note 11) | | 20 | | | µs |
| $e_n$ | Output Noise Voltage | BW = 10 Hz to 100 kHz,<br>$C_{OUT}$ = 1µF tant. | 90 | | | µVrms |
| $I_{EN}$ | Maximum Input Current at EN | $V_{EN}$ = 0.4 and $V_{IN}$ = 6.0 | ±1 | | | nA |

## Electrical Characteristics (Continued)

Unless otherwise specified: $V_{IN}$ = 2.5V for 1.5, 1.8, & 2.0V options, $V_{IN}$ = $V_{OUT}$ + 0.5 for output options higher than 2.5V, $C_{IN}$ = 1 µF, $I_{OUT}$ = 1mA, $C_{OUT}$ = 1 µF, tantalum. Typical values and limits appearing in standard typeface are for $T_J$ = 25˚C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40˚C to +125˚C. (Note 7) (Note 8)

| Symbol | Parameter | Conditions | Typ | Limit | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{IL}$ | Maximum Low Level Input Voltage at EN | $V_{IN}$ = 2.5 to 6.0V | | | **0.4** | V |
| $V_{IH}$ | Minimum High Level Input Voltage at EN | $V_{IN}$ = 2.5 to 6.0V | | **1.4** | | V |
| $C_{OUT}$ | Output Capacitor | Capacitance | | **1** | **22** | µF |
| | | ESR | | **2** | **10** | Ω |
| TSD | Thermal Shutdown Temperature | | 160 | | | ˚C |
| | Thermal Shutdown Hysteresis | | 20 | | | ˚C |

**Note 1:** Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

**Note 2:** All voltages are with respect to the potential at the GND pin.

**Note 3:** Additional information on pad temperature can be found in National Semiconductor Application Note (AN-1112).

**Note 4:** The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula: $P_D = (T_J - T_A)/\theta_{JA}$,

where $T_J$ is the junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance. The 364mW rating for SOT23-5 appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, 150˚C, for $T_J$, 70˚C for $T_A$, and 220˚C/W for $\theta_{JA}$. More power can be dissipated safely at ambient temperatures below 70˚C . Less power can be dissipated safely at ambient temperatures above 70˚C. The Absolute Maximum power dissipation for SOT23-5 can be increased by 4.5mW for each degree below 70˚C, and it must be derated by 4.5mW for each degree above 70˚C.

**Note 5:** The human body model is 100pF discharged through 1.5kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

**Note 6:** Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. The 250mW rating for SOT23-5 appearing under Operating Ratings results from substituting the maximum junction temperature for operation, 125˚C, for $T_J$, 70˚C for $T_A$, and 220˚C/W for $\theta_{JA}$ into (Note 4) above. More power can be dissipated at ambient temperatures below 70˚C . Less power can be dissipated at ambient temperatures above 70˚C. The maximum power dissipation for operation can be increased by 4.5mW for each degree below 70˚C, and it must be derated by 4.5mW for each degree above 70˚C.

**Note 7:** All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with $T_J$ = 25˚C or correlated using Statistical Quality Control (SQC) methods. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

**Note 8:** The target output voltage, which is labeled $V_{OUT(nom)}$, is the desired voltage option.

**Note 9:** An increase in the load current results in a slight decrease in the output voltage and vice versa.

**Note 10:** Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. This specification does not apply for input voltages below 2.5V.

**Note 11:** Turn-on time is time measured between the enable input just exceeding $V_{IH}$ and the output voltage just reaching 95% of its nominal value.

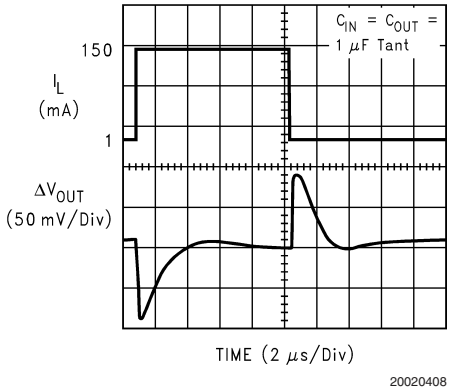



**FIGURE 1. Line Transient Input Test Signal**

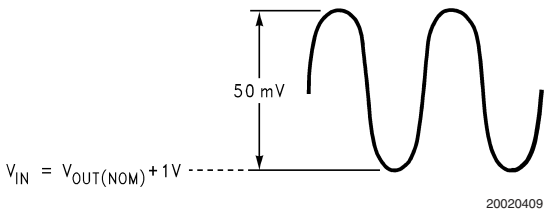
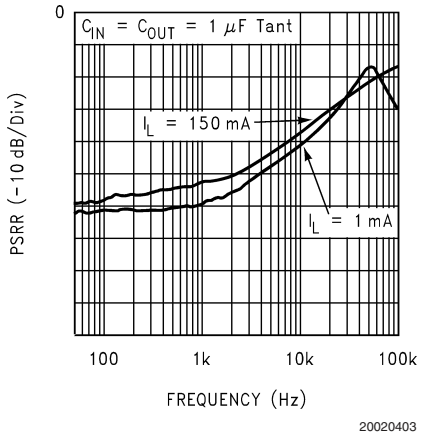



**FIGURE 2. PSRR Input Test Signal**

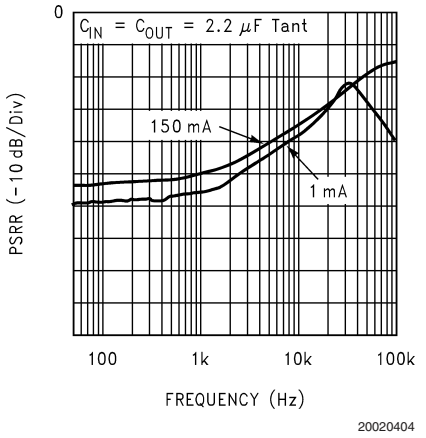
## Typical Performance Characteristics

Unless otherwise specified, $C_{IN}$ = $C_{OUT}$ = 1 µF Tantalum, $V_{IN}$ = 2.5 for 1.5, 1.8, and 2.0V options, $V_{IN}$ = $V_{OUT}$ + 0.2V for output options higher than 2.5V, $T_A$ = 25˚C, Enable pin is tied to $V_{IN}$.

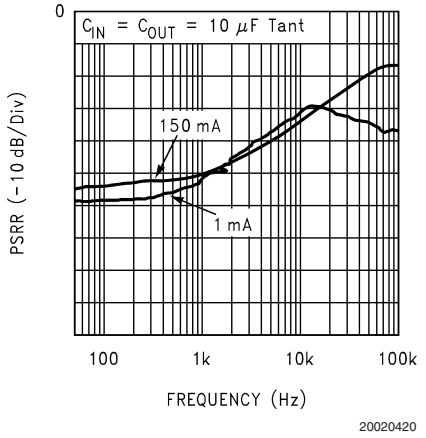
**Power Supply Rejection Ratio ($V_{IN}$ = 3.5V)**



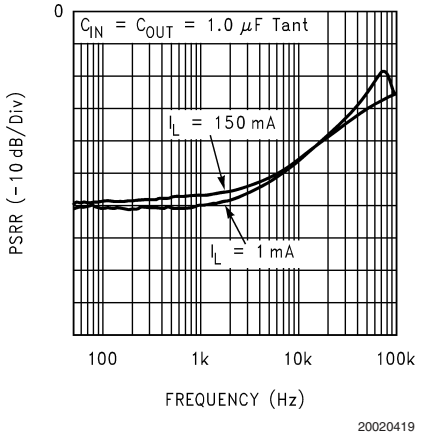

**Power Supply Rejection Ratio ($V_{IN}$ = 3.5V)**




**Power Supply Rejection Ratio ($V_{IN}$ = 3.5V)**



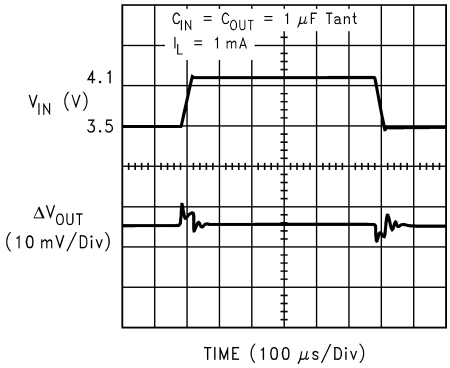

**Power Supply Rejection Ratio (LP3984-1.5, $V_{IN}$ = 2.5V)**



## Typical Performance Characteristics

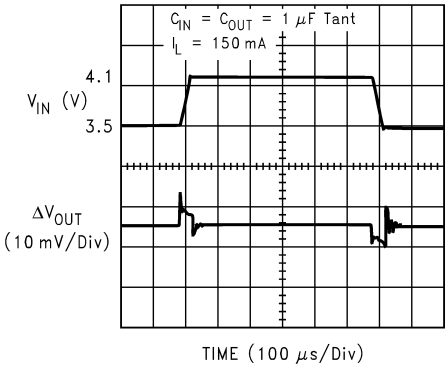
Unless otherwise specified, $C_{IN} = C_{OUT} = 1\ \mu F$ Tantalum, $V_{IN} = 2.5$ for 1.5, 1.8, and 2.0V options, $V_{IN} = V_{OUT} + 0.2V$ for output options higher than 2.5V, $T_A = 25^{\circ}C$, Enable pin is tied to $V_{IN}$. (Continued)

**Line Transient Response (LP3984-3.1)**



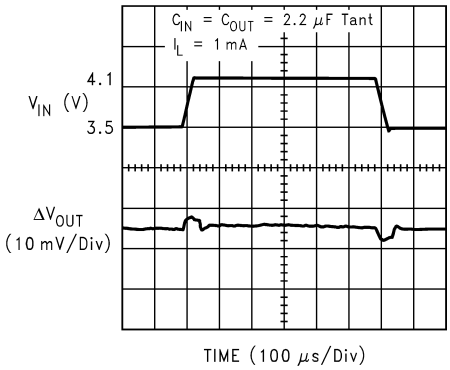

20020418

**Line Transient Response (LP3984-3.1)**



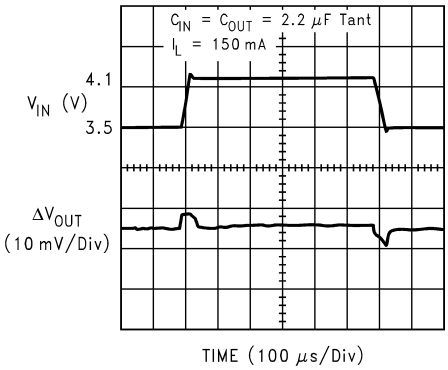

20020417

**Line Transient Response (LP3984-3.1)**



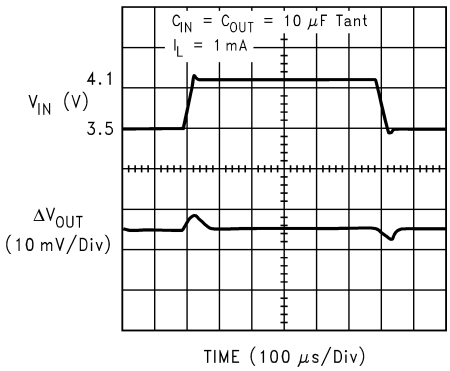

20020416

**Line Transient Response (LP3984-3.1)**



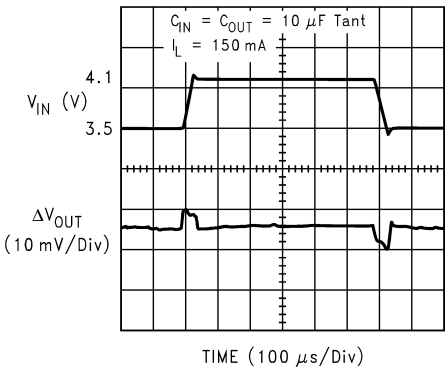

20020415

**Line Transient Response (LP3984-3.1)**




20020414

**Line Transient Response (LP3984-3.1)**

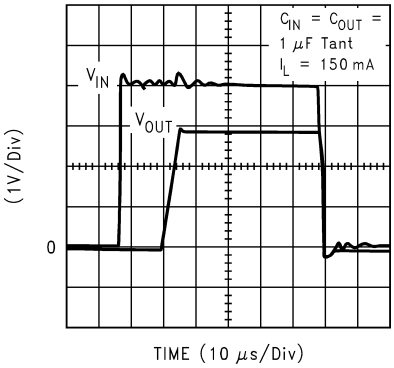



20020413

## Typical Performance Characteristics

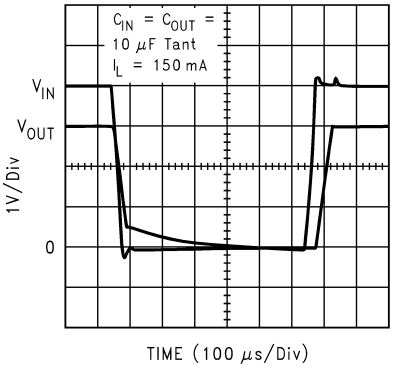
Unless otherwise specified, $C_{IN} = C_{OUT} = 1\ \mu F$ Tantalum, $V_{IN} = 2.5$ for 1.5, 1.8, and 2.0V options, $V_{IN} = V_{OUT} + 0.2V$ for output options higher than 2.5V, $T_A = 25^{\circ}C$, Enable pin is tied to $V_{IN}$. (Continued)

**Start Up Response**



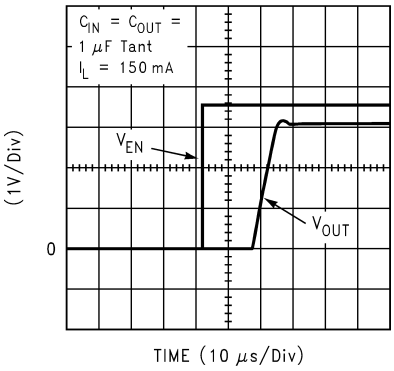

20020412

**Start Up Response**



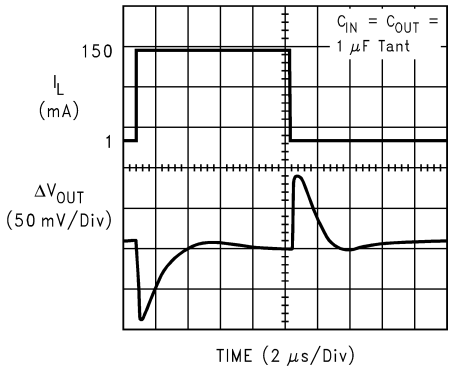

20020411

**Enable Response**



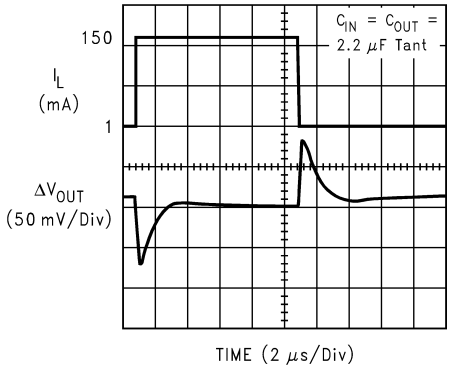

20020410

**Load Transient Response (LP3984-3.1**



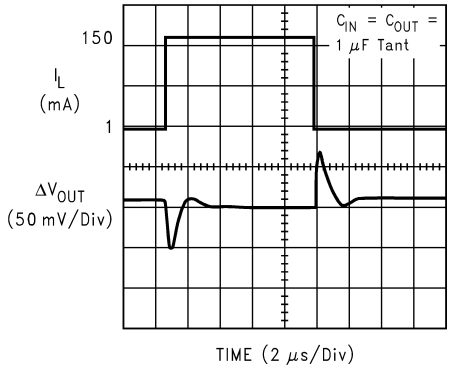

20020408

**Load Transient Response (LP3984-3.1)**




20020406

**Load Transient Response ($V_{IN}$ = 4.2V)**




20020405

# Application Hints

### EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP3984 requires external capacitors for regulator stability. The LP3984 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

### INPUT CAPACITOR

An input capacitance of ≅ 1µF is required between the LP3984 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

**Important:** Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be ≅ 1µF over the entire operating temperature range.

### OUTPUT CAPACITOR

The LP3984 is designed specifically to work with tantalum output capacitors. A tantalum capacitor in 1 to 22 µF range with 2Ω to 10Ω ESR range is suitable in the LP3984 application circuit.

It may also be possible to use film capacitors at the output, but these are not as attractive for reasons of size and cost.

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range (2Ω to 10Ω).

### NO-LOAD STABILITY

The LP3984 will remain stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

### ON/OFF INPUT OPERATION

The LP3984 is turned off by pulling the $V_{EN}$ pin low, and turned on by pulling it high. If this feature is not used, the $V_{EN}$ pin should be tied to $V_{IN}$ to keep the regulator output on at all times. To assure proper operation, the signal source used to drive the $V_{EN}$ input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under $V_{IL}$ and $V_{IH}$.

### FAST ON-TIME

The LP3984 output is turned on after $V_{ref}$ voltage reaches its final value (1.23V nominal). To speed up this process, the noise reduction capacitor at the bypass pin is charged with an internal 70µA current source. The curernt source is turned off when the bandgap voltage reaches approximately 95% of its final value. The turn on time is determined by the time constant of the bypass cpacitor. The smaller the capacitor value, the shorter the turn on time, but less noise gets reduced. As a result, turn on time and noise reduction need to be taken into design consideration when choosing the value of the byupass capacitor.

### MICRO SMD MOUNTING

The micro SMD package requires specific mounting techniques which are detailed in National Semiconductor Application Note (AN-1112). Referring to the section *Surface Mount Technology (SMT) Assembly Considerations*, it should be noted that the pad style which must be used with the 5 pin package is NSMD (non-solder mask defined) type.

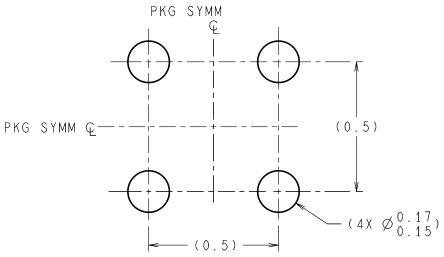
For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the micro SMD device.

### MICRO SMD LIGHT SENSITIVITY

Exposing the micro SMD device to direct sunlight will cause misoperation of the device. Light sources such as halogen lamps can effect electrical performance if brought near to the device.

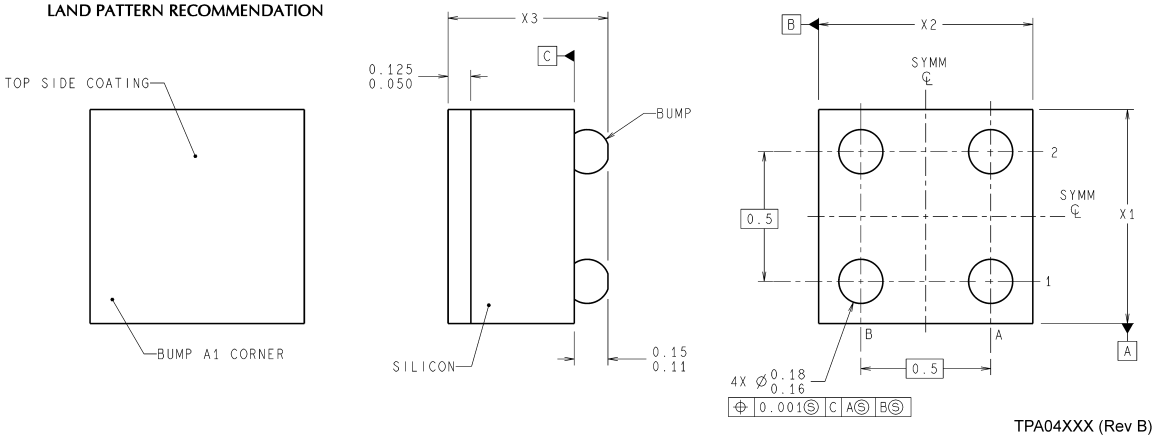
The wavelengths which have most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has very little effect on performance. A micro SMD test board was brought to within 1cm of a fluorescent desk lamp and the effect on the regulated output voltage was negligible, showing a deviation of less than 0.1% from nominal.

## Physical Dimensions inches (millimeters)
unless otherwise noted




DIMENSIONS ARE IN MILLIMETERS

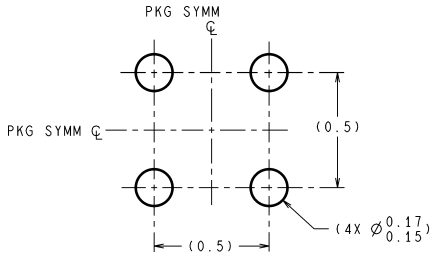
LAND PATTERN RECOMMENDATION




TPA04XXX (Rev B)

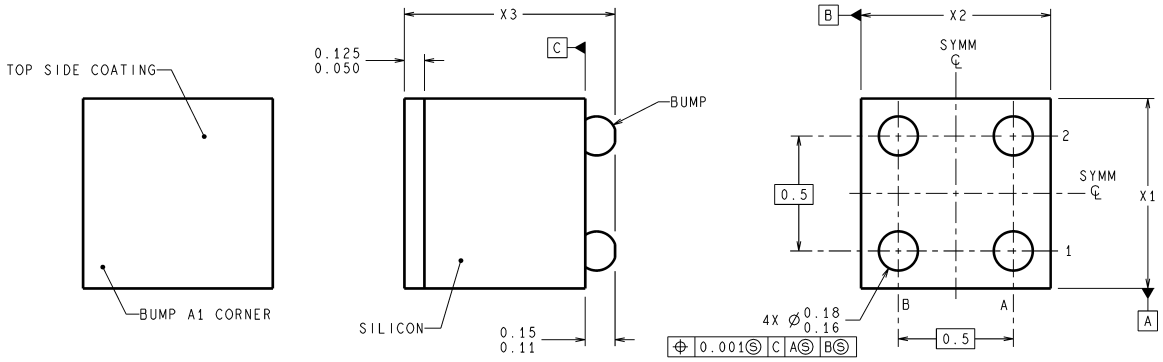
**Micro SMD, 4 Bump Package (TPA04)**
**NS Package Number TPA04EJA**
**X1 = 0.879 ± 0.03mm**
**X2 = 0.980 ± 0.03mm**
**X3 = 0.500 ± 0.075mm**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



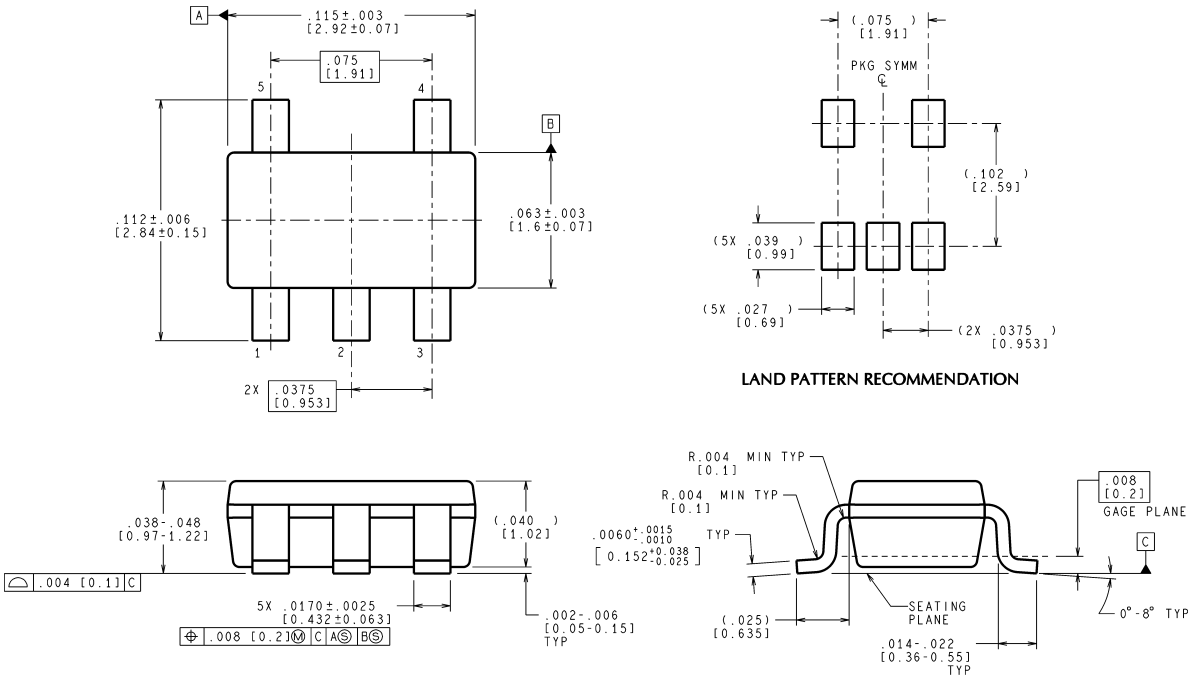

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION




BPA04XXX (Rev E)

**Micro SMD, 4 Bump Package (BPA04)**
**NS Package Number BPA04EJC**
**X1 = 0.879 ± 0.03mm**
**X2 = 0.980 ± 0.03mm**
**X3 = 0.900 ± 0.1mm**




CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MF05A (Rev B)

**5-Lead Small Outline Package (MF)**
**NS Package Number MF05A**

## Notes

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**BANNED SUBSTANCE COMPLIANCE**

National Semiconductor certifies that the products and packing materials meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no ''Banned Substances'' as defined in CSP-9-111S2.

**National Semiconductor**
**Americas Customer**
**Support Center**
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

**National Semiconductor**
**Europe Customer Support Center**
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor**
**Asia Pacific Customer**
**Support Center**
Email: ap.support@nsc.com

**National Semiconductor**
**Japan Customer Support Center**
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560