

POWER MANAGEMENT

Description

The SC4211 is a high performance positive voltage regulator designed for use in applications requiring very low Input voltage and very low dropout voltage at up to 1 amperes. It operates with a V_{in} as low as 1.4V, with output voltage programmable as low as 0.5V. The SC4211 features ultra low dropout, ideal for applications where V_{out} is very close to V_{in} . Additionally, the SC4211 has an enable pin to further reduce power dissipation while shutdown. The SC4211 provides excellent regulation over variations in line, load and temperature.

The SC4211 is available in the SOIC-8-EDP (Exposed Die Pad) package. Depending on how the FB pin is configured, the output voltage can be either externally adjusted or fixed to either 0.5V or 1V.

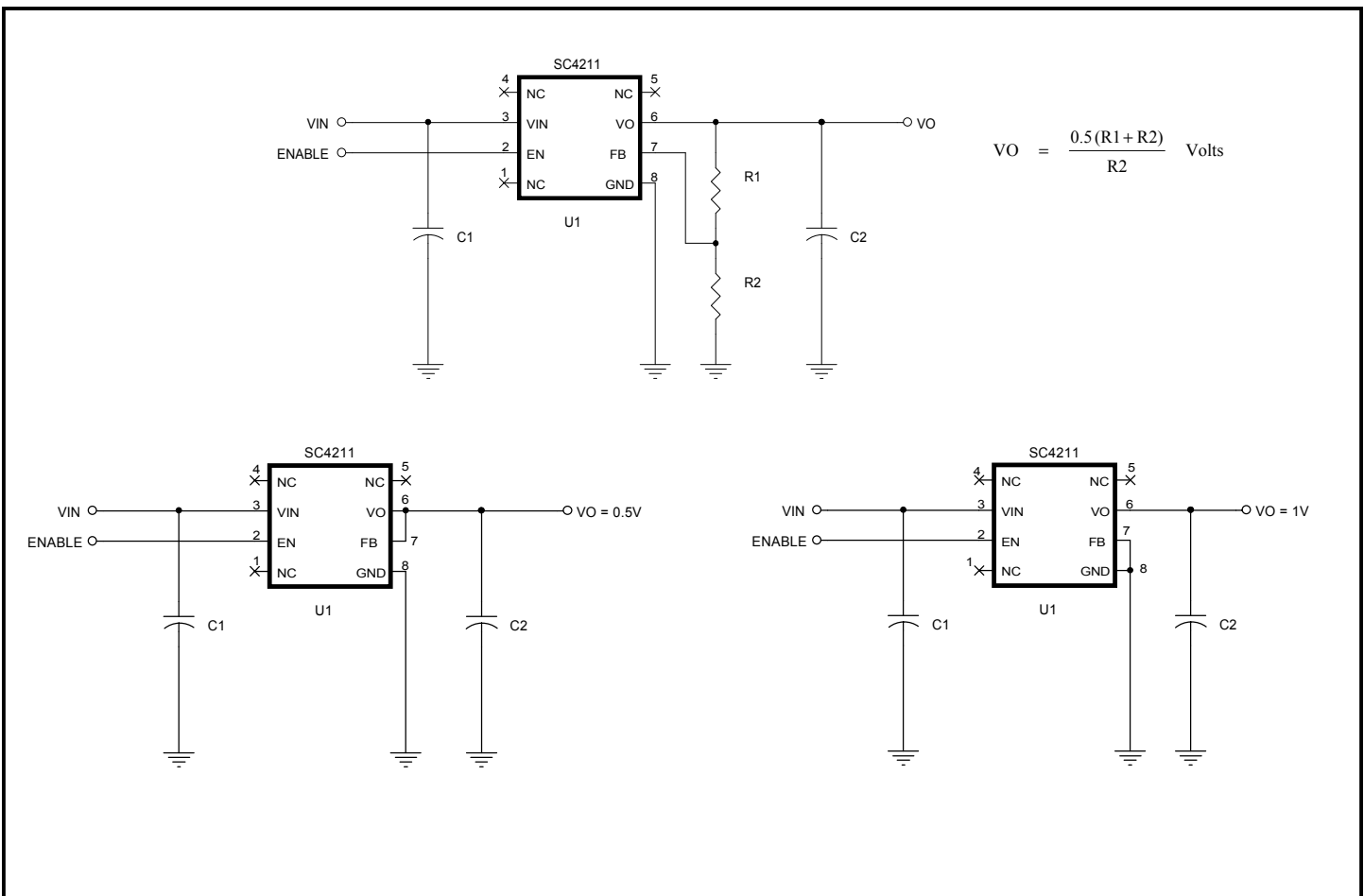
Features

- ◆ Input Voltage as low as 1.4V
- ◆ 400mV dropout @ 1A
- ◆ Adjustable output from 0.5V
- ◆ Over current and over temperature protection
- ◆ Enable pin
- ◆ 10 μ A quiescent current in shutdown
- ◆ Full industrial temperature range
- ◆ Available in SOIC-8-EDP Lead-free package, fully WEEE and RoHS compliant

Applications

- ◆ Telecom/Networking cards
- ◆ Motherboards/Peripheral cards
- ◆ Industrial Applications
- ◆ Wireless infrastructure
- ◆ Set top boxes
- ◆ Medical equipment
- ◆ Notebook computers
- ◆ Battery powered systems

Typical Application Circuits



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Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Max	Units
V _{in} , EN, V _o , FB to GND		7	V
Power Dissipation	P _D	Internally Limited	W
Thermal Resistance Junction to Ambient ⁽¹⁾	θ _{JA}	36	°C/W
Thermal Resistance Junction to Case ⁽¹⁾	θ _{JC}	5.5	°C/W
Operating Ambient Temperature Range	T _A	-40 to +85	°C
Operating Junction Temperature Range	T _J	-40 to +125	°C
Storage Temperature Range	T _{STG}	-65 to +150	°C
Peak IR Reflow Temperature (10s to 30s)	T _P	260	°C
ESD Rating (Human Body Model) ⁽²⁾	V _{ESD}	2	kV

Notes:

(1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards,

(2) Tested according to JEDEC standard JESD22-A114-B.

Electrical Characteristics

Unless specified: V_{EN} = V_{IN}, V_{FB} = V_O, V_{IN} = 1.40V to 6.0V, I_O = 10μA to 1A.
Values in **bold** apply over the full operating temperature range.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VIN						
Supply Voltage Range	V _{IN}		1.40		6.0	V
Quiescent Current	I _Q	V _{IN} = 3.3V, I _O = 0A			3	mA
		V _{IN} = 6.0V, V _{EN} = 0V		10	50	μA
VO						
Output Voltage ⁽¹⁾	V _O	V _{IN} = V _O + 0.5V, I _O = 10mA	-2%	V _O	+2%	V
(Fixed Voltage, V _{FB} = 0)		1.40V ≤ V _{IN} ≤ 6.0V, I _O = 10mA	-3%		+3%	
Line Regulation ⁽¹⁾	REG _(LINE)	I _O = 10mA		0.2	0.4	%/V
Load Regulation ⁽¹⁾	REG _(LOAD)	I _O = 10mA to 1A		0.5	1.5	%/V
Dropout Voltage ⁽¹⁾⁽²⁾	V _{DO}	I _O = 500mA		100	250	mV
					300	

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Electrical Characteristics (Cont.)

Unless specified: $V_{EN} = V_{IN}$, $V_{FB} = V_O$, $V_{IN} = 1.40V$ to $6.0V$, $I_O = 10\mu A$ to $1A$.
 Values in **bold** apply over the full operating temperature range.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VO (Cont.)						
Dropout Voltage ⁽¹⁾⁽²⁾	V_{DO}	$I_O = 1A$		200	400	mV
					500	
Minimum Load Current ⁽³⁾	I_O	$V_{IN} = V_O + 0.5V$			10	μA
Current Limit ⁽⁴⁾	I_{CL}		1.1	1.5	2.0	A
Feedback						
Reference Voltage ⁽¹⁾	V_{REF}	$V_{IN} = 3.3V$, $V_{FB} = V_{OUT}$, $I_O = 10mA$	0.495	0.5	0.505	V
		Full I_{OUT} , and V_{IN} Range	0.490		0.510	
Feedback Pin Current ⁽⁴⁾	I_{ADJ}	$V_{FB} = V_{REF}$		80	200	nA
Feedback Pin Threshold ⁽⁵⁾	$V_{TH(FB)}$		0.05	0.16	0.40	V
EN						
Enable Pin Current	I_{EN}	$V_{EN} = 0V$, $V_{IN} = 3.3V$		1.5	10	μA
Enable Pin Threshold	V_{IH}	$V_{IN} = 3.3V$	1.6			V
	V_{IL}	$V_{IN} = 3.3V$			0.4	
Over Temperature Protection						
High Trip level	T_{HI}			160		$^{\circ}C$
Hysteresis	T_{HYST}			10		$^{\circ}C$

Notes:

- (1) Low duty cycle pulse testing with Kelvin connections required.
- (2) $V_{DO} = V_{IN} - V_O$ when V_O decreases by 1.5% of its nominal output voltage with $V_{IN} = V_O + 0.8V$.
- (3) Required to maintain regulation. Voltage set resistors R1 and R2 are usually utilized to meet this requirement.
- (4) Guaranteed by design.
- (5) When V_{FB} exceeds this threshold, the "Sense Select" switch disconnects the internal feedback chain from the error amplifier and connects V_{FB} instead.

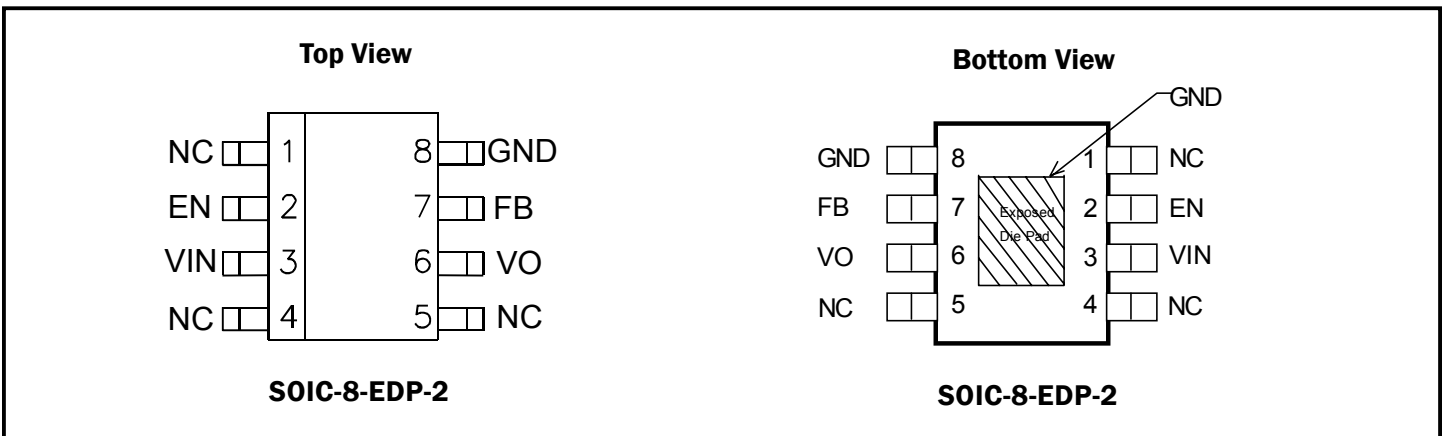
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Ordering Information

Part Number	Package	Temp. Range (T _j)
SC4211STRT ⁽¹⁾⁽²⁾	SOIC-8-EDP	-40 to +125 °C
SC4211EVB	Evaluation Board	

Notes:

(1) Only available in tape and reel packaging. A reel contains 2500 devices.

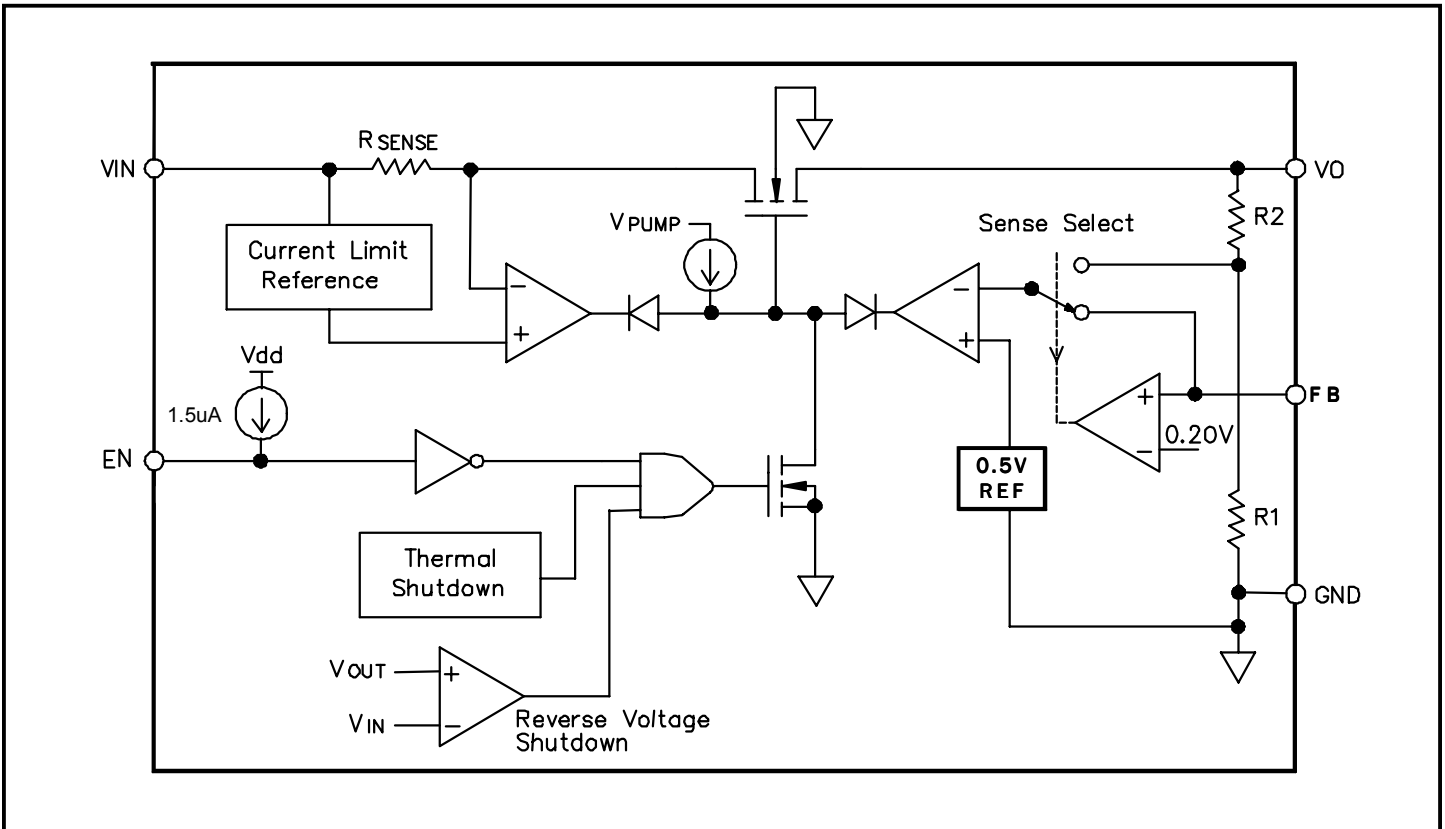
(2) Lead-free product. This product is fully WEEE and RoHS compliant.

Pin Configuration

Pin Descriptions

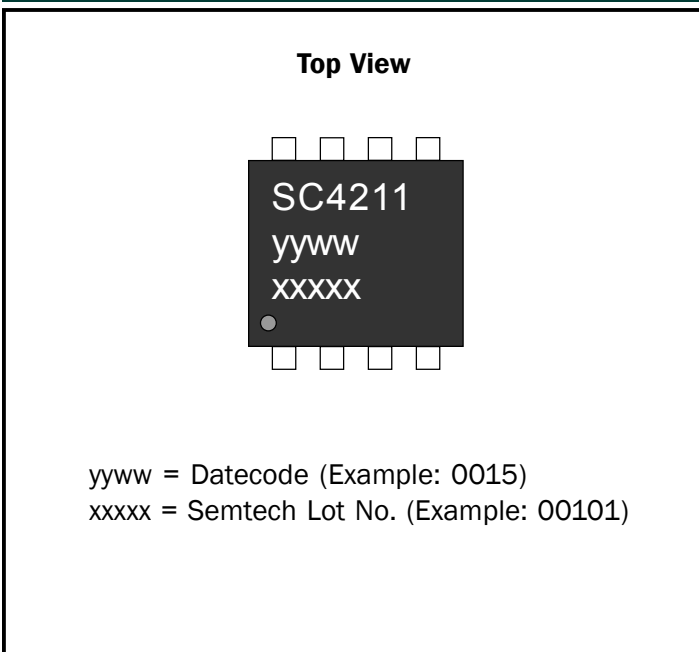
Pin #	Pin Name	Pin Description
2	EN	Enable Input. Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. The device will be enabled if this pin is left open. Connect to VIN if not being used.
3	VIN	Input voltage. For regulation at full load, the input to this pin must be between (VO+ 0.5V) and 5.5V. Minimum VIN = 1.4V. A large bulk capacitance should be placed closely to this pin to ensure that the input supply does not sag below 1.4V. Also a minimum of 4.7uF ceramic capacitor should be placed directly at this pin.
6	VO	The pin is the power output of the device. A minimum of 10uF capacitor should be placed directly at this pin.
7	FB	When this pin is grounded, an internal resistor divider sets the output voltage to 1.0V. If connected to the Vo pin, the output voltage will be set at 0.5V. If external feedback resistors are used, the output voltage will be (See Application Circuits on page 1): $VO = \frac{0.5(R1 + R2)}{R2} \text{ Volts}$
8	GND	Reference ground. The GND pin and the exposed die pad must be connected together at the IC pin.
1,4,5	NC	No Connection.
	THERMAL PAD	Pad for heatsinking purposes. Connect to ground plane using multiple vias. Not electrically connected internally.

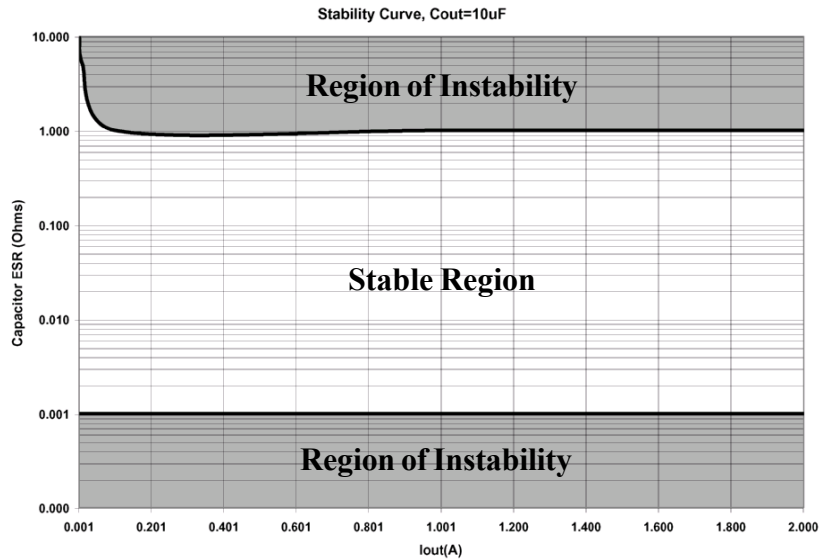
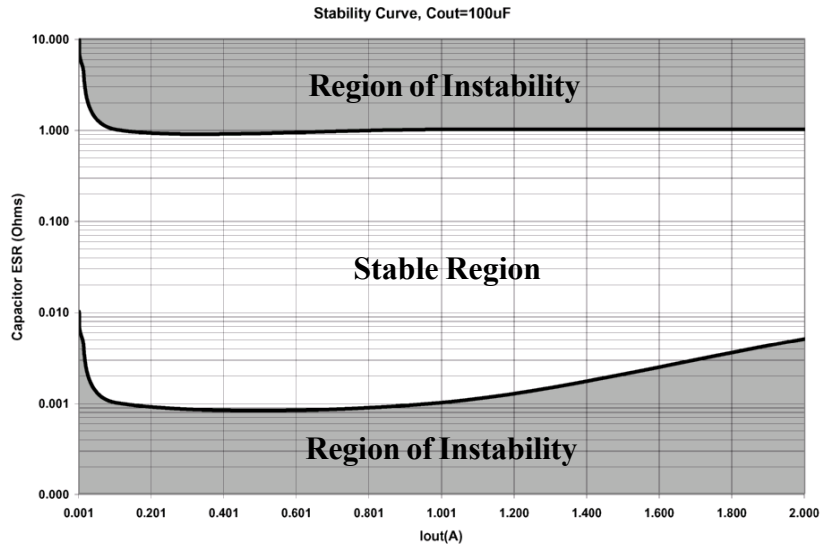
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Block Diagram



Marking Information





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Applications Information
Introduction

The SC4211 is intended for applications where high current capability and very low dropout voltage are required. It provides a very simple, low cost solution that uses very little PCB real estate. Additional features include an enable pin to allow for a very low power consumption standby mode, and a fully adjustable output.

Component Selection

Input capacitor: A large bulk capacitance of about $\geq 10\mu\text{F}/\text{A}$ (output load) should be closely placed to the input supply pin of the SC4211 to ensure that V_{IN} does not sag below 1.4V. Also a minimum of 4.7 μF ceramic capacitor is recommended to be placed directly next to the V_{IN} pin. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, input droop due to load transients is reduced, improving load transient response. Additional capacitance may be added if required by the application.

Output capacitor: A minimum bulk capacitance of $\geq 10\mu\text{F}/\text{A}$ (output load), along with a 0.1 μF ceramic decoupling capacitor is recommended. Increasing the bulk capacitance will improve the overall transient response. The use of multiple lower value ceramic capacitors in parallel to achieve the desired bulk capacitance will not cause stability issues. Although designed for use with ceramic output capacitors, the SC4211 is extremely tolerant of output capacitor ESR values and thus will also work comfortably with tantalum output capacitors.

Noise immunity: In very electrically noisy environments, it is recommended that 0.1 μF ceramic capacitors be placed from IN to GND and OUT to GND as close to the device pins as possible.

Internal voltage selection: By connecting the FB pin to GND, an internal resistor divider will regulate the output voltage to 1.0V. If the FB pin is connected directly to the VO pin, the output voltage will be regulated to the 0.5V internal reference.

External voltage selection resistors: The use of 1% resistors, and designing for a current flow $\geq 10\mu\text{A}$ is recommended to ensure a well regulated output (thus $R_2 \leq 50\text{k}\Omega$).

Enable: Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. A pull up resistor up to 400kOhms should be connected from this pin to the V_{IN} pin in application where supply voltages of $V_{\text{IN}} < 1.9\text{V}$ is required. For applications with higher voltages than 1.9V, EN pin could be left open or connected to V_{IN} .

Thermal Considerations

The power dissipation in the SC4211 is approximately equal to the product of the output current and the input to output voltage differential:

$$P_D \approx (V_{\text{IN}} - V_{\text{OUT}}) \cdot I_O$$

The absolute worst-case dissipation is given by:

$$P_{D(\text{MAX})} = (V_{\text{IN}(\text{MAX})} - V_{\text{OUT}(\text{MIN})}) \cdot I_{O(\text{MAX})} + V_{\text{IN}(\text{MAX})} \cdot I_{Q(\text{MAX})}$$

For a typical scenario, $V_{\text{IN}} = 3.3\text{V} \pm 5\%$, $V_{\text{OUT}} = 2.8\text{V}$ and $I_O = 1\text{A}$, therefore:

$$V_{\text{IN}(\text{MAX})} = 3.465\text{V}, V_{\text{OUT}(\text{MIN})} = 2.744\text{V} \text{ and } I_{Q(\text{MAX})} = 1.75\text{mA},$$

$$\text{Thus } P_{D(\text{MAX})} = .722\text{W}.$$

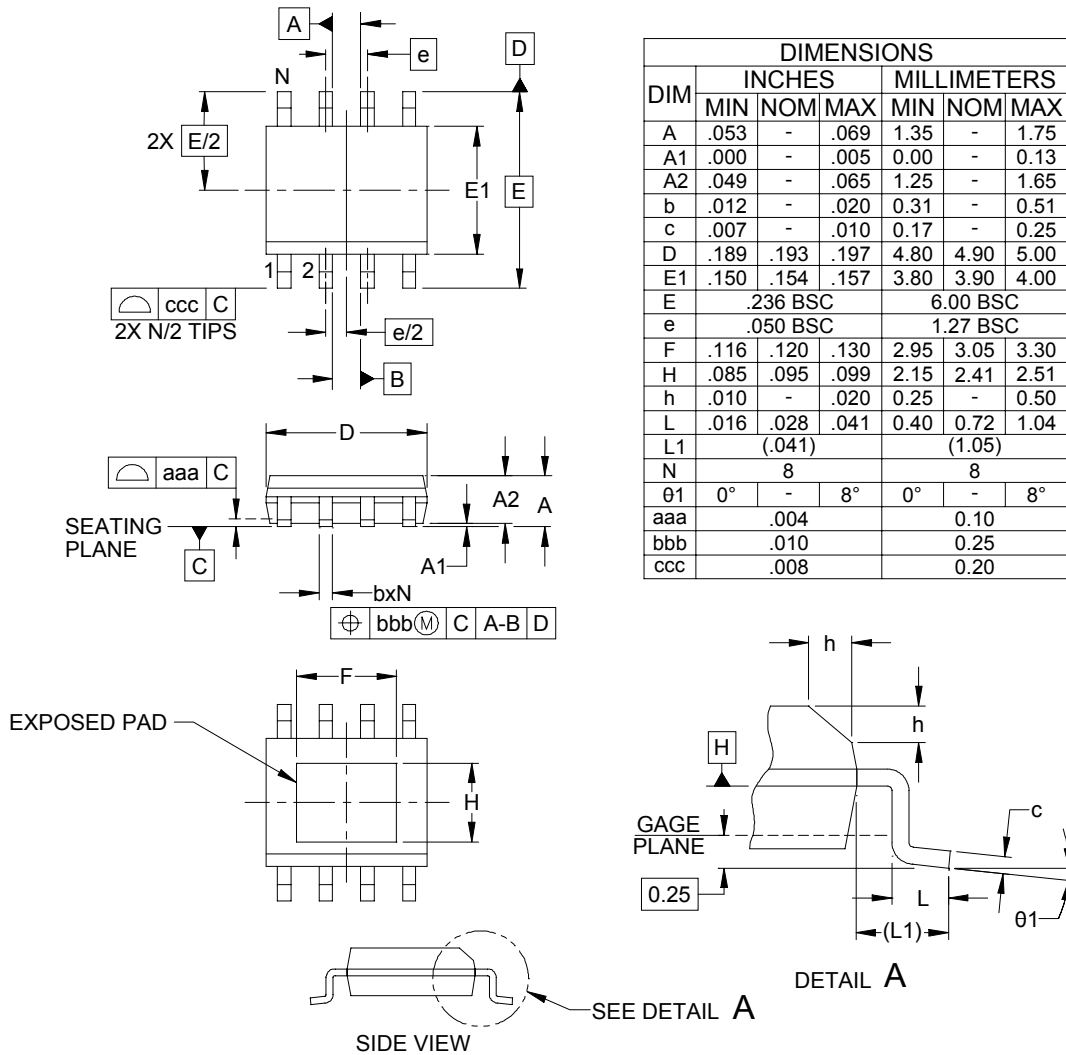
Using this figure, and assuming $T_{A(\text{MAX})} = 70^\circ\text{C}$, we can calculate the maximum thermal impedance allowable to maintain $T_J \leq 150^\circ\text{C}$:

$$R_{\text{TH}(J-A)(\text{MAX})} = \frac{(T_{J(\text{MAX})} - T_{A(\text{MAX})})}{P_{D(\text{MAX})}} = \frac{(150 - 70)}{.722} = 110^\circ\text{C}/\text{W}$$

This should be achievable for the SOIC-8-EDP package using PCB copper area to aid in conducting the heat away, such as one square inch of copper connected to the ground pins of the device. Internal ground/power planes and air flow will also assist in removing heat. For higher ambient temperatures it may be necessary to use additional copper area.

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Outline Drawing - SOIC-8-EDP

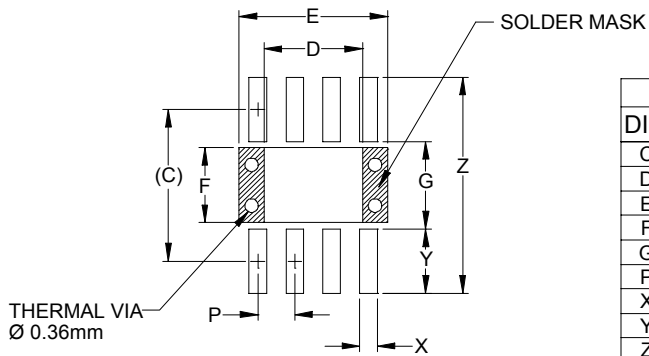


NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION BA.

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Land Pattern - SOIC-8-EDP



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
D	.134	3.40
E	.201	5.10
F	.101	2.56
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Contact Information

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