Adjustable Output Ultralow I_Q, 200 mA, SOT-23, anyCAP® Low Dropout Regulator

ADP3331

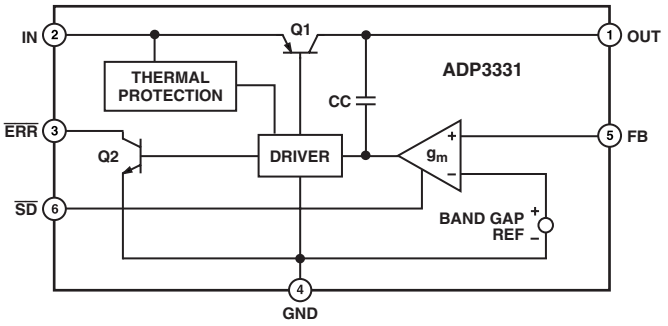
FEATURES

- High Accuracy over Line and Load: ±0.7% @ 25°C, 1.4% over Temperature
- Ultralow Dropout Voltage: 140 mV (Typ) @ 200 mA
- Can Be Used as a High Current (>1 A) LDO Controller
- Requires Only C_O = 0.47 μF for Stability
- anyCAP = Stable with Any Type of Capacitor (Including MLCC)
- Current and Thermal Limiting
- Low Noise
- Low Shutdown Current: 10 nA Typical
- 2.6 V to 12 V Supply Range
- 1.5 V to 11.75 V Output Range
- –40°C to +85°C Ambient Temperature Range
- Ultrasmall Thermally Enhanced Chip-on-Lead™ SOT-23-6 Lead Package

APPLICATIONS

- Cellular Telephones
- Notebook, Palmtop Computers
- Battery-Powered Systems
- PCMCIA Regulators
- Bar Code Scanners
- Camcorders, Cameras

FUNCTIONAL BLOCK DIAGRAM



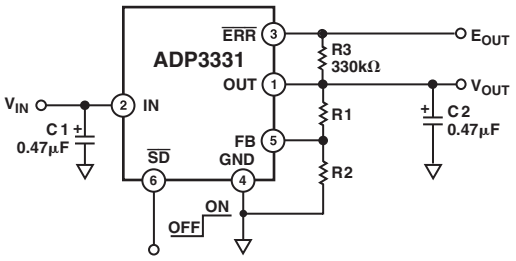


Figure 1. Typical Application Circuit

GENERAL DESCRIPTION

The ADP3331 is a member of the ADP330x family of precision low dropout anyCAP voltage regulators. The ADP3331 operates with an input voltage range of 2.6 V to 12 V and delivers a load current up to 200 mA. The ADP3331 stands out from the conventional LDOs with a novel architecture and an enhanced process that enables it to offer performance advantages and higher output current than its competition. Its patented design requires only a 0.47 μF output capacitor for stability. This device is insensitive to capacitor equivalent series resistance (ESR), and is stable with any good quality capacitor, including ceramic (MLCC) types for space restricted applications. The ADP3331 achieves exceptional accuracy of ±0.7% at room temperature and ±1.4% overall accuracy over temperature, line, and load variations. The dropout voltage of the ADP3331 is only 140 mV (typical) at 200 mA. This device also includes a safety current limit, thermal overload protection, and a shutdown feature. In shutdown mode, the ground current is reduced to less than 2 μA. The ADP3331 has ultralow quiescent current 34 μA (typical) in light load situations. The SOT-23-6 package has been thermally enhanced using Analog Device's proprietary Chip-on-Lead feature to maximize power dissipation.

REV. A

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ADP3331–SPECIFICATIONS (T_A = –40°C to +85°C, V_{IN} = 7 V, C_{IN} = 0.47 µF, C_{OUT} = 0.47 µF, unless otherwise noted.)[1, 2]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE ACCURACY[3] HIGH OUTPUT VOLTAGE RANGE		V_{IN} = V_{OUTNOM} + 0.25 V to 12 V, V_{OUTNOM} ≥ 2.35 V, I_L = 0.1 mA to 200 mA, T_A = 25°C	–0.7		+0.7	%
		V_{IN} = V_{OUTNOM} + 0.25 V to 12 V, V_{OUTNOM} ≥ 2.35 V, I_L = 0.1 mA to 150 mA, T_A = –40°C to +85°C	–1.4		+1.4	%
		V_{IN} = V_{OUTNOM} + 0.25 V to 12 V, V_{OUTNOM} ≥ 2.35 V, I_L = 0.1 mA to 200 mA, T_A = –20°C to +85°C	–1.4		+1.4	%
OUTPUT VOLTAGE ACCURACY[3] LOW OUTPUT VOLTAGE RANGE		V_{IN} = 2.6 V to 12 V, V_{OUTNOM} = 1.5 V to 2.35 V, I_L = 0.1 mA to 200 mA, T_A = 25°C	–0.7		+0.7	%
		V_{IN} = 2.6 V to 12 V, V_{OUTNOM} = 1.5 V to 2.35 V, I_L = 0.1 mA to 150 mA, T_A = –40°C to +85°C	–1.4		+1.4	%
		V_{IN} = 2.6 V to 12 V, V_{OUTNOM} = 1.5 V to 2.35 V, I_L = 0.1 mA to 200 mA, T_A = –20°C to +85°C	–1.4		+1.4	%
LINE REGULATION	$\frac{\Delta V_O}{\Delta V_{IN}}$	V_{IN} = V_{OUTNOM} + 0.25 V to 12 V T_A = 25°C		0.06		mV/V
LOAD REGULATION	$\frac{\Delta V_O}{\Delta I_L}$	I_L= 0.1 mA to 200 mA T_A = 25°C		0.04		mV/mA
GROUND CURRENT	I_{GND}	I_L = 200 mA, T_A = –20°C to +85°C I_L = 150 mA I_L = 50 mA I_L = 0.1 mA		1.6 1.2 0.4 34	4.0 3.1 1.1 50	mA mA mA µA
GROUND CURRENT IN DROPOUT	I_{GND}	V_{IN} = V_{OUTNOM} – 100 mV I_L = 0.1 mA		37	55	µA
DROPOUT VOLTAGE[2]	V_{DROP}	V_{OUT} = 98% of V_{OUTNOM} I_L = 200 mA, T_A = –20°C to +85°C I_L = 150 mA I_L = 10 mA I_L = 1 mA		0.14 0.11 0.042 0.025	0.23 0.17 0.06 0.05	V V V V
PEAK LOAD CURRENT	I_{LDPK}	V_{IN} = V_{OUTNOM} + 1 V		300		mA
OUTPUT NOISE	V_{NOISE}	f = 10 Hz–100 kHz, C_L = 10 µF I_L = 200 mA, C_{NR} = 10 nF, V_{OUT} = 3 V f = 10 Hz–100 kHz, C_L = 10 µF I_L = 200 mA, C_{NR} = 0 nF, V_{OUT} = 3 V		47 95		µV rms µV rms
SHUTDOWN THRESHOLD	$V_{TH\overline{SD}}$	ON OFF	2.0		0.4	V V
SHUTDOWN PIN INPUT CURRENT	$I_{\overline{SD}}$	0 < $\overline{SD}$ ≤ 12 V 0 < $\overline{SD}$ ≤ 5 V		1.9 1.4	9 6	µA µA
GROUND CURRENT IN SHUTDOWN MODE	$I_{GND\overline{SD}}$	$\overline{SD}$ = 0 V, V_{IN} = 12 V		0.01	2	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT CURRENT IN SHUTDOWN MODE	$I_{O\overline{SD}}$	T_A = 25°C @ V_{IN} = 12 V T_A = 85°C @ V_{IN} = 12 V			1 2	µA µA
ERROR PIN OUTPUT LEAKAGE	I_{EL}	V_{EO} = 5 V			1	µA
ERROR PIN OUTPUT LOW VOLTAGE	V_{EOL}	I_{SINK} = 400 µA		0.19	0.40	V

NOTES
[1]Ambient temperature of 85°C corresponds to a junction temperature of 125°C under typical full load test conditions.
[2]Application stable with no load.
[3]Assumes the use of ideal resistors. Overall accuracy also depends on the tolerance of the external resistors used to set the output voltage.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

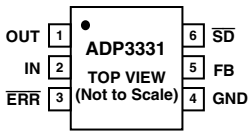
Input Supply Voltage . . . . . –0.3 V to +16 V
Shutdown Input Voltage . . . . . –0.3 V to +16 V
Power Dissipation . . . . . Internally Limited
Operating Ambient Temperature Range . . . . –40°C to +85°C
Operating Junction Temperature Range . . . –40°C to +125°C
θ_{JA} (4-Layer Board) . . . . . 165°C/W
θ_{JA} (2-Layer Board) . . . . . 190°C/W
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Output Voltage	Package Option	Branding
ADP3331ART	ADJ	RT-6 (SOT-23-6)	L9B

PIN CONFIGURATION



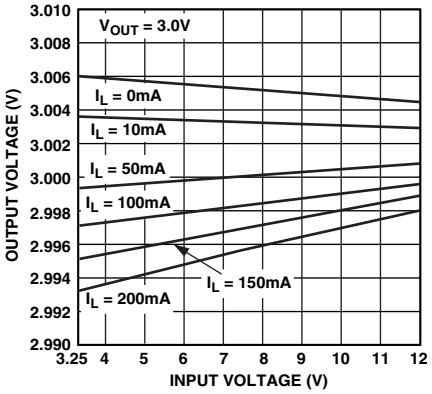
PIN FUNCTION DESCRIPTIONS

Pin	Name	Function
1	OUT	Output of the Regulator. Bypass to ground with a 0.47 µF or larger capacitor.
2	IN	Regulator Input.
3	$\overline{ERR}$	Open Collector Output that goes low to indicate that the output is about to go out of regulation.
4	GND	Ground.
5	FB	Feedback Input. Connect to an external resistor divider, which sets the output voltage.
6	$\overline{SD}$	Active Low Shutdown Pin. Connect to ground to disable the regulator output. When shutdown is not used, this pin should be connected to the input pin.

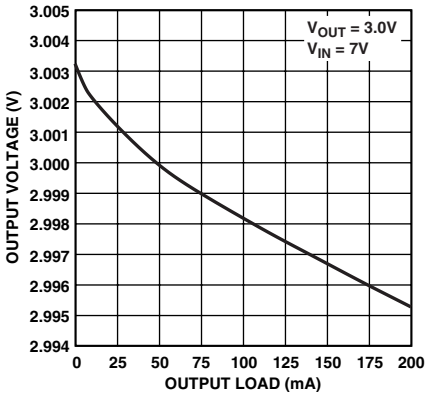
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3331 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

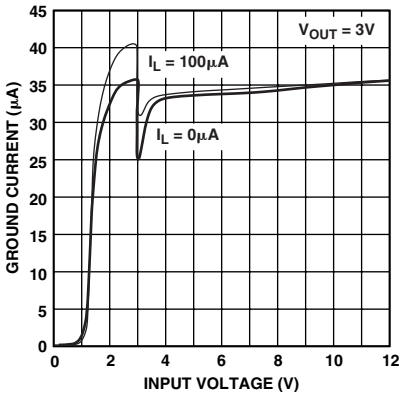
ADP3331–Typical Performance Characteristics



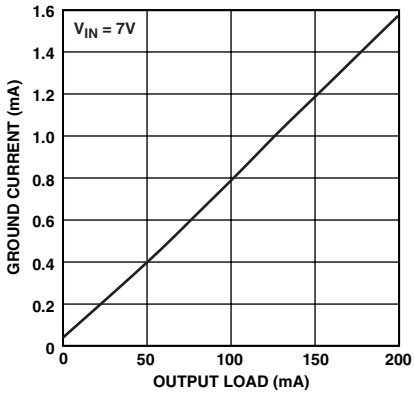
TPC 1. Line Regulation Output Voltage vs. Supply Voltage



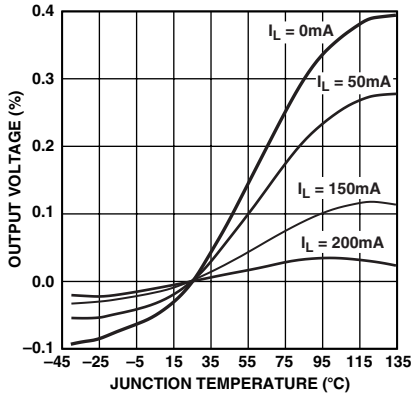
TPC 2. Output Voltage vs. Load Current



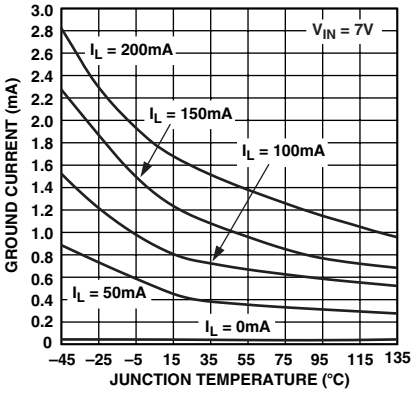
TPC 3. Ground Current vs. Supply Voltage



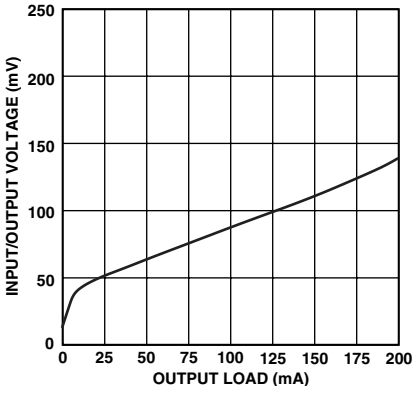
TPC 4. Ground Current vs. Load Current



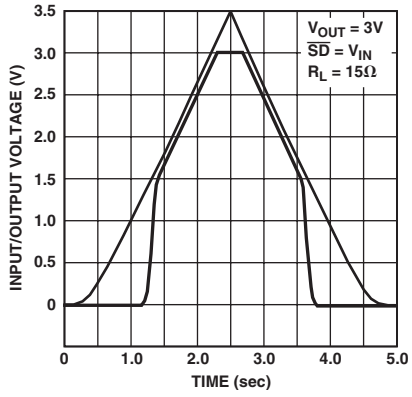
TPC 5. Output Voltage Variation % vs. Junction Temperature



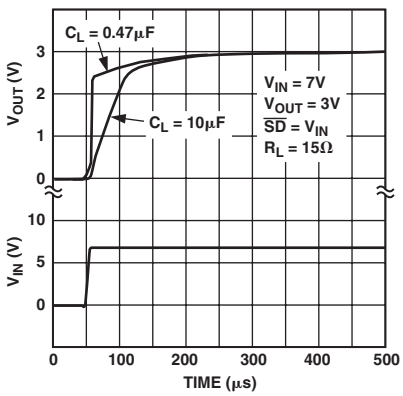
TPC 6. Ground Current vs. Junction Temperature



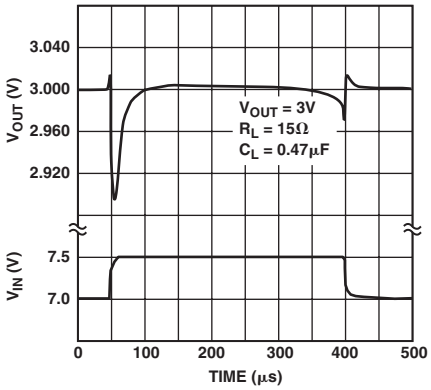
TPC 7. Dropout Voltage vs. Output Current



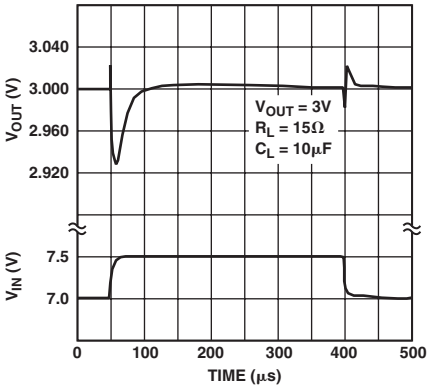
TPC 8. Power-Up/Power-Down



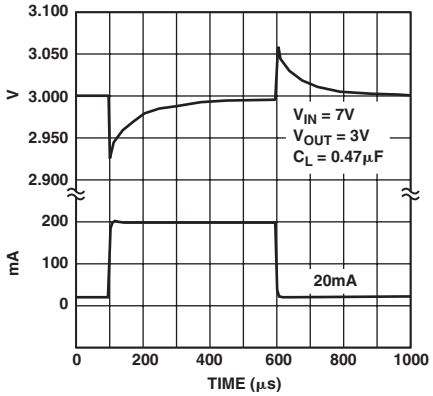
TPC 9. Power-Up Response



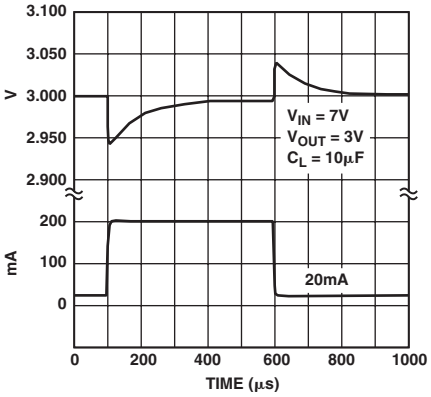
TPC 10. Line Transient Response



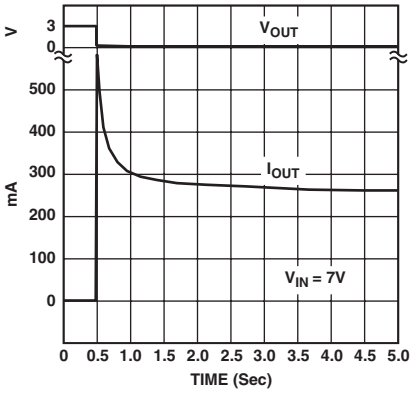
TPC 11. Line Transient Response



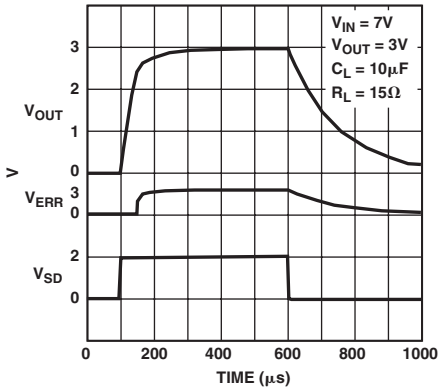
TPC 12. Load Transient Response



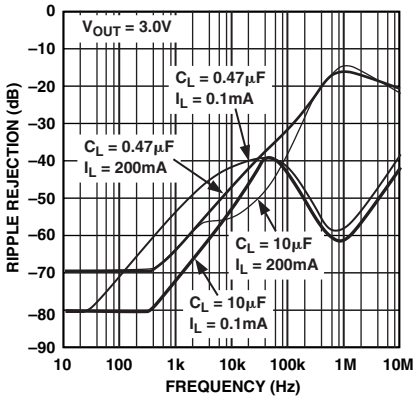
TPC 13. Load Transient Response



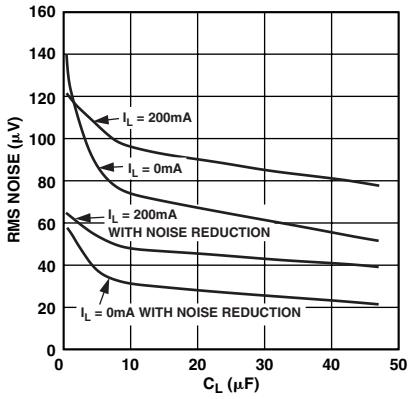
TPC 14. Short Circuit Current



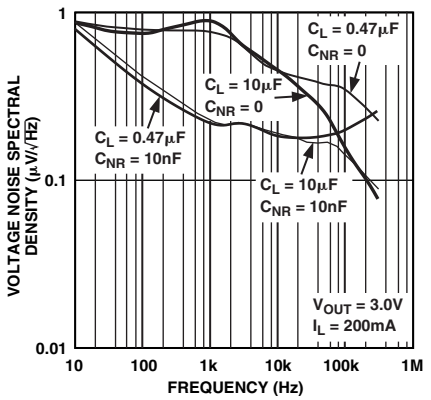
TPC 15. Turn On–Turn Off Response



TPC 16. Power Supply Ripple Rejection



TPC 17. RMS Noise vs. C_L (10 Hz to 100 kHz)



TPC 18. Output Noise Density

THEORY OF OPERATION

The ADP3331 anyCAP LDO uses a single control loop for both regulation and reference functions, as shown in Figure 2. The output voltage is sensed by an external resistive voltage divider consisting of R1 and R2. Feedback is taken from this network by way of a series diode (D1) and a second resistor divider (R3 and R4) to the input of an amplifier.

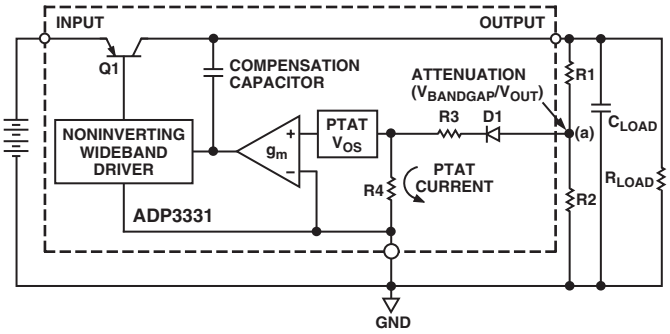


Figure 2. Functional Block Diagram

A very high gain error amplifier is used to control this loop. The amplifier is constructed in such a way that at equilibrium it produces a large, temperature-proportional input offset voltage that is repeatable and very well controlled. The temperature-proportional offset voltage is combined with the complementary diode voltage to form a virtual band gap voltage, implicit in the network, although it never appears explicitly in the circuit. Ultimately, this patented design makes it possible to control the loop with only one amplifier. This technique also improves the noise characteristics of the amplifier by providing more flexibility on the trade-off of noise sources, which leads to a low noise design.

The R1, R2 divider is chosen in the same ratio as the band gap voltage to output voltage. Although the R1, R2 resistor divider is loaded by the diode D1 and a second divider consisting of R3 and R4, the values are chosen to produce a temperature stable output. This unique arrangement specifically corrects for the loading of the divider so that the error resulting from the base current loading in conventional circuits is avoided.

The patented amplifier controls a new and unique noninverting driver that drives the pass transistor, Q1. The use of this special noninverting driver enables the frequency compensation to include the load capacitor in a pole-splitting arrangement to achieve reduced sensitivity to the value, type, and ESR of the load capacitor.

Most LDOs place strict requirements on the range of ESR values for the output capacitor because they are difficult to stabilize due to the uncertainty of the load capacitance and resistance. Moreover, the ESR value required to keep conventional LDOs stable changes, depending on load and temperature. These ESR limitations make designing with LDOs more difficult because of their unclear specifications and extreme variations over temperature.

The ADP3331 solves this problem. It can be used with any good quality capacitor, with no constraint on the minimum ESR. The innovative design allows the circuit to be stable with just a small 0.47 µF capacitor on the output. Additional advantages of the pole-splitting scheme include superior line noise rejection and very high regulator gain. The high gain leads to excellent regulation, and ±1.4% accuracy is guaranteed over line, load, and temperature.

Additional features of the circuit include current limit, thermal shutdown, and an error flag. Compared to standard solutions that give a warning after the output has lost regulation, the ADP3331 provides improved system performance by enabling the $\overline{\text{ERR}}$ pin to give a warning just before the device loses regulation.

As the chip's temperature rises above +165°C, the circuit activates a soft thermal shutdown to reduce the current to a safe level. The thermal shutdown condition is indicated by the $\overline{\text{ERR}}$ signal going low.

APPLICATION INFORMATION

Capacitor Selection

Output Capacitor: The stability and transient response of the LDO is a function of the output capacitor. The ADP3331 is stable with a wide range of capacitor values, types, and ESR (anyCAP). A capacitor as low as 0.47 µF is all that is needed for stability; larger capacitors can be used if high current surges on the output are anticipated. The ADP3331 is stable with extremely low ESR capacitors (ESR ≈ 0), such as multilayer ceramic capacitors (MLCC) or OSCON. Note that the effective capacitance of some capacitor types falls below the minimum over temperature or with dc voltage.

Input Capacitor: An input bypass capacitor is not strictly required but is recommended in any application involving long input wires or high source impedance. Connecting a 0.47 µF capacitor from the input to ground reduces the circuit's sensitivity to PC board layout and input transients. If a larger output capacitor is necessary, a larger value input capacitor is also recommended.

Noise Reduction Capacitor: A noise reduction capacitor can be used to reduce the output noise by 6 dB to 10 dB. This capacitor limits the noise gain when connected between the feedback pin (FB) and the output pin (OUT), as shown in Figure 3. Low leakage capacitors in the 10 pF to 500 pF range provide the best performance. Since FB is internally connected to a high impedance node, any connection to this node should be carefully done to avoid noise pickup from external sources. The pad connected to this pin should be as small as possible; long PC board traces are not recommended. When adding a noise reduction capacitor, use the following guidelines:

- Maintain a minimum load current of 1 mA when not in shutdown.
- For CNR values greater than 500 pF, add a 100 kΩ series resistor (RNR).

It is important to note that as CNR increases, the turn-on time will be delayed. With CNR values greater than 1 nF, this delay may be on the order of several milliseconds.

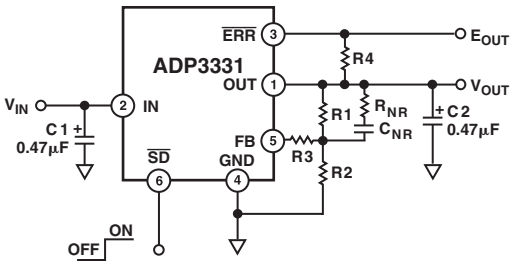


Figure 3. Noise Reduction Circuit

Output Voltage

The ADP3331 has an adjustable output voltage that can be set by an external resistor divider. The output voltage will be divided by R1 and R2, and then fed back to the FB pin. Refer to Figure 3.

For the output voltage to have the lowest possible sensitivity to temperature variations, it is important that the parallel resistance of R1 and R2 be as close as possible to 230 kΩ:

$$\frac{R1 \times R2}{R1 + R2} = 230\ k\Omega \tag{1}$$

Also, for the best accuracy over temperature, the feedback voltage should set for 1.204 V:

$$V_{OUT}\left(\frac{R2}{R1 + R2}\right) = V_{FB} \tag{2}$$

Where V_{OUT} is the desired output voltage and V_{FB} is the virtual band gap voltage. Note that V_{FB} does not actually appear at the FB pin due to loading by the internal PTAT current.

Combining the above equations and solving for $R1$ and $R2$ results in the following formulas:

$$R1 = 230\left(\frac{V_{OUT}}{V_{FB}}\right) k\Omega \tag{3}$$

$$R2 = \frac{230}{\left(1 - \frac{V_{FB}}{V_{OUT}}\right)} k\Omega \tag{4}$$

The output voltage can be adjusted to any voltage from 1.5 V to 11.75 V. For example, Table I shows some representative feedback resistor values for output voltages in the specified range.

Table I. Feedback Resistor Selection

V_{OUT} (V)	R1 (1%)	R2 (1%)	R3 (1%)
1.5	243 kΩ	1.00 MΩ	34.8 kΩ
1.8	340 kΩ	698 kΩ	
2.2	422 kΩ	511 kΩ	
2.7	511 kΩ	412 kΩ	
3.3	634 kΩ	365 kΩ	
5	953 kΩ	301 kΩ	
9	1.00 MΩ	154 kΩ	97.6 kΩ

Note that at output voltages above 5.2 V and below 1.6 V, nonstandard resistor values or the addition of a resistor to the divider network is required to achieve the best performance. For output voltages below 1.6 V, select a standard resistance value for $R2$ and then calculate the value of $R1$:

$$R1 = \left(\frac{V_{OUT}}{V_{FB}} - 1\right) \times R2 \tag{5}$$

For output voltages above 5.2 V, select a standard resistance for R1, and calculate the value of $R2$:

$$R2 = R1 \times \left(\frac{V_{FB}}{V_{OUT} - V_{FB}}\right) \tag{6}$$

After selecting values for $R1$ and $R2$, calculate the value of $R3$ needed to maintain the 230 $k\Omega$ impedance:

$$R3 = 230\ k\Omega - \left(\frac{R1 \times R2}{R1 + R2}\right) \tag{7}$$

Using standard values, as shown in Table I, will sacrifice some output voltage accuracy.

Output Current Limit

The ADP3331 is short-circuit protected by limiting the pass transistor's base drive current. The maximum output current is limited to about 300 mA.

Thermal Overload Protection

The ADP3331 is protected by its thermal overload protection circuit against damage due to excessive power dissipation. Thermal protection limits the die temperature to a maximum of 165°C. Under extreme conditions (i.e., high ambient temperature and power dissipation) where the die temperature starts to rise above 165°C, the output current will be reduced until the die temperature has dropped to a safe level.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For normal operation, the device's power dissipation should be externally limited so that the junction temperature will not exceed 125°C.

Chip-on-Lead

The ADP3331 uses a patented Chip-on-Lead package design to ensure the best thermal performance in a SOT-23 footprint. In a standard SOT-23, most of the heat flows out of the ground pin. The Chip-on-Lead package uses an electrically isolated die attach, which allows all the pins to contribute to heat conduction. This technique reduces the thermal resistance to 190°C/W on a 2-layer board compared to >230°C/W for a standard SOT-23 lead frame. Figure 4 shows the difference between the standard SOT-23 and the Chip-on-Lead lead frames.

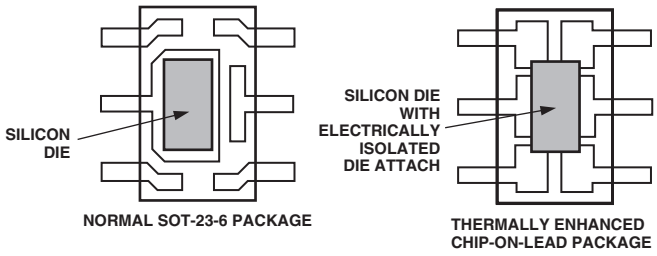


Figure 4. Chip-on-Lead Package

Calculating Junction Temperature
Device power dissipation is calculated as follows:

$$P_D = (V_{IN} - V_{OUT})I_{LOAD} + (V_{IN})I_{GND} \quad (8)$$

Where I_{LOAD} and I_{GND} are load current and ground current and V_{IN} and V_{OUT} are the input and output voltages, respectively.

Assuming that the worst case operating conditions are I_{LOAD} = 200 mA, I_{GND} = 4 mA, V_{IN} = 4.2 V, and V_{OUT} = 3.0 V, the device power dissipation is

$$P_D = (4.2\,V - 3.0\,V)\,200\,mA + (4.2\,V)\,4\,mA = 257\,mW \quad (9)$$

The proprietary package used on the ADP3331 has a thermal resistance of 165°C/W when placed on a 4-layer board and 190°C/W when placed on a 2-layer board. This allows the ambient temperature to be significantly higher for a given power dissipation than with a standard package. Assuming a 4-layer board, the junction temperature rise above ambient will be approximately equal to

$$\Delta T_{JA} = 0.257\,W \times 165^{\circ}C/W = 42.4^{\circ}C \quad (10)$$

To limit the junction temperature to 125°C, the maximum allowable ambient temperature is

$$T_{A(MAX)} = +125^{\circ}C - 42.4^{\circ}C = 82.6^{\circ}C \quad (11)$$

Shutdown Mode
Applying a TTL level high signal to the shutdown ($\overline{SD}$) pin, or tying it to the input pin, will turn the output ON. Pulling the $\overline{SD}$ to 0.4 V or below, or tying it to ground, will turn the output OFF. In shutdown mode, the quiescent current is reduced to less than 1 μA.

Error Flag Dropout Detector
The ADP3331 will maintain its output voltage over a wide range of load, input voltage, and temperature conditions. If the output is about to lose regulation due to the input voltage approaching the dropout level, the error flag will be activated. The $\overline{ERR}$ output is an open collector, which will be driven low.

Once set, the $\overline{ERR}$ flag's hysteresis will keep the output low until a small margin of operating range is restored either by raising the supply voltage or reducing the load.

Low Voltage Applications
In applications where the output voltage is 2.2 V or less, the ADP3331 may begin to exhibit some turn-on overshoot. The degree of overshoot is determined by several factors: the output voltage setting, the output load, the noise reduction capacitor, and the output capacitor.

The output voltage setting is determined by the application and cannot be tailored for minimum overshoot. In general, for output voltages of 2.2 V or less, the overshoot becomes larger as the output voltage decreases.

The output load is also determined by the system requirements. However, if the ADP3331 has no load on the output during startup, a small amount of preload can be added to minimize overshoot. A preload of 2 μA to 20 μA is recommended.

A noise reduction capacitor, if not already being used, is suggested to reduce the overshoot. Values in the range of 10 pF to 100 pF work best, along with the preload suggested previously.

The output capacitor can be adjusted to minimize the overshoot. Values in the 0.47 μF to 1.0 μF range should be used in conjunction with the preload and noise reduction capacitor. Further increases in the output capacitance may be acceptable if the output already has a sizable load during startup.

Higher Output Current
The ADP3331 can source up to 200 mA without any heat sink or pass transistor. If higher current is needed, an appropriate pass transistor can be used, as in Figure 5, to increase the output current to 1 A.

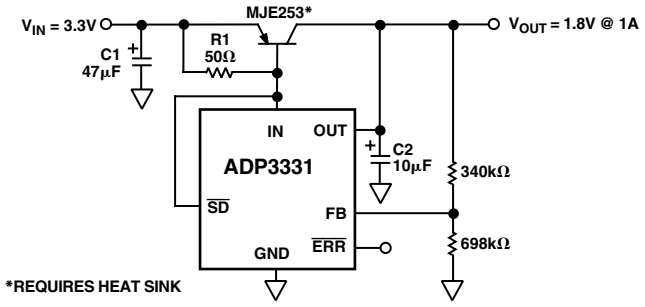


Figure 5. High Output Current Linear Regulator

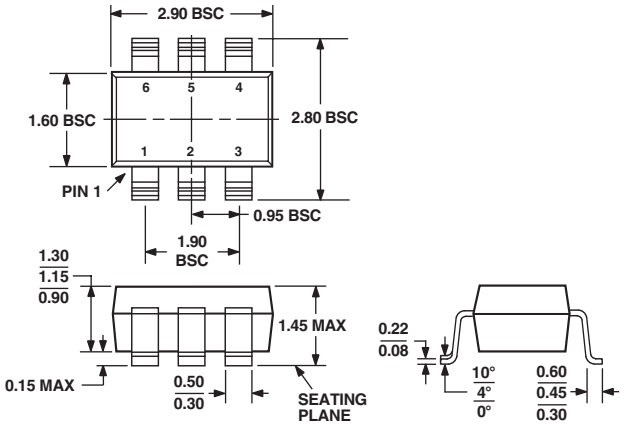
Printed Circuit Board Layout Considerations
Use the following general guidelines when designing printed circuit boards:

1. PC board traces with larger cross sectional areas will remove more heat from the ADP3331. For optimum heat transfer, specify thick copper and use wide traces.
2. The thermal resistance can be decreased by approximately 10% by adding a few square centimeters of copper area to the lands connected to the pins of the LDO.
3. The feedback pin is a high impedance input, and care should be taken when making a connection to this pin. The voltage setting resistors and noise reduction network must be located as close as possible. Long PC board traces are not recommended. Avoid routing traces near possible noise sources.

OUTLINE DIMENSIONS

6-Lead Small Outline Transistor Package [SOT-23]
(RT-6)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178AB

Revision History

Location	Page
5/03—Data Sheet changed from REV. 0 to REV. A.	
Renumbered figures and TPCs	Universal
Changes to FEATURES	1
Changes to Figure 3	7
Changes to Output Voltage section	7
Changes to Table I	7
Updated Outline Dimensions	9