ANALOG DEVICES

Ultralow Noise, 200 mA, CMOS Linear Regulator

ADP151

FEATURES

Ultralow noise: 9 μV rms
No noise bypass capacitor required
Stable with 1 μF ceramic input and output capacitors
Maximum output current: 200 mA
Input voltage range: 2.2 V to 5.5 V
Low quiescent current
  I_{GND} = 10 μA with 0 load
  I_{GND} = 265 μA with 200 mA load
Low shutdown current: <1 μA
Low dropout voltage: 140 mV at 200 mA load
Initial accuracy: ±1%
Accuracy over line, load, and temperature: ±2.5%
16 fixed output voltage options: 1.1 V to 3.3 V
PSRR performance of 70 dB at 10 kHz
Current-limit and thermal overload protection
Logic controlled enable
Internal pull-down resistor on EN input
5-lead TSOT package
6-lead LFCSP package
4-ball, 0.4 mm pitch WLCSP

APPLICATIONS

RF, VCO, and PLL power supplies
Mobile phones
Digital camera and audio devices
Portable and battery-powered equipment
Post dc-to-dc regulation
Portable medical devices

TYPICAL APPLICATION CIRCUIT

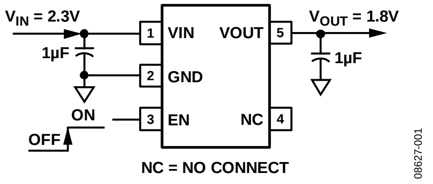

Figure 1. TSOT ADP151 with Fixed Output Voltage, 1.8 V

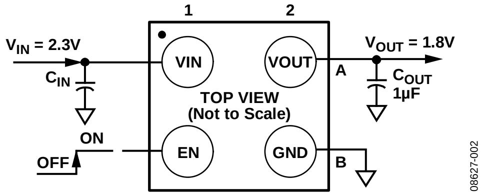

Figure 2. WLCSP ADP151 with Fixed Output Voltage, 1.8 V

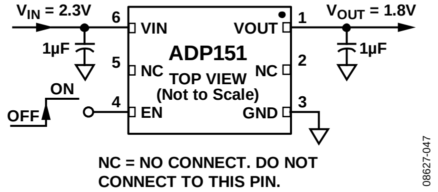

Figure 3. LFCSP ADP151 with Fixed Output Voltage, 1.8 V

GENERAL DESCRIPTION

The ADP151 is an ultralow noise, low dropout linear regulator that operates from 2.2 V to 5.5 V and provides up to 200 mA of output current. The low 140 mV dropout voltage at 200 mA load improves efficiency and allows operation over a wide input voltage range.

Using an innovative circuit topology, the ADP151 achieves ultralow noise performance without the necessity of a bypass capacitor, making it ideal for noise-sensitive analog and RF applications. The ADP151 also achieves ultralow noise performance without compromising PSRR or transient line and load performance. The low 265 μA of quiescent current at 200 mA load makes the ADP151 suitable for battery-operated portable equipment.

The ADP151 also includes an internal pull-down resistor on the EN input.

The ADP151 is specifically designed for stable operation with tiny 1 μF, ±30% ceramic input and output capacitors to meet the requirements of high performance, space constrained applications.

The ADP151 is capable of 16 fixed output voltage options, ranging from 1.1 V to 3.3 V.

Short-circuit and thermal overload protection circuits prevent damage in adverse conditions. The ADP151 is available in tiny 5-lead TSOT, 6-lead LFCSP, and 4-ball, 0.4 mm pitch, halide-free WLCSP packages for the smallest footprint solution to meet a variety of portable power application requirements.

Rev. D

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
Typical Application Circuit ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
  Input and Output Capacitor, Recommended Specifications .. 4
Absolute Maximum Ratings ... 5
  Thermal Data ... 5
  Thermal Resistance ... 5
  ESD Caution ... 5
Pin Configurations and Function Descriptions ... 6
Typical Performance Characteristics ... 7
Theory of Operation ... 11
Applications Information ... 12
  Capacitor Selection ... 12
  Enable Feature ... 13
  Adjustable Output Voltage Operation ... 13
  Current-Limit and Thermal Overload Protection ... 15
  Thermal Considerations ... 15
Printed Circuit Board Layout Considerations ... 20
Outline Dimensions ... 21
  Ordering Guide ... 22

REVISION HISTORY

3/11—Rev. C to Rev. D

Changes to Current-Limit Threshold Temperature Range ... 4
Added EPAD Notation ... 6
Changes to Ordering Guide ... 22

1/11—Rev. B to Rev. C

Changes to Figure 23 ... 9

12/10—Rev. A to Rev. B

Added LFCSP Package ... Universal
Added Figure 3; Renumbered Sequentially ... 1
Added Table 2 Caption; Renumbered Sequentially ... 4
Changes to Table 4 ... 5
Added Figure 6, Changes to Table 5 ... 6
Changes to Figure 23 ... 9
Changes to Figure 37 and Figure 38 ... 14
Added Figure 51 to Figure 56 ... 18
Added Figure 59 ... 19
Added Figure 62 ... 20
Added Figure 65 ... 21
Updated Outline Dimensions ... 21
Changes to Ordering Guide ... 23

8/10—Rev. 0 to Rev. A

Changes to Figure 8 ... 7
Changes to Figure 15 Caption and Figure 16 Caption ... 8
Changes to Figure 17 Caption and Figure 18 Caption ... 9
Changes to Ordering Guide ... 21

3/10—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.4 V) or 2.2 V, whichever is greater; EN = V_{IN}, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +125°C	2.2		5.5	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 0 µA		10		µA
		I_{OUT} = 0 µA, T_J = −40°C to +125°C			20	µA
		I_{OUT} = 100 µA		20		µA
		I_{OUT} = 100 µA, T_J = −40°C to +125°C			40	µA
		I_{OUT} = 10 mA		60		µA
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			90	µA
		I_{OUT} = 200 mA		265		µA
		I_{OUT} = 200 mA, T_J = −40°C to +125°C			350	µA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND		0.2		µA
		EN = GND, T_J = −40°C to +125°C			1.0	µA
OUTPUT VOLTAGE ACCURACY						
	V_{OUT}	I_{OUT} = 10 mA	−1		+1	%
TSOT/LFCSP	V_{OUT}	T_J = −40°C to +125°C				
		V_{OUT} < 1.8 V				
		100 µA < I_{OUT} < 200 mA, V_{IN} = (V_{OUT} + 0.4 V) to 5.5 V	−3		+2	%
		V_{OUT} ≥1.8 V				
		100 µA < I_{OUT} < 200 mA, V_{IN} = (V_{OUT} + 0.4 V) to 5.5 V	−2.5		+1.5	%
WLCSP	V_{OUT}	T_J = −40°C to +125°C				
		V_{OUT} < 1.8 V				
		100 µA < I_{OUT} < 200 mA, V_{IN} = (V_{OUT} + 0.4 V) to 5.5 V	−2.5		+2	%
		V_{OUT} ≥1.8 V				
		100 µA < I_{OUT} < 200 mA, V_{IN} = (V_{OUT} + 0.4 V) to 5.5 V	−2		+1.5	%
REGULATION						
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.4 V) to 5.5 V, T_J = −40°C to +125°C	−0.05		+0.05	%/V
Load Regulation (TSOT/LFCSP)[1]	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{OUT} < 1.8 V				%/mA
		I_{OUT} = 100 µA to 200 mA		0.006		%/mA
		I_{OUT} = 100 µA to 200 mA, T_J = −40°C to +125°C			0.012	%/mA
		V_{OUT} ≥ 1.8 V				
		I_{OUT} = 100 µA to 200 mA		0.003		%/mA
		I_{OUT} = 100 µA to 200 mA, T_J = −40°C to +125°C			0.008	%/mA
Load Regulation (WLCSP)[1]	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{OUT} < 1.8 V				%/mA
		I_{OUT} = 100 µA to 200 mA		0.004		%/mA
		I_{OUT} = 100 µA to 200 mA, T_J = −40°C to +125°C			0.009	%/mA
		V_{OUT} ≥1.8 V				
		I_{OUT} = 100 µA to 200 mA		0.002		%/mA
		I_{OUT} = 100 µA to 200 mA, T_J = −40°C to +125°C			0.006	%/mA
DROPOUT VOLTAGE[2]	$V_{DROPOUT}$	I_{OUT} = 10 mA		10		mV
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			30	mV
TSOT/LFCSP		I_{OUT} = 200 mA		150		mV
		I_{OUT} = 200 mA, T_J = −40°C to +125°C			230	mV
WLCSP		I_{OUT} = 200 mA		135		mV
		I_{OUT} = 200 mA, T_J = −40°C to +125°C			200	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
START-UP TIME[3]	$t_{START-UP}$	V_{OUT} = 3.3 V		180		μs
CURRENT-LIMIT THRESHOLD[4]	I_{LIMIT}	T_J = 0°C to +125°C	220	300	400	mA
UNDERVOLTAGE LOCKOUT		T_J = −40°C to +125°C				
Input Voltage Rising	$UVLO_{RISE}$				1.96	V
Input Voltage Falling	$UVLO_{FALL}$		1.28			V
Hysteresis	$UVLO_{HYS}$			120		mV
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
EN INPUT						
EN Input Logic High	V_{IH}	2.2 V ≤ V_{IN} ≤ 5.5 V	1.2			V
EN Input Logic Low	V_{IL}	2.2 V ≤ V_{IN} ≤ 5.5 V			0.4	V
EN Input Pull-Down Resistance	R_{EN}	V_{IN} = V_{EN} = 5.5 V		2.6		MΩ
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 3.3 V		9		μV rms
		10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 2.5 V		9		μV rms
		10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 1.1 V		9		μV rms
POWER SUPPLY REJECTION RATIO	PSRR					
$V_{IN} = V_{OUT} + 0.5$ V		10 kHz, V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 10 mA		70		dB
		100 kHz, V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 10 mA		55		dB
$V_{IN} = V_{OUT} + 1$ V		10 kHz, V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 10 mA		70		dB
		100 kHz, V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 10 mA		55		dB
		10 kHz, V_{IN} = 2.2 V, V_{OUT} = 1.1 V, I_{OUT} = 10 mA		70		dB
		100 kHz, V_{IN} = 2.2 V, V_{OUT} = 1.1 V, I_{OUT} = 10 mA		55		dB

[1] Based on an end-point calculation using 0.1 mA and 200 mA loads. See Figure 8 for typical load regulation performance for loads less than 1 mA.

[2] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.2 V.

[3] Start-up time is defined as the time between the rising edge of EN and V_{OUT} being at 90% of its nominal value.

[4] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V (that is, 2.7 V).

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Minimum Input and Output Capacitance[1]	C_{MIN}	T_A = −40°C to +125°C	0.7			μF
Capacitor ESR	R_{ESR}	T_A = −40°C to +125°C	0.001		0.2	Ω

[1] The minimum input and output capacitance should be greater than 0.7 μF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	−0.3 V to +6.5 V
VOUT to GND	−0.3 V to VIN
EN to GND	−0.3 V to +6.5V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Operating Ambient Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP151 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

The maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

The junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in. circuit board. See JESD51-7 and JESD51-9 for detailed information on the board construction. For additional information, see the AN-617 Application Note, *MicroCSP™ Wafer Level Chip Scale Package*, available at www.analog.com.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

See JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
5-Lead TSOT	170	43	°C/W
4-Ball, 0.4 mm Pitch WLCSP	260	58	°C/W
6-Lead 2 mm × 2 mm LFCSP	63.6	28.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

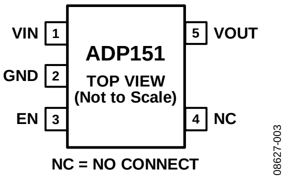


Figure 4. 5-Lead TSOT Pin Configuration

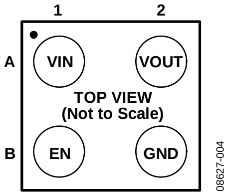
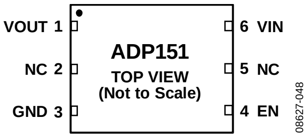


Figure 5. 4-Ball WLCSP Pin Configuration



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED PAD MUST BE CONNECTED TO GROUND.

Figure 6. 6-Lead LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.				
TSOT	**WLCSP**	**LFCSP**	**Mnemonic**	**Description**
1	A1	6	VIN	Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor.
2	B2	3	GND	Ground.
3	B1	4	EN	Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
4	N/A	2	NC	No Connect. Not connected internally.
5	A2	1	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 1 µF or greater capacitor.
N/A	N/A	5	NC	No Connect. Not connected internally.
N/A	N/A		EPAD	Exposed Pad. The exposed pad must be connected to ground. The exposed pad enhances the thermal performance of the package.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1 μF, T_A = 25°C, unless otherwise noted.

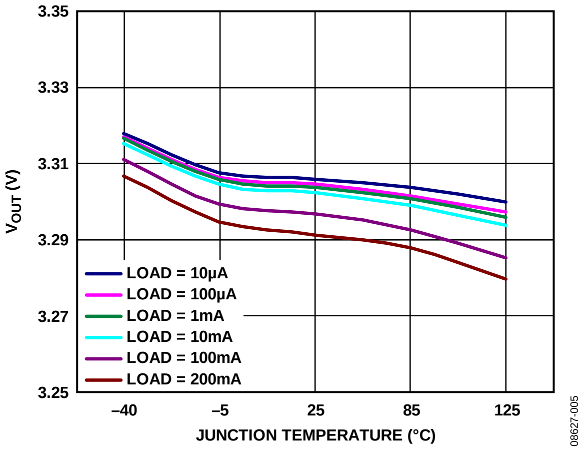


Figure 7. Output Voltage vs. Junction Temperature

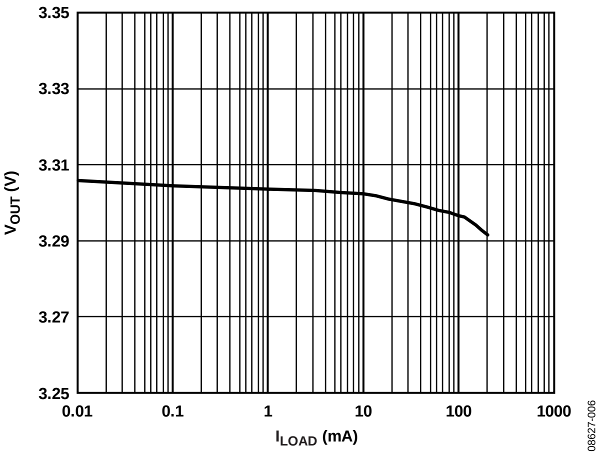


Figure 8. Output Voltage vs. Load Current

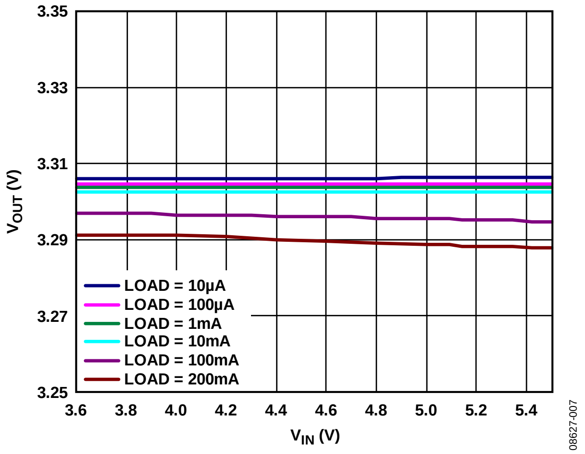


Figure 9. Output Voltage vs. Input Voltage

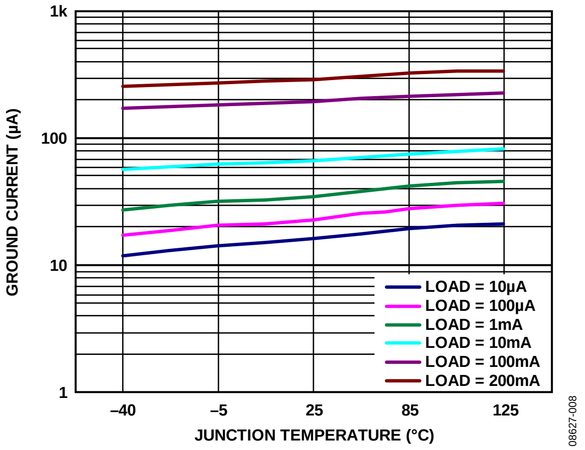


Figure 10. Ground Current vs. Junction Temperature

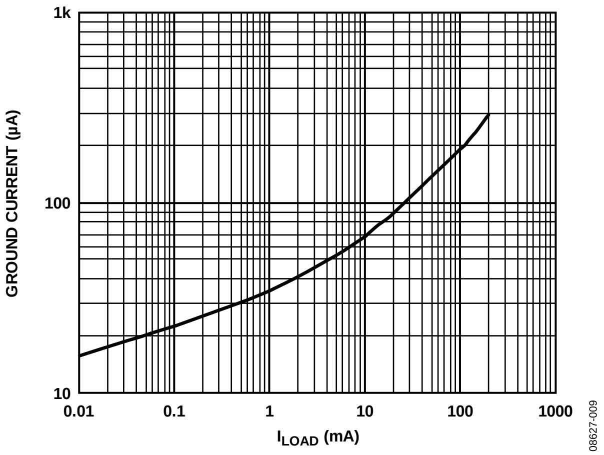


Figure 11. Ground Current vs. Load Current

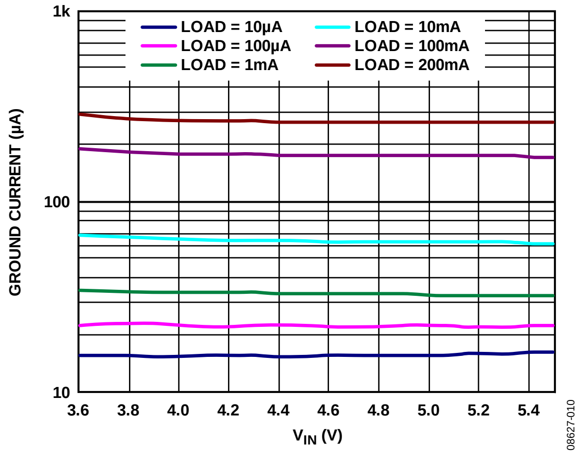


Figure 12. Ground Current vs. Input Voltage

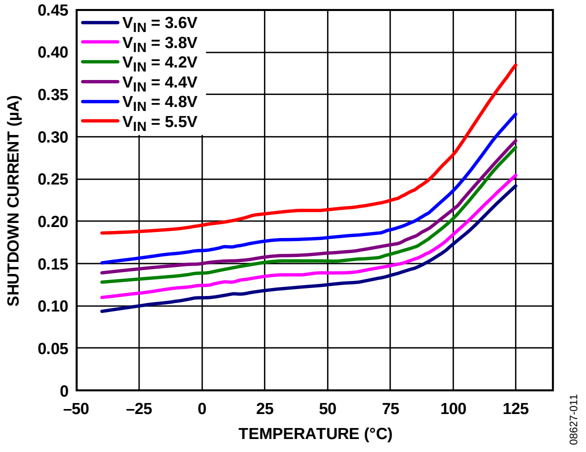


Figure 13. Shutdown Current vs. Temperature at Various Input Voltages

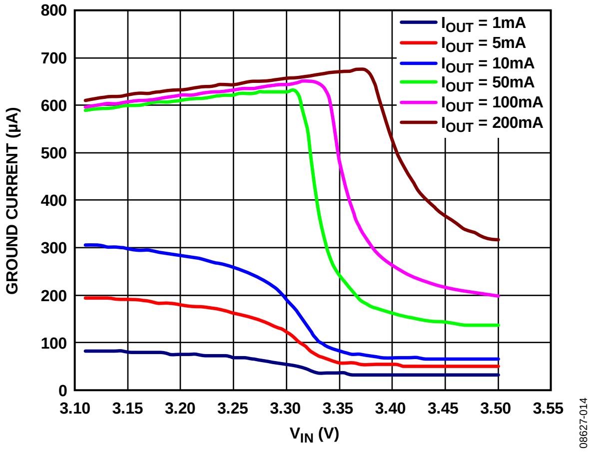


Figure 16. Ground Current vs. Input Voltage (in Dropout)

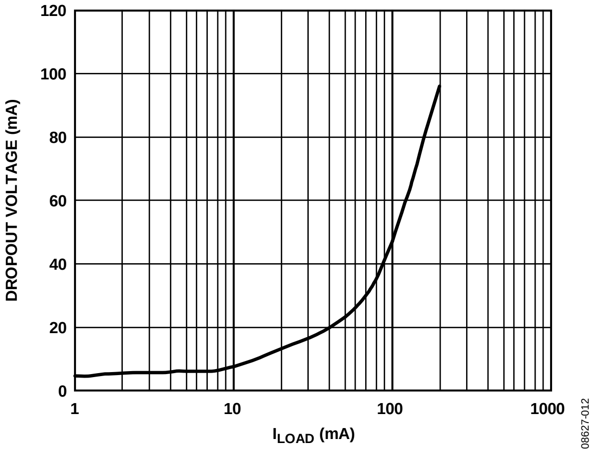


Figure 14. Dropout Voltage vs. Load Current

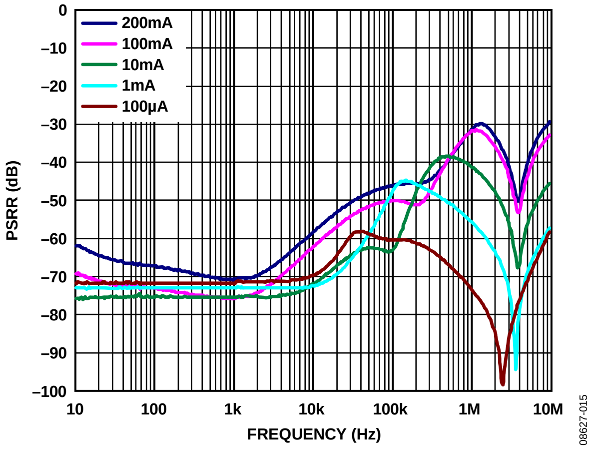


Figure 17. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 1.2 V, V_{IN} = 2.2 V

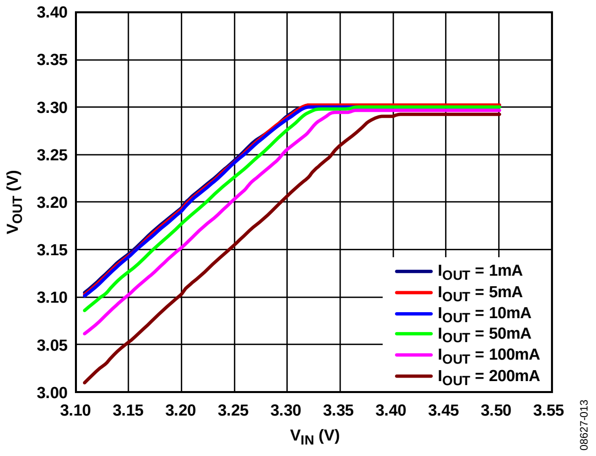


Figure 15. Output Voltage vs. Input Voltage (in Dropout)

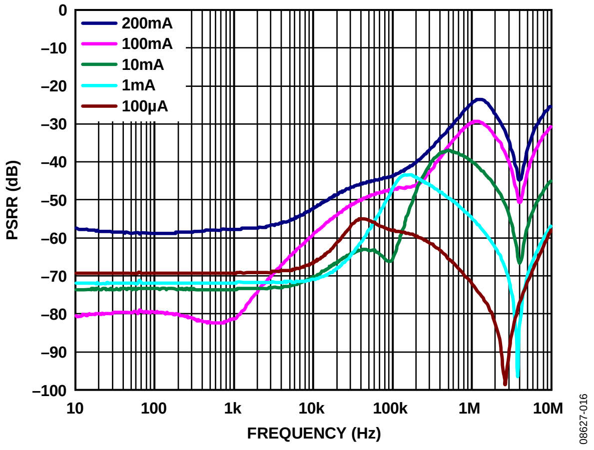


Figure 18. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 2.8 V, V_{IN} = 3.3 V

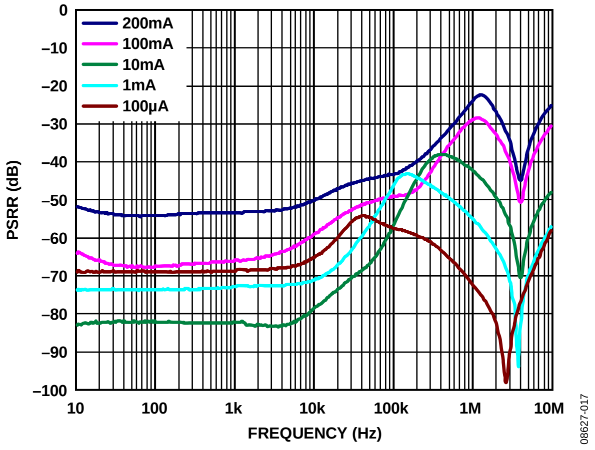


Figure 19. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 3.3 V, V_{IN} = 3.8 V

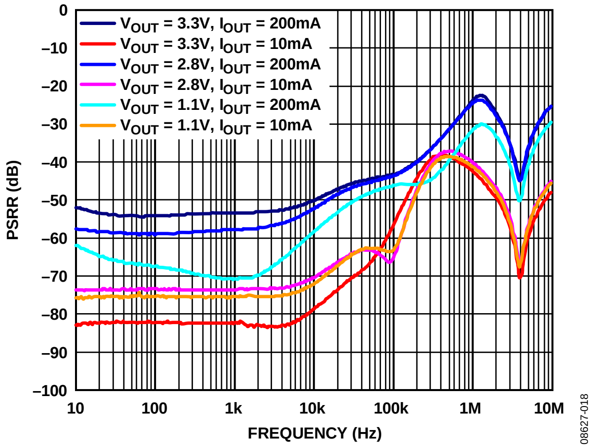


Figure 20. Power Supply Rejection Ratio vs. Frequency at Various Output Voltages and Load Currents, $V_{OUT} – V_{IN}$ = 0.5 V, except for V_{OUT} = 1.1 V, V_{IN} = 2.2 V

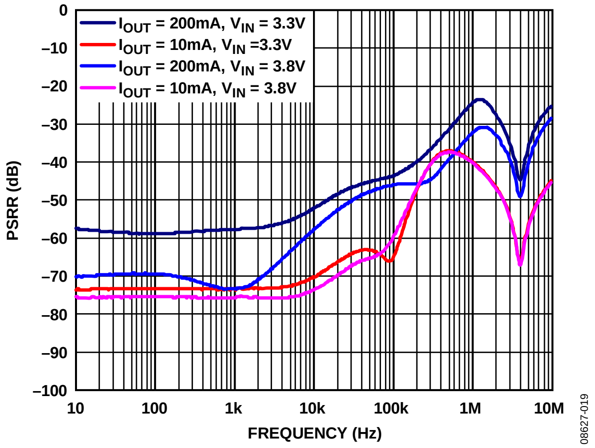


Figure 21. Power Supply Rejection Ratio vs. Frequency at Various Voltages and Load Currents, V_{OUT} = 2.8 V

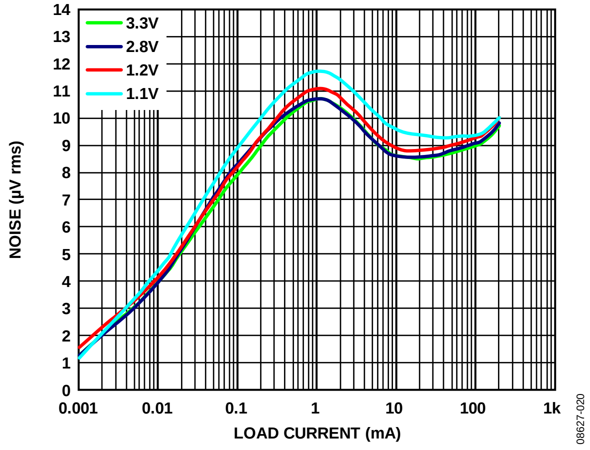


Figure 22. Output Noise vs. Load Current and Output Voltage, V_{IN} = 5 V, C_{OUT} = 1 µF

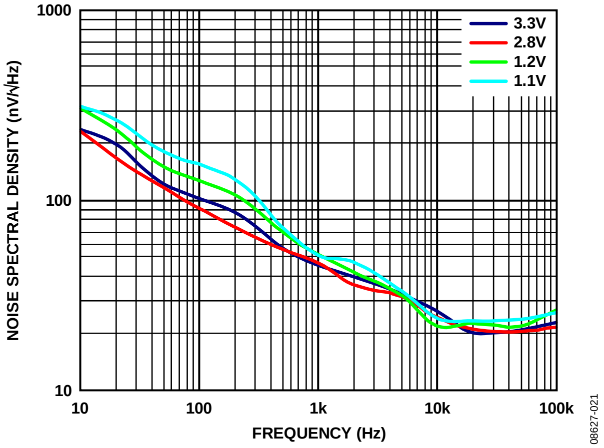


Figure 23. Output Noise Spectral Density vs. Frequency, V_{IN} = 5 V, I_{LOAD} = 10 mA, C_{OUT} = 1 µF

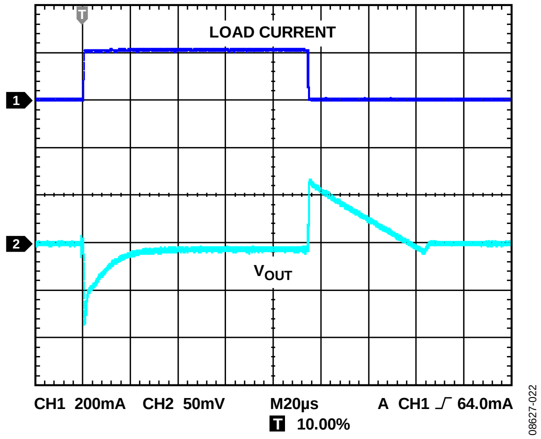


Figure 24. Load Transient Response, C_{IN}, C_{OUT} = 1 µF, I_{LOAD} = 1 mA to 200 mA

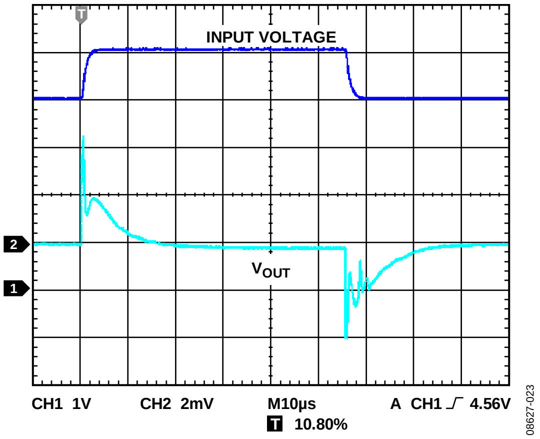


Figure 25. Line Transient Response, C_{IN}, C_{OUT} = 1 µF, I_{LOAD} = 200 mA

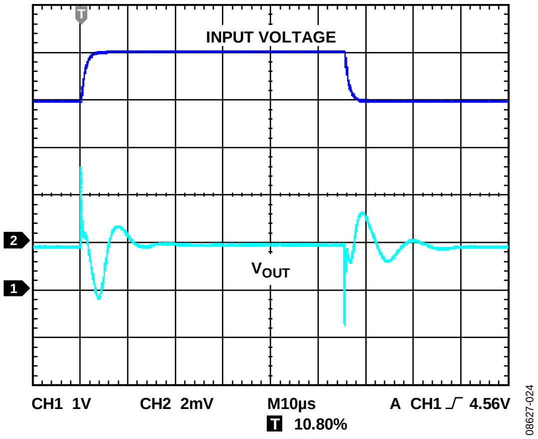


Figure 26. Line Transient Response, C_{IN}, C_{OUT} = 1 µF, I_{LOAD} = 1 mA

THEORY OF OPERATION

The ADP151 is an ultralow noise, low quiescent current, low dropout linear regulator that operates from 2.2 V to 5.5 V and can provide up to 200 mA of output current. Drawing a low 265 μA of quiescent current (typical) at full load makes the ADP151 ideal for battery-operated portable equipment. Shutdown current consumption is typically 200 nA.

Using new innovative design techniques, the ADP151 provides superior noise performance for noise-sensitive analog and RF applications without the need for a noise bypass capacitor. The ADP151 is also optimized for use with small 1 μF ceramic capacitors.

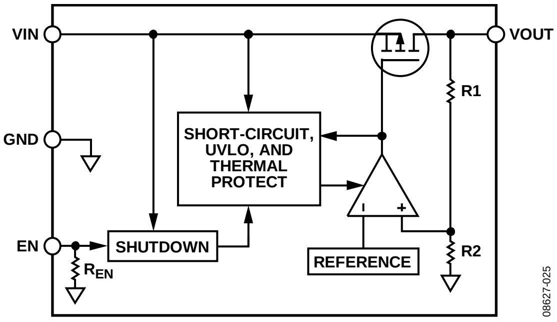


Figure 27. Internal Block Diagram

Internally, the ADP151 consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

An internal pull-down resistor on the EN input holds the input low when the pin is left open.

The ADP151 is available in 16 output voltage options, ranging from 1.1 V to 3.3 V. The ADP151 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is high, VOUT turns on; when EN is low, VOUT turns off. For automatic startup, EN can be tied to VIN.

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP151 is designed for operation with small, space-saving ceramic capacitors but can function with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 1 µF capacitance with an ESR of 1 Ω or less is recommended to ensure the stability of the ADP151. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP151 to large changes in load current. Figure 28 shows the transient responses for an output capacitance value of 1 µF.

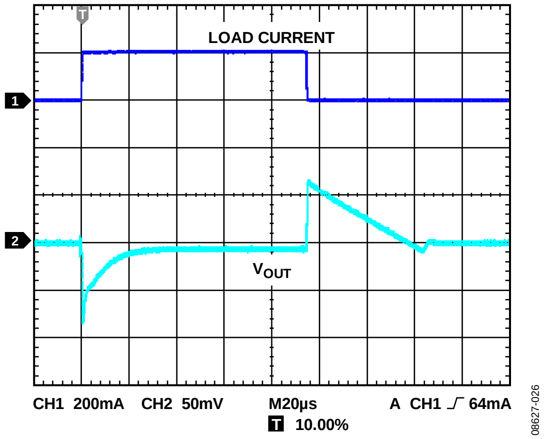


Figure 28. Output Transient Response, C_{OUT} = 1 µF

Input Bypass Capacitor

Connecting a 1 µF capacitor from VIN to GND reduces the circuit sensitivity to the printed circuit board (PCB) layout, especially when long input traces or high source impedance are encountered. If greater than 1 µF of output capacitance is required, the input capacitor should be increased to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitor can be used with the ADP151, as long as it meets the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have an adequate dielectric to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 29 depicts the capacitance vs. voltage bias characteristic of an 0402, 1 µF, 10 V X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is ~±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

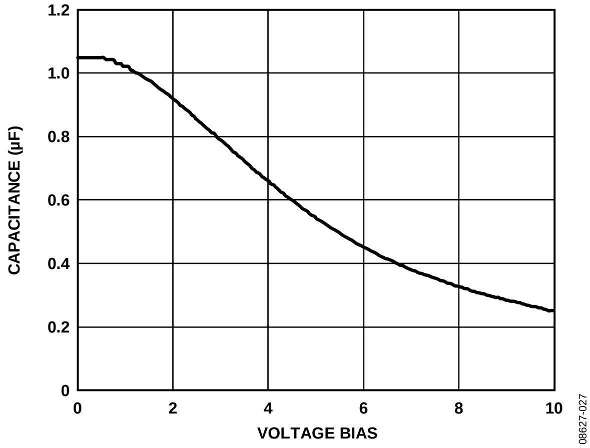


Figure 29. Capacitance vs. Voltage Bias Characteristic

Use Equation 1 to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \tag{1}$$

where:

C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 0.94 µF at 1.8 V, as shown in Figure 29.

Substituting these values in Equation 1 yields

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP151, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

ENABLE FEATURE

The ADP151 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 30, when a rising voltage on EN crosses the active threshold, VOUT turns on. When a falling voltage on EN crosses the inactive threshold, VOUT turns off.

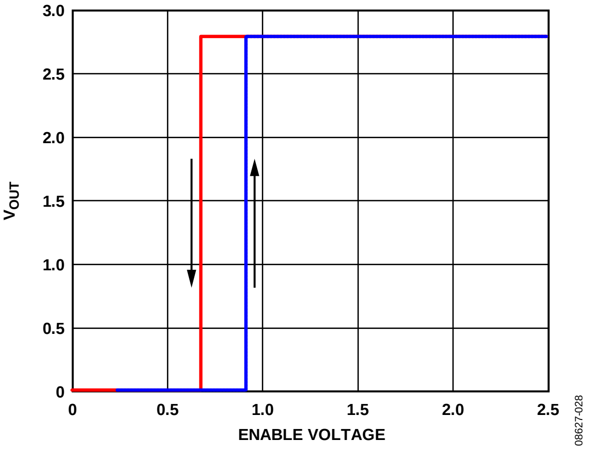


Figure 30. ADP151 Typical EN Pin Operation

As shown in Figure 30, the EN pin has hysteresis built in. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds are derived from the VIN voltage. Therefore, these thresholds vary with changing input voltage. Figure 31 shows typical EN active/inactive thresholds when the input voltage varies from 2.2 V to 5.5 V.

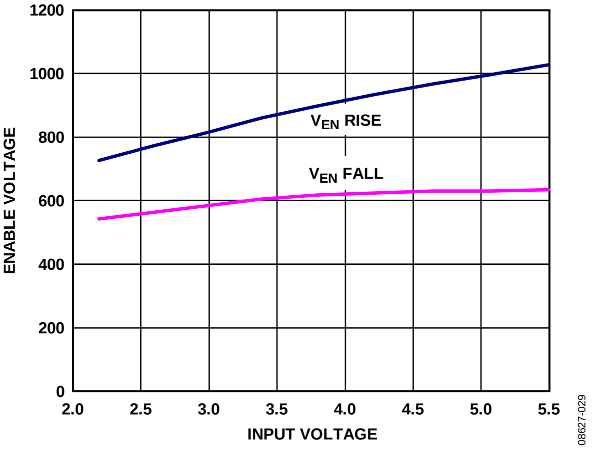


Figure 31. Typical EN Pin Thresholds vs. Input Voltage

The ADP151 uses an internal soft start to limit the inrush current when the output is enabled. The start-up time for the 3.3 V option is approximately 160 µs from the time the EN active threshold is crossed to when the output reaches 90% of its final value. As shown in Figure 32, the start-up time is dependent on the output voltage setting.

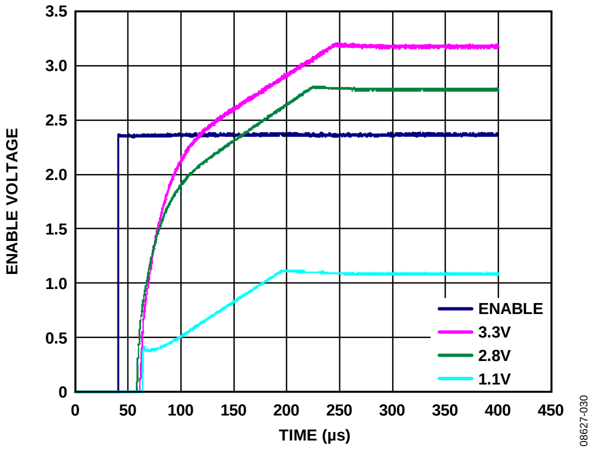


Figure 32. Typical Start-Up Behavior

ADJUSTABLE OUTPUT VOLTAGE OPERATION

The unique architecture of the ADP151 makes an adjustable version difficult to implement in silicon. However, it is possible to create an adjustable regulator at the expense of increasing the quiescent current of the regulator circuit.

The ADP151, and similar LDOs, are designed to regulate the output voltage, V_{OUT}, appearing at the VOUT pin with respect to the GND pin. If the GND pin is at a potential other than 0 V (for example, at V_{OFFSET}), the ADP151 output voltage is $V_{OUT} + V_{OFFSET}$. By taking advantage of this behavior, it is possible to create an adjustable ADP151 circuit that retains most of the desirable characteristics of the ADP151.

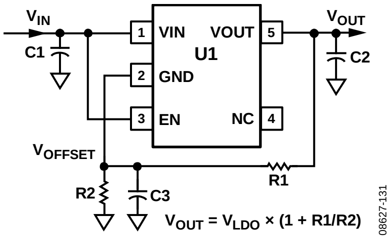


Figure 33. Adjustable LDO Using the ADP151

The circuit shown in Figure 33 is an example of an adjustable LDO using the ADP151. A stable V_{OFFSET} voltage is created by passing a known current through R2. The current through R2 is determined by the voltage across R1. Because the voltage across R1 is set by the voltage between VOUT and GND, the current passing through R2 is fixed, and V_{OFFSET} is stable.

To minimize the effect variation of the ADP151 ground current (I_{GND}) with load, it is best to keep R1 as small as possible. It is also best to size the current passing through R2 to at least 20× greater than the maximum expected ground current.

To create a 4 V LDO circuit, start with the 3.3 V version of the ADP151 to minimize the value of R2. Because V_{OUT} is 4 V, V_{OFFSET} must be 0.7 V, and the current through R2 must be 7 mA. R1 is, therefore, 3.3 V/7 mA or 471 Ω. A 470 Ω standard value introduces less than 1% error. Capacitor C3 is necessary to stabilize the LDO; a value of 1 µF is adequate.

Figure 34 through Figure 38 show the typical performance of the 4 V LDO circuit.

The noise performance of the 4 V LDO circuit is only about 1 µV worse than the same LDO used at 3.3 V because the output noise of the circuit is almost solely determined by the LDO and not the external components. The small difference may be attributed to the internally generated noise in the LDO ground current working with R2. By keeping R2 small, this noise contribution can be minimized.

The PSRR of the 4 V circuit is as much as 10 dB poorer than the 3.3 V LDO with 500 mV of headroom because the ground current of the LDO varies slightly with input voltage. This, in turn, modulates V_{OFFSET} and reduces the PSRR of the regulator. By increasing the headroom to 1 V, the PSRR performance is nearly restored to the performance of the fixed output LDO.

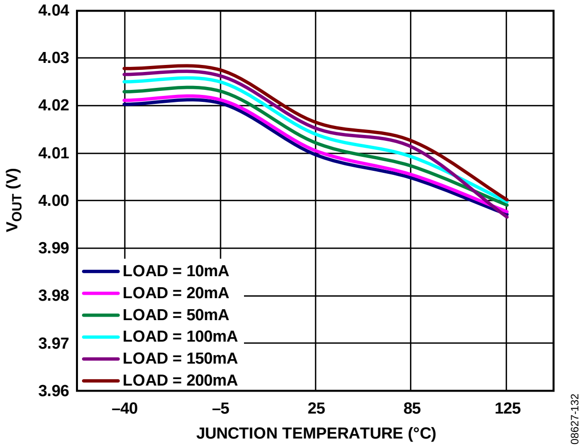


Figure 34. 4 V LDO Circuit, Typical Load Regulation over Temperature

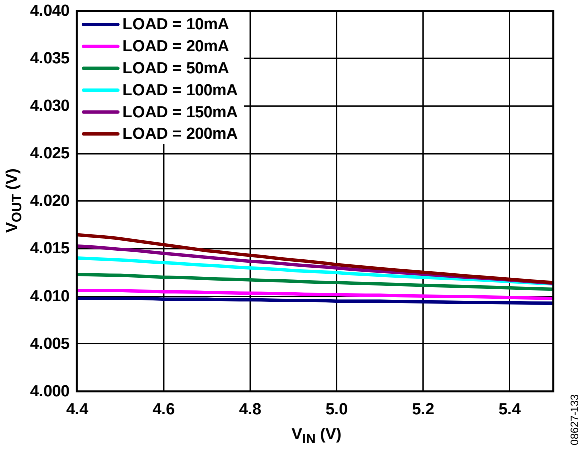


Figure 35. 4 V LDO Circuit, Typical Line Regulation over Load Current

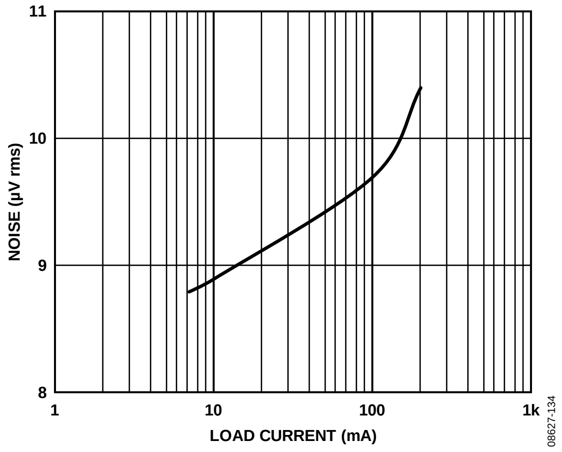


Figure 36. 4 V LDO Circuit, Typical RMS Output Noise, 10 Hz to 100 kHz

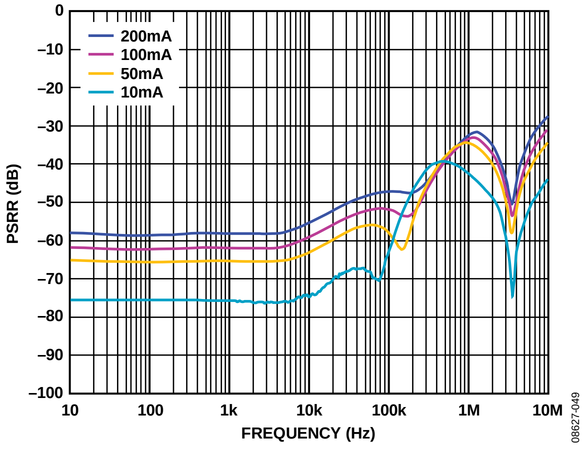


Figure 37. 4 V LDO Circuit, Typical PSRR vs. Load Current, 1 V Headroom

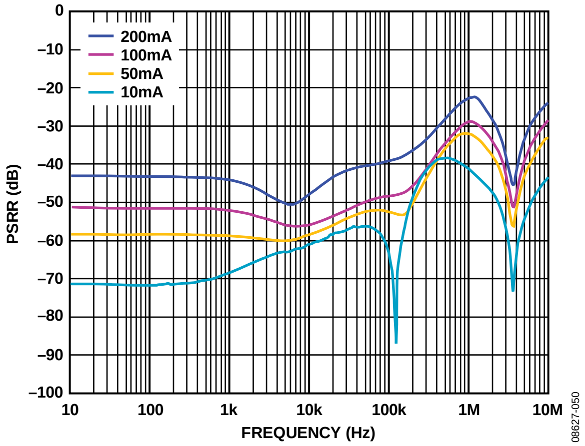


Figure 38. 4 V LDO Circuit, Typical PSRR vs. Load Current, 500 mV Headroom

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP151 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP151 is designed to current limit when the output load reaches 300 mA (typical). When the output load exceeds 300 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to 0. When the junction temperature drops below 135°C, the output is turned on again, and output current is restored to its nominal value.

Consider the case where a hard short from VOUT to ground occurs. At first, the ADP151 current limits, so that only 300 mA is conducted into the short. If self-heating of the junction causes its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to 0. As the junction temperature cools and drops below 135°C, the output turns on and conducts 300 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 300 mA and 0 mA that continues as long as the short remains at the output.

Current- and thermal-limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that junction temperatures do not exceed 125°C.

THERMAL CONSIDERATIONS

In most applications, the ADP151 does not dissipate much heat due to its high efficiency. However, in applications with a high ambient temperature and a high supply voltage to output voltage differential, the heat dissipated in the package can cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 150°C, the converter enters thermal shutdown. It recovers only after the junction temperature has decreased below 135°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is very important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADP151 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pins to the PCB.

Table 6 shows typical θ_{JA} values of the 5-lead TSOT, 6-lead LFCSP, and 4-ball WLCSP packages for various PCB copper sizes. Table 7 shows the typical Ψ_{JB} values of the 5-lead TSOT, 6-lead LFCSP, and 4-ball WLCSP.

Table 6. Typical θ_{JA} Values

	θ_{JA} (°C/W)		
Copper Size (mm²)	**TSOT**	**WLCSP**	**LFCSP**
0[1]	170	260	231.2
50	152	159	161.8
100	146	157	150.1
300	134	153	111.5
500	131	151	91.8

[1] Device soldered to minimum size pin traces.

Table 7. Typical Ψ_{JB} Values

Model	Ψ_{JB} (°C/W)
TSOT	43
WLCSP	58
LFCSP	28.3

The junction temperature of the ADP151 can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (3)$$

where:
I_{LOAD} is the load current.
I_{GND} is the ground current.
V_{IN} and V_{OUT} are input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input-to-output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 39 through Figure 59 show junction temperature calculations for various ambient temperatures, load currents, V_{IN}-to-V_{OUT} differentials, and areas of PCB copper.

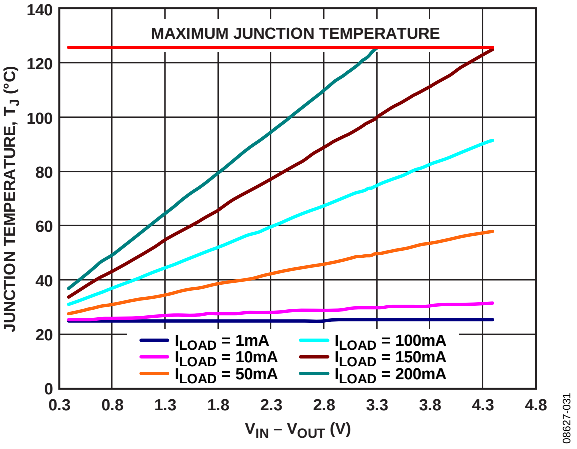


Figure 39. WLCSP 500 mm² of PCB Copper, T_A = 25°C

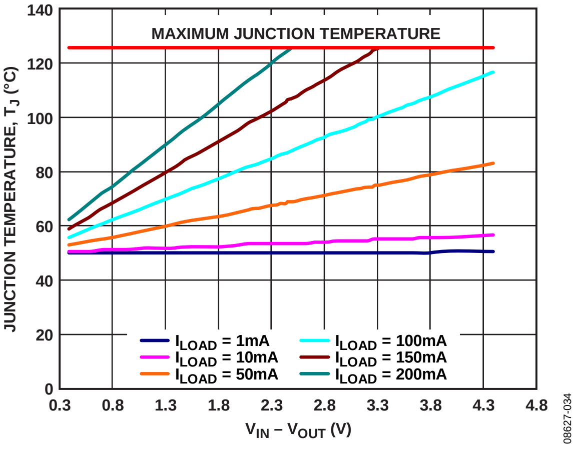


Figure 42. WLCSP 500 mm² of PCB Copper, T_A = 50°C

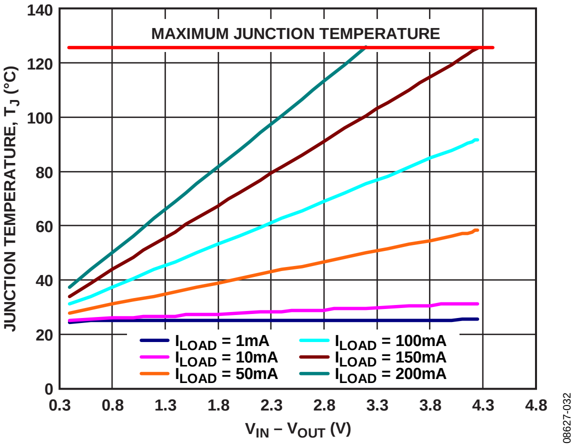


Figure 40. WLCSP 100 mm² of PCB Copper, T_A = 25°C

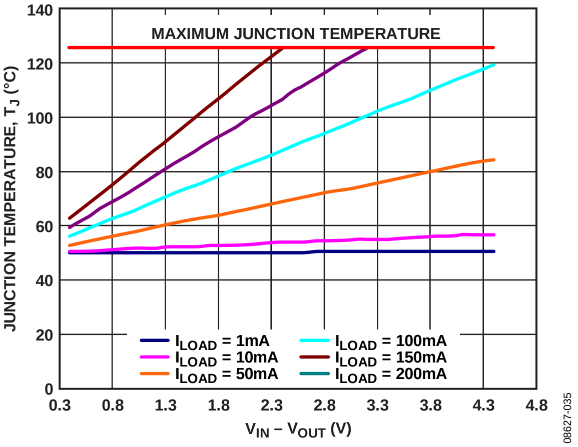


Figure 43. WLCSP 100 mm² of PCB Copper, T_A = 50°C

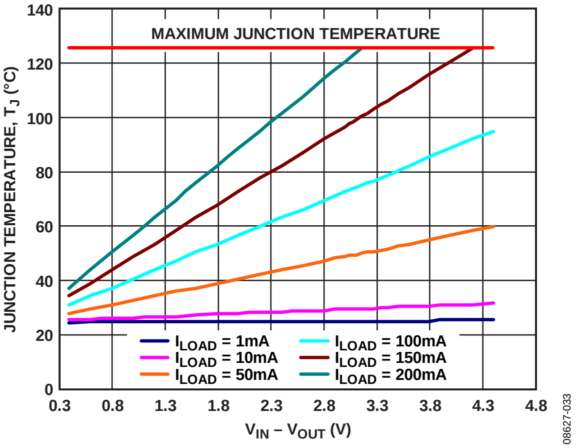


Figure 41. WLCSP 50 mm² of PCB Copper, T_A = 25°C

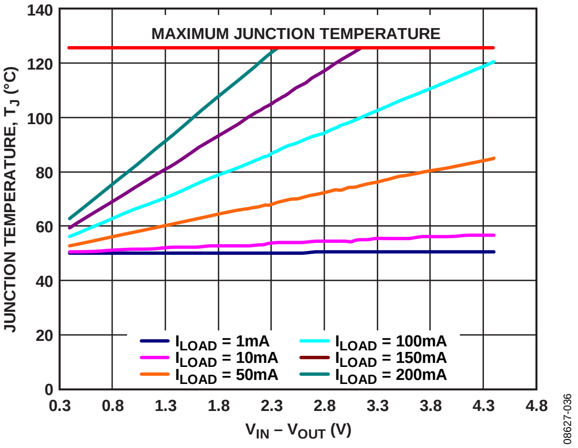


Figure 44. WLCSP 50 mm² of PCB Copper, T_A = 50°C

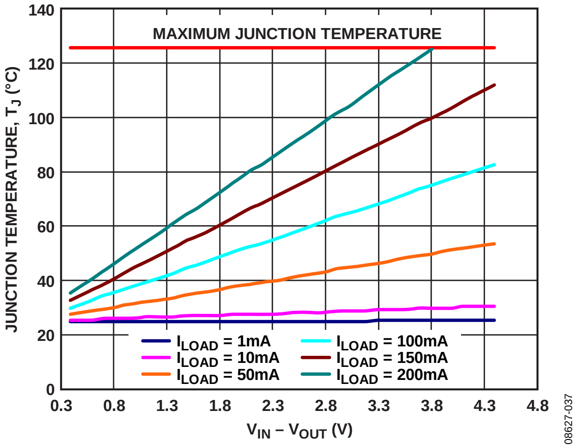


Figure 45. TSOT 500 mm^2 of PCB Copper, T_A = 25°C

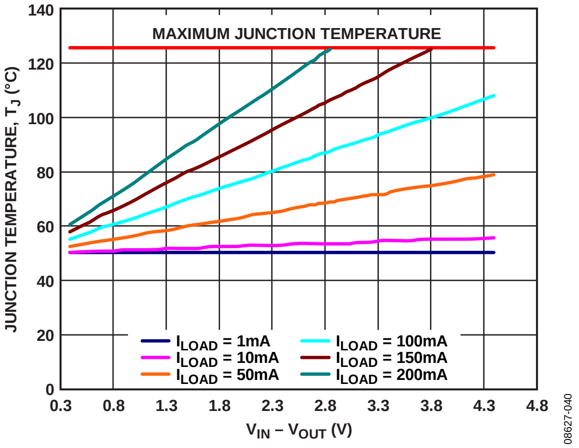


Figure 48. TSOT 500 mm^2 of PCB Copper, T_A = 50°C

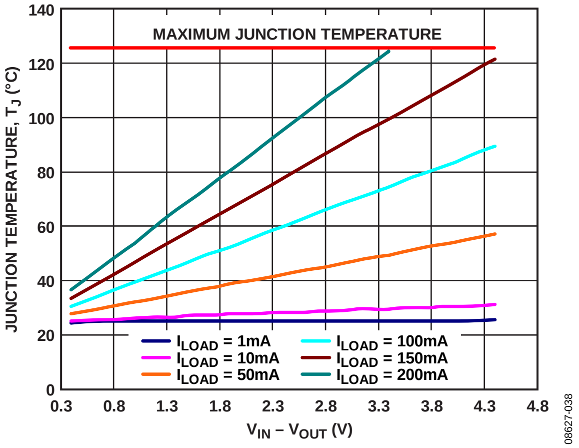


Figure 46. TSOT 100 mm^2 of PCB Copper, T_A = 25°C

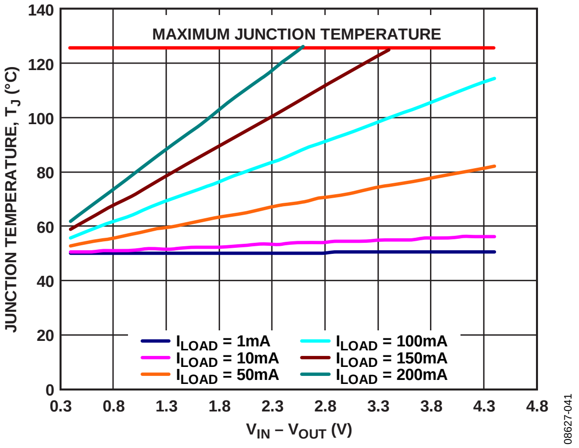


Figure 49. TSOT 100 mm^2 of PCB Copper, T_A = 50°C

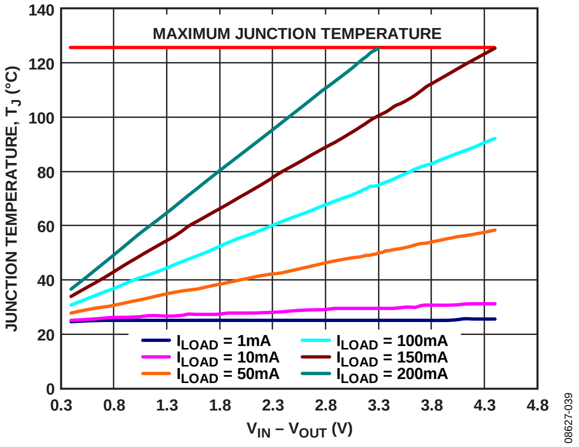


Figure 47. TSOT 50 mm^2 of PCB Copper, T_A = 25°C

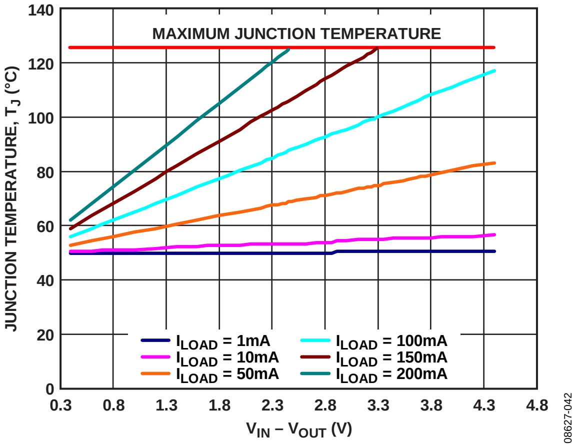


Figure 50. TSOT 50 mm^2 of PCB Copper, T_A = 50°C

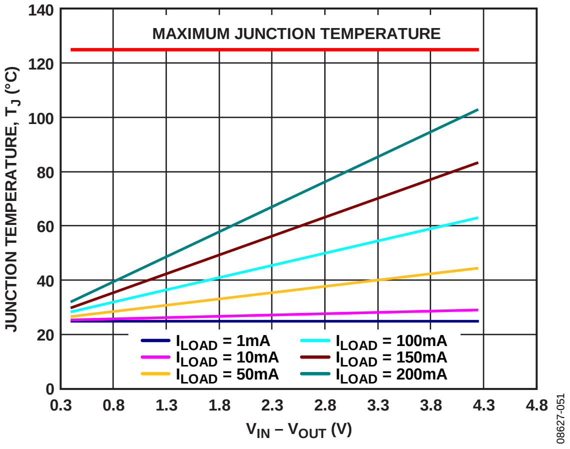


Figure 51. LFCSP 500 mm^2 of PCB Copper, T_A = 25°C

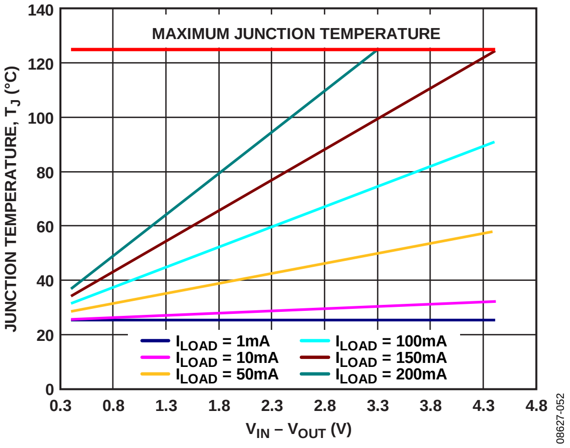


Figure 52. LFCSP 100 mm^2 of PCB Copper, T_A = 25°C

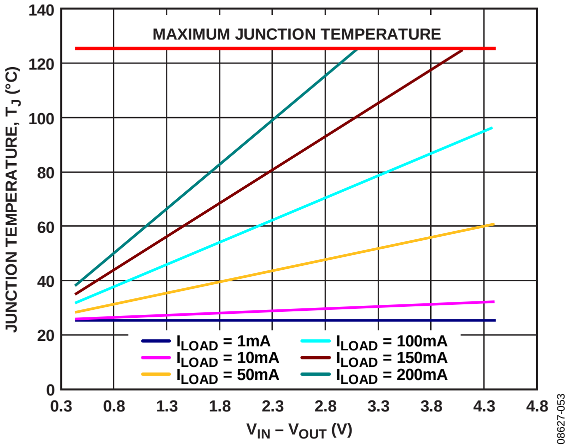


Figure 53. LFCSP 50 mm^2 of PCB Copper, T_A = 25°C

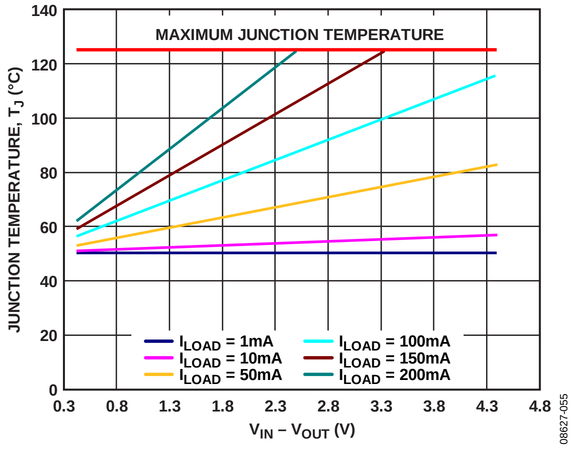


Figure 54. LFCSP 500 mm^2 of PCB Copper, T_A = 50°C

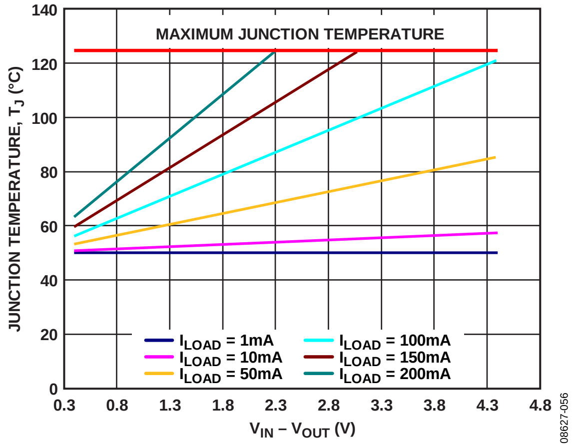


Figure 55. LFCSP 100 mm^2 of PCB Copper, T_A = 50°C

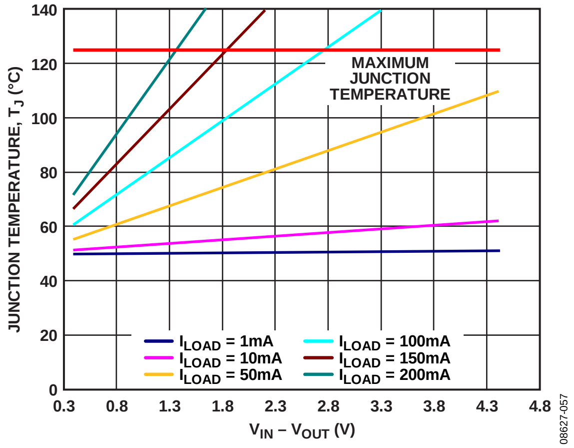


Figure 56. LFCSP 50 mm^2 of PCB Copper, T_A = 50°C

In the case where the board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise (see Figure 57 and Figure 58). Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \tag{5}$$

The typical value of Ψ_{JB} is 58°C/W for the 4-ball WLCSP package, 43°C/W for the 5-lead TSOT package, and 28.3°C/W for the 6-lead LFCSP package.

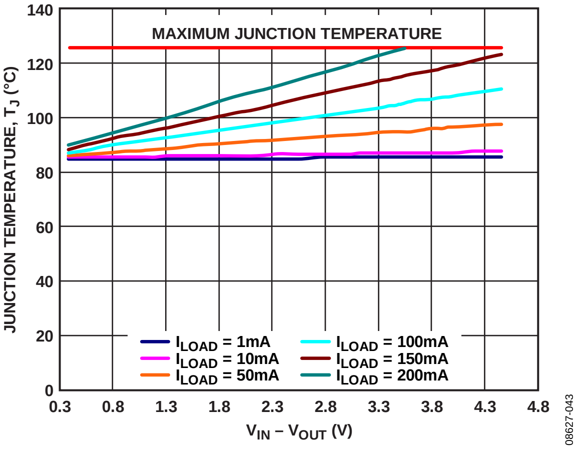


Figure 57. WLCSP, T_A = 85°C

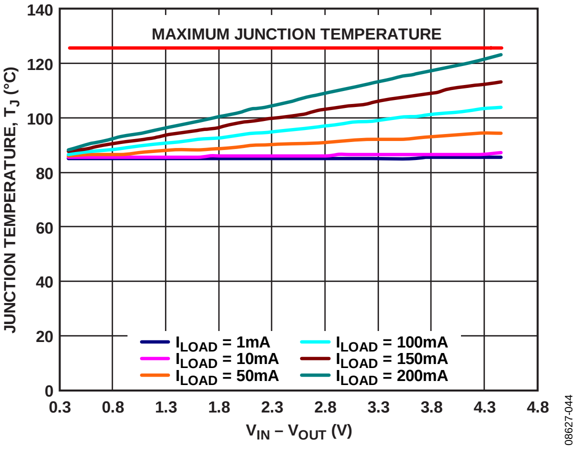


Figure 58. TSOT, T_A = 85°C

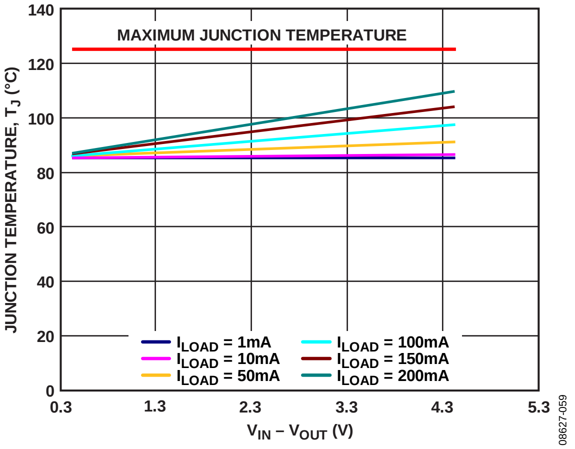


Figure 59. LFCSP, T_A = 85°C

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP151. However, as listed in Table 6, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Use of 0402 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

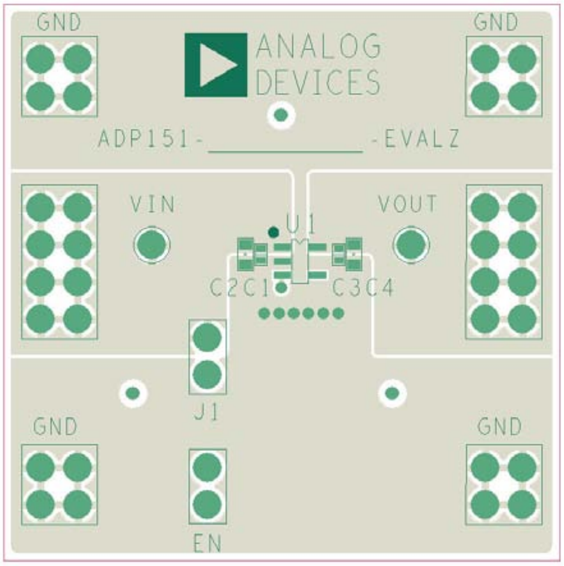


Figure 60. Example TSOT PCB Layout

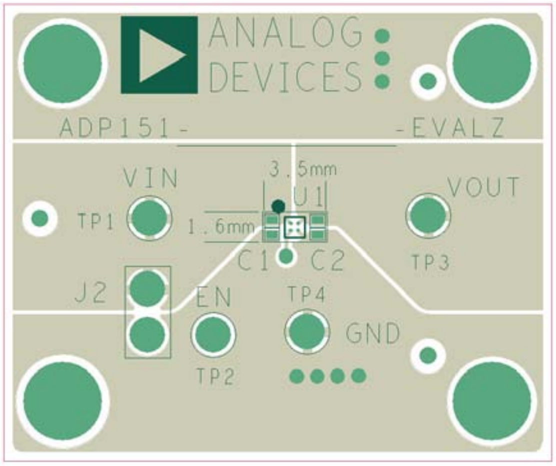


Figure 61. Example WLCSP PCB Layout

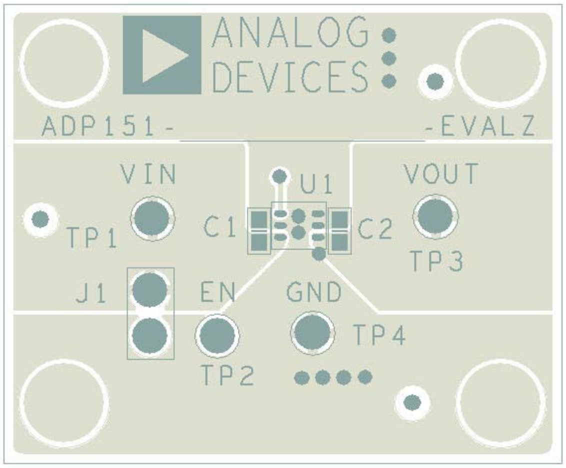


Figure 62. Example LFCSP PCB Layout

OUTLINE DIMENSIONS

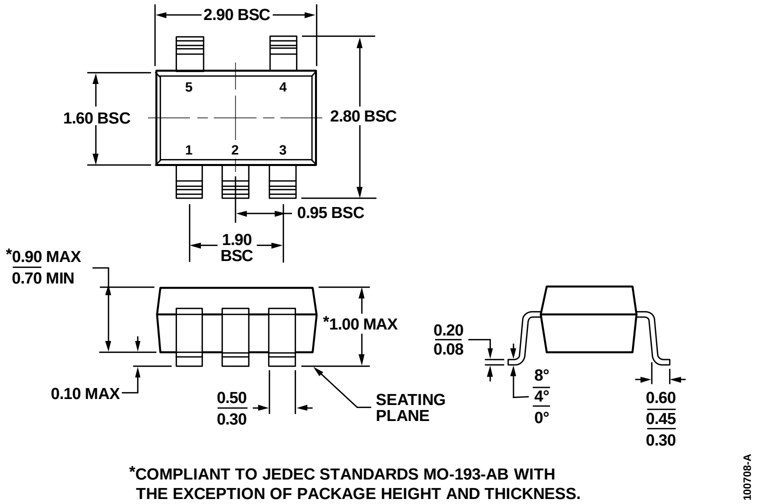


Figure 63. 5-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-5)
Dimensions show in millimeters

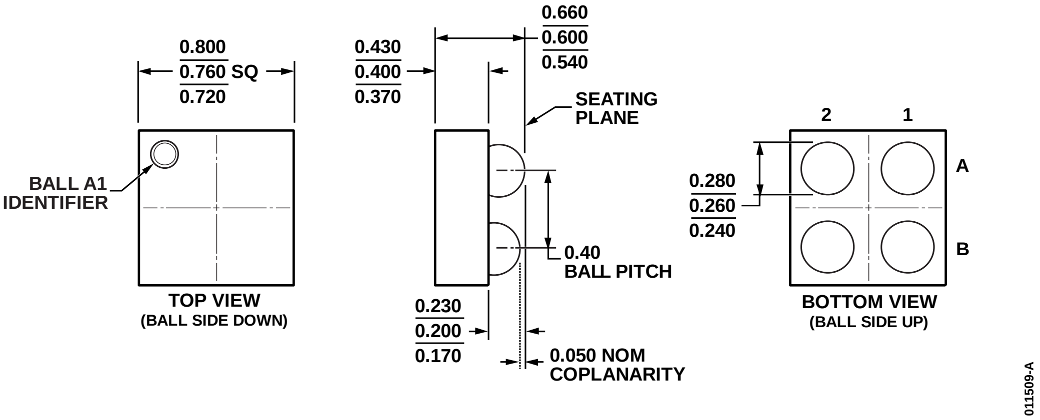


Figure 64. 4-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-4-3)
Dimensions show in millimeters

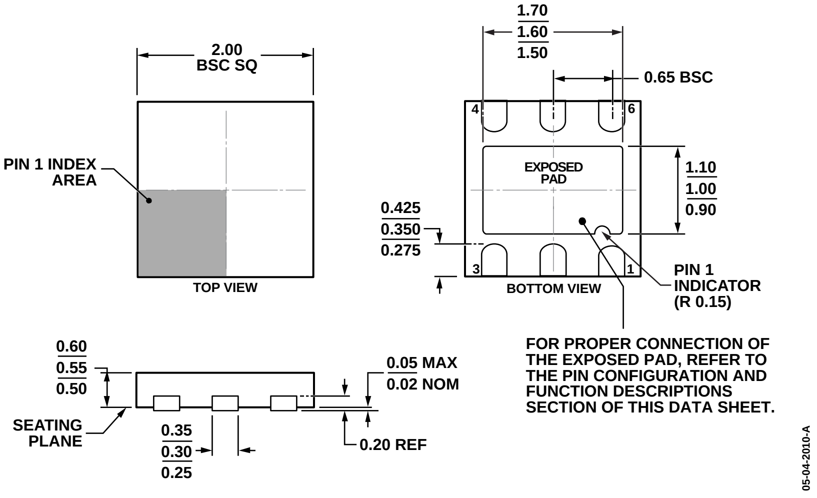


Figure 65. 6-Lead Lead Frame Chip Scale Package [LFCSP_UD]
2.00 mm × 2.00 mm Body, Ultra Thin, Dual Lead
(CP-6-3)
Dimensions show in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)[2]	Package Description	Package Option[3]	Branding
ADP151ACBZ-1.2-R7	−40°C to +125°C	1.2	4-Ball WLCSP	CB-4-3	4R
ADP151ACBZ-1.5-R7	−40°C to +125°C	1.5	4-Ball WLCSP	CB-4-3	4S
ADP151ACBZ-1.8-R7	−40°C to +125°C	1.8	4-Ball WLCSP	CB-4-3	4T
ADP151ACBZ-2.5-R7	−40°C to +125°C	2.5	4-Ball WLCSP	CB-4-3	4U
ADP151ACBZ-2.75-R7	−40°C to +125°C	2.75	4-Ball WLCSP	CB-4-3	4V
ADP151ACBZ-2.8-R7	−40°C to +125°C	2.8	4-Ball WLCSP	CB-4-3	4X
ADP151ACBZ-2.85-R7	−40°C to +125°C	2.85	4-Ball WLCSP	CB-4-3	4Y
ADP151ACBZ-3.0-R7	−40°C to +125°C	3.0	4-Ball WLCSP	CB-4-3	4Z
ADP151ACBZ-3.3-R7	−40°C to +125°C	3.3	4-Ball WLCSP	CB-4-3	50
ADP151ACBZ-2.1-R7	−40°C to +125°C	2.1	4-Ball WLCSP	CB-4-3	5E
ADP151AUJZ-1.2-R7	−40°C to +125°C	1.2	5-Lead TSOT	UJ-5	LF6
ADP151AUJZ-1.5-R7	−40°C to +125°C	1.5	5-Lead TSOT	UJ-5	LF7
ADP151AUJZ-1.8-R7	−40°C to +125°C	1.8	5-Lead TSOT	UJ-5	LF8
ADP151AUJZ-2.5-R7	−40°C to +125°C	2.5	5-Lead TSOT	UJ-5	LF9
ADP151AUJZ-2.8-R7	−40°C to +125°C	2.8	5-Lead TSOT	UJ-5	LFG
ADP151AUJZ-3.0-R7	−40°C to +125°C	3.0	5-Lead TSOT	UJ-5	LFH
ADP151AUJZ-3.3-R7	−40°C to +125°C	3.3	5-Lead TSOT	UJ-5	LFJ
ADP151ACPZ-1.2-R7	−40°C to +125°C	1.2	6-Lead LFCSP_UD	CP-6-3	LF6
ADP151ACPZ-1.5-R7	−40°C to +125°C	1.5	6-Lead LFCSP_UD	CP-6-3	LF7
ADP151ACPZ-1.8-R7	−40°C to +125°C	1.8	6-Lead LFCSP_UD	CP-6-3	LF8
ADP151ACPZ-2.5-R7	−40°C to +125°C	2.5	6-Lead LFCSP_UD	CP-6-3	LF9
ADP151ACPZ-2.7-R7	−40°C to +125°C	2.7	6-Lead LFCSP_UD	CP-6-3	LKZ
ADP151ACPZ-2.8-R7	−40°C to +125°C	2.8	6-Lead LFCSP_UD	CP-6-3	LFG
ADP151ACPZ-3.0-R7	−40°C to +125°C	3.0	6-Lead LFCSP_UD	CP-6-3	LFH
ADP151ACPZ-3.3-R7	−40°C to +125°C	3.3	6-Lead LFCSP_UD	CP-6-3	LFJ
ADP151UJZ-REDYKIT			Evaluation Board Kit		
ADP151CPZ-REDYKIT			Evaluation Board Kit		
ADP151CB-3.3-EVALZ			Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] For additional voltage options for the ADP151ACBZ package option, contact a local Analog Devices, Inc., sales or distribution representative.
[3] The ADP151ACBZ package option is halide free.

NOTES

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