

# SC70/ $\mu$ DFN, Single/Dual Low-Voltage, Low-Power $\mu$ P Reset Circuits

## General Description

The MAX6381–MAX6390 microprocessor ( $\mu$ P) supervisory circuits monitor power-supply voltages from +1.8V to +5.0V while consuming only 3 $\mu$ A of supply current at +1.8V. Whenever  $V_{CC}$  falls below the factory-set reset thresholds, the reset output asserts and remains asserted for a minimum reset timeout period after  $V_{CC}$  rises above the reset threshold. Reset thresholds are available from +1.58V to +4.63V, in approximately 100mV increments. Seven minimum reset timeout delays ranging from 1ms to 1200ms are available.

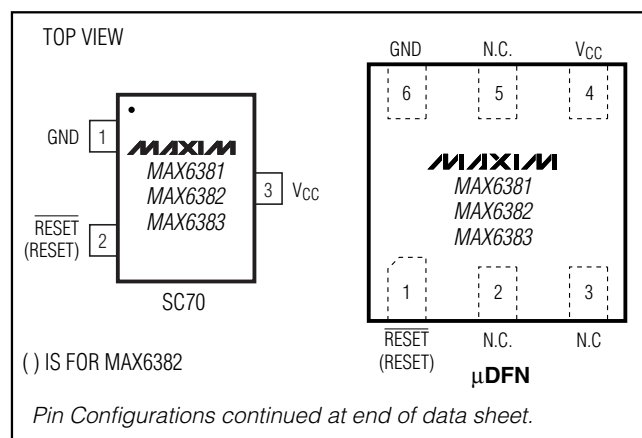
The MAX6381/MAX6384/MAX6387 have a push-pull active-low reset output. The MAX6382/MAX6385/MAX6388 have a push-pull active-high reset output, and the MAX6383/MAX6386/MAX6389/MAX6390 have an open-drain active-low reset output. The MAX6384/MAX6385/MAX6386 also feature a debounced manual reset input (with internal pullup resistor). The MAX6387/MAX6388/MAX6389 have an auxiliary input for monitoring a second voltage. The MAX6390 offers a manual reset input with a longer  $V_{CC}$  reset timeout period (1120ms or 1200ms) and a shorter manual reset timeout (140ms or 150ms).

The MAX6381/MAX6382/MAX6383 are available in 3-pin SC70 and 6-pin  $\mu$ DFN packages and the MAX6384–MAX6390 are available in 4-pin SC70 and 6-pin  $\mu$ DFN packages.

## Applications

Computers	Critical $\mu$ P and $\mu$ C
Controllers	Power Monitoring
Intelligent Instruments	Portable/Battery-Powered Equipment
	Dual Voltage Systems

## Pin Configurations



## Features

- ◆ Factory-Set Reset Threshold Voltages Ranging from +1.58V to +4.63V in Approximately 100mV Increments
- ◆  $\pm 2.5\%$  Reset Threshold Accuracy Over Temperature (-40°C to +125°C)
- ◆ Seven Reset Timeout Periods Available: 1ms, 20ms, 140ms, 280ms, 560ms, 1120ms, 1200ms (min)
- ◆ 3 Reset Output Options
  - Active-Low Push-Pull
  - Active-High Push-Pull
  - Active-Low Open-Drain
- ◆ Reset Output State Guaranteed Valid Down to  $V_{CC} = 1V$
- ◆ Manual Reset Input (MAX6384/MAX6385/MAX6386)
- ◆ Auxiliary RESET IN (MAX6387/MAX6388/MAX6389)
- ◆  $V_{CC}$  Reset Timeout (1120ms or 1200ms)/Manual Reset Timeout (140ms or 150ms) (MAX6390)
- ◆ Negative-Going  $V_{CC}$  Transient Immunity
- ◆ Low Power Consumption of 6 $\mu$ A at +3.6V and 3 $\mu$ A at +1.8V
- ◆ Pin Compatible with MAX809/MAX810/MAX803/MAX6326/MAX6327/MAX6328/MAX6346/MAX6347/MAX6348, and MAX6711/MAX6712/MAX6713
- ◆ Tiny 3-Pin/4-Pin SC70 and 6-Pin  $\mu$ DFN Packages

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX6381LT_ _D_+T	-40°C to +125°C	6 $\mu$ DFN-6	L611-1
MAX6381XR_ _D_+T	-40°C to +125°C	3 SC70-3	X3-2
MAX6382LT_ _D_+T	-40°C to +125°C	6 $\mu$ DFN-6	L611-1
MAX6382XR_ _D_+T	-40°C to +125°C	3 SC70-3	X3-2

**Note:** Insert reset threshold suffix (see Reset Threshold table) after "XR", "XS", or "LT." Insert reset timeout delay (see Reset Timeout Delay table) after "D" to complete the part number. Sample stock is generally held on standard versions only (see Standard Versions table). Standard versions have an order increment requirement of 2500 pieces. Nonstandard versions have an order increment requirement of 10,000 pieces. Contact factory for availability of nonstandard versions.

+Denotes a lead-free package.

Ordering Information continued at end of data sheet.  
 Typical Operating Circuit appears at end of data sheet.  
 Selector Guide appears at end of data sheet.

# SC70/ $\mu$ DFN, Single/Dual Low-Voltage, Low-Power $\mu$ P Reset Circuits

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$ to GND .....	-0.3V to +6.0V
RESET Open-Drain Output .....	-0.3V to +6.0V
RESET, RESET (push-pull output) .....	-0.3V to ( $V_{CC}$ + 0.3V)
MR, RESET IN .....	-0.3V to ( $V_{CC}$ + 0.3V)
Input Current ( $V_{CC}$ ) .....	20mA
Output Current (all pins) .....	20mA

Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )	
3-Pin SC70 (derate 2.9mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$ ) .....	235mW
4-Pin SC70 (derate 3.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$ ) .....	245mW
6-Pin $\mu$ DFN (derate 2.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$ ) .....	167.7mW
Operating Temperature Range .....	$-40^\circ\text{C}$ to $+125^\circ\text{C}$
Storage Temperature Range .....	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (soldering, 10s) .....	$+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{CC}$  = full range,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise specified. Typical values are at  $T_A = +25^\circ\text{C}$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	$V_{CC}$		1.0		5.5	V
$V_{CC}$ Supply Current	$I_{CC}$	$V_{CC} = 5.5\text{V}$ , no load		7	13	$\mu\text{A}$
		$V_{CC} = 3.6\text{V}$ , no load		6	11	
		$V_{CC} = 2.5\text{V}$ , no load		4	7	
		$V_{CC} = 1.8\text{V}$ , no load		3	6	
$V_{CC}$ Reset Threshold (See Reset Thresholds table)	$V_{TH}$	$T_A = +25^\circ\text{C}$	$V_{TH} - 1.5\%$	$V_{TH}$	$V_{TH} + 1.5\%$	V
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	$V_{TH} - 2.5\%$	$V_{TH}$	$V_{TH} + 2.5\%$	
Reset Threshold Tempco	$\Delta V_{TH}/^\circ\text{C}$			60		ppm/ $^\circ\text{C}$
$V_{CC}$ to Reset Delay		$V_{CC}$ falling at $10\text{mV}/\mu\text{s}$ from $V_{TH} + 100\text{mV}$ to $V_{TH} - 100\text{mV}$		35		$\mu\text{s}$
Reset Timeout Period MAX6381-MAX6389 (See Reset Timeout table)	$t_{RP}$	D1	1		2	ms
		D2	20		40	
		D3	140		280	
		D5	280		560	
		D6	560		1120	
		D4	1120		2240	
		D7	1200		2400	
Reset Timeout Period MAX6390	$t_{RP}$	$\overline{\text{MR}}$ timeout period	D4	140	280	ms
			D7	150	300	
		$V_{CC}$ timeout period	D4	1120	2240	
			D7	1200	2400	
$\overline{\text{MR}}$ Input Voltage	$V_{IL}$	$V_{TH} < 4\text{V}$			$0.3 \times V_{CC}$	V
	$V_{IH}$			$0.7 \times V_{CC}$		
	$V_{IL}$	$V_{TH} > 4\text{V}$			0.8	
	$V_{IH}$			2.4		

# SC70/ $\mu$ DFN, Single/Dual Low-Voltage, Low-Power $\mu$ P Reset Circuits

MAX6381-MAX6390

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC}$  = full range,  $T_A$  = -40°C to +125°C, unless otherwise specified. Typical values are at  $T_A$  = +25°C.) (Note 1)

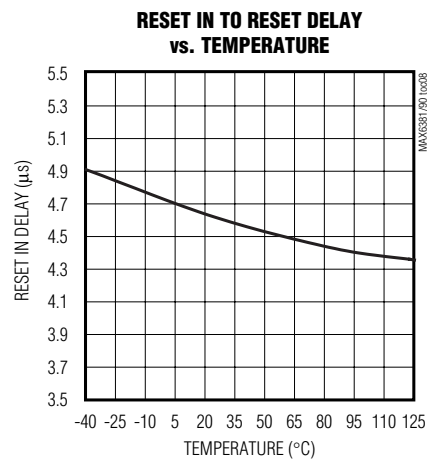
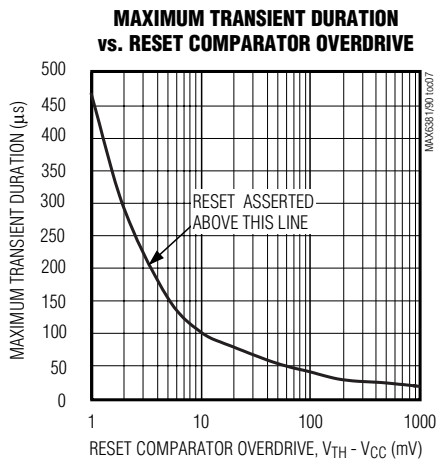
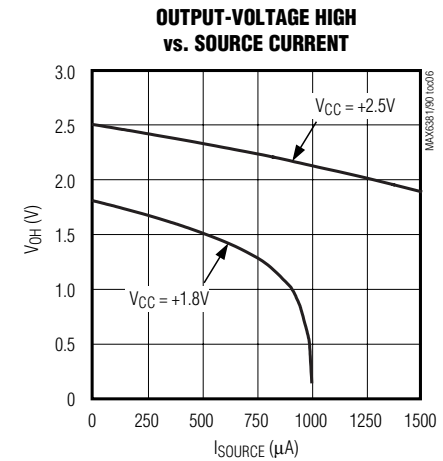
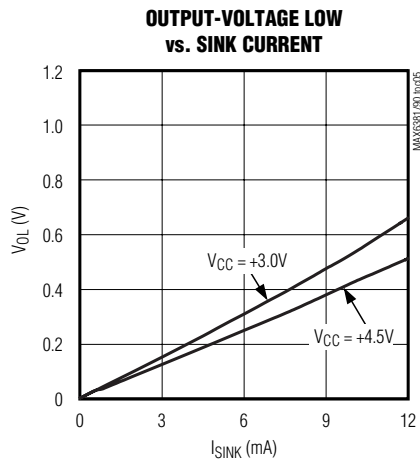
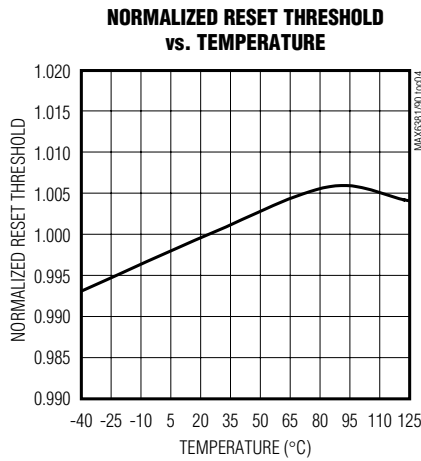
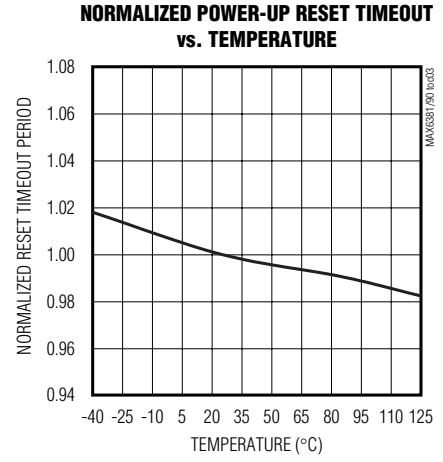
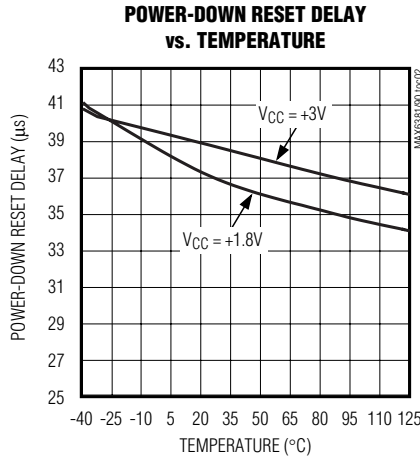
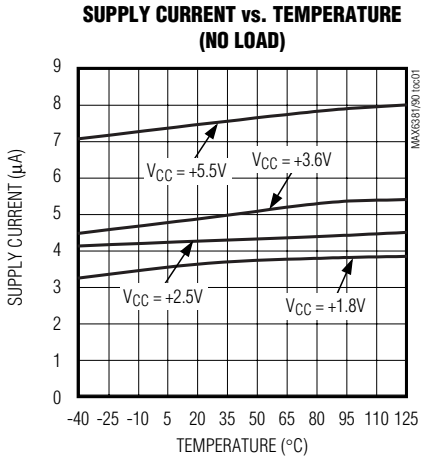
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
$\overline{MR}$ Minimum Input Pulse Width			1			$\mu$ s	
$\overline{MR}$ Glitch Rejection				100		ns	
$\overline{MR}$ to Reset Delay				200		ns	
$\overline{MR}$ Internal Pullup Resistance		MAX6381-MAX6389	32	63	100	k $\Omega$	
		MAX6390	500	1560	3000	$\Omega$	
RESET IN Input Threshold	$V_{THRST}$	$T_A$ = +25°C	1.245	1.27	1.295	V	
		$T_A$ = 0°C to +85°C	1.232		1.308		
		$T_A$ = -40°C to +125°C	1.219		1.321		
RESET IN to RESET Delay		$V_{RESETIN}$ falling at 4mV/ $\mu$ s from $V_{THRST} + 40$ mV to $V_{THRST} - 40$ mV		4.5		$\mu$ s	
RESET IN Input Leakage Current	$I_{RESETIN}$		-50	$\pm 1$	+50	nA	
Open-Drain $\overline{RESET}$ Output Voltage	$V_{OL}$	$V_{CC} \geq 4.5$ V, $I_{SINK} = 3.2$ mA, reset asserted			0.4	V	
		$V_{CC} \geq 2.5$ V, $I_{SINK} = 1.2$ mA, reset asserted			0.3		
		$V_{CC} \geq 1.0$ V, $I_{SINK} = 80$ $\mu$ A, reset asserted			0.3		
Open-Drain $\overline{RESET}$ Output Leakage Current	$I_{LKG}$	$V_{CC} > V_{TH}$ , $\overline{RESET}$ not asserted			1.0	$\mu$ A	
Push-Pull $\overline{RESET}$ Output Voltage	$V_{OL}$	$V_{CC} \geq 4.5$ V, $I_{SINK} = 3.2$ mA, reset asserted			0.4	V	
		$V_{CC} \geq 2.5$ V, $I_{SINK} = 1.2$ mA, reset asserted			0.3		
		$V_{CC} \geq 1.0$ V, $I_{SINK} = 80$ $\mu$ A, reset asserted			0.3		
	$V_{OH}$	$V_{CC} \geq 4.5$ V, $I_{SOURCE} = 800$ $\mu$ A, reset not asserted		0.8 x $V_{CC}$			
		$V_{CC} \geq 2.5$ V, $I_{SOURCE} = 500$ $\mu$ A, reset not asserted		0.8 x $V_{CC}$			
Push-Pull RESET Output Voltage	$V_{OH}$	$V_{CC} \geq 4.5$ V, $I_{SOURCE} = 800$ $\mu$ A, reset asserted		0.8 x $V_{CC}$		V	
		$V_{CC} \geq 2.5$ V, $I_{SOURCE} = 500$ $\mu$ A, reset asserted		0.8 x $V_{CC}$			
		$V_{CC} \geq 1.8$ V, $I_{SOURCE} = 150$ $\mu$ A, reset asserted		0.8 x $V_{CC}$			
		$V_{CC} \geq 1.0$ V, $I_{SOURCE} = 1$ $\mu$ A, reset asserted		0.8 x $V_{CC}$			
	$V_{OL}$	$V_{CC} \geq 4.5$ V, $I_{SINK} = 3.2$ mA, reset not asserted			0.4		
		$V_{CC} \geq 2.5$ V, $I_{SINK} = 1.2$ mA, reset not asserted			0.3		

**Note 1:** Specifications over temperature are guaranteed by design, not production tested.

# SC70/ $\mu$ DFN, Single/Dual Low-Voltage, Low-Power $\mu$ P Reset Circuits

## Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



# SC70/ $\mu$ DFN, Single/Dual Low-Voltage, Low-Power $\mu$ P Reset Circuits

## Pin Description

MAX6381-MAX6390

$\mu$ DFN	PIN						NAME	FUNCTION
	3-PIN SC70		4-PIN SC70					
	MAX6381/ MAX6383	MAX6382	MAX6384/ MAX6386/ MAX6390	MAX6385	MAX6387/ MAX689	MAX6388		
1 (MAX6382/ MAX6385/ MAX6388)		2	—	2	—	2	RESET	Active-High Push-Pull Reset Output. RESET changes from low to high when any monitored voltage ( $V_{CC}$ or $V_{RESETIN}$ ) drops below the reset threshold or $\overline{MR}$ is pulled low. RESET remains high for the reset timeout period after monitored voltages exceed the reset thresholds or $\overline{MR}$ is released.
1 (MAX6381/ MAX6383/ MAX6384/ MAX6386/ MAX6387/ MAX6390)	2	—	2	—	2	—	$\overline{RESET}$	Active-Low Open-Drain/Push-Pull Reset Output. $\overline{RESET}$ changes from high to low when any monitored voltage ( $V_{CC}$ or $V_{RESETIN}$ ) drops below the reset threshold or $\overline{MR}$ is pulled low. $\overline{RESET}$ remains low for the reset timeout period after the monitored voltages exceed the reset thresholds or $\overline{MR}$ is released. Open-drain requires an external pullup resistor.
2, 3, 5 (MAX6381/ MAX6382/ MAX6383)	—	—	—	—	—	—	N.C.	No Connection. Not Internally connected.
2, 5 (MAX6384- MAX6390)								
3 (MAX6384/ MAX6385/ MAX6386/ MAX6390)	—	—	3	3	—	—	$\overline{MR}$	Active-Low Manual Reset Input. Drive low to force a reset. Reset remains active as long as $\overline{MR}$ is low and for the reset timeout period after $\overline{MR}$ is released. Leave unconnected or connect to $V_{CC}$ if unused. $\overline{MR}$ has an internal $63k\Omega$ ( $1.56k\Omega$ for MAX6390) pullup resistor to $V_{CC}$ .
3 (MAX6387/ MAX6388/ MAX6389)	—	—	—	—	3	3	RESET IN	Auxiliary Reset Input. High-impedance input to the auxiliary reset comparator. Connect RESET IN to the center point of an external resistor voltage-divider network to set the reset threshold voltage. Reset asserts when either $V_{CC}$ or RESET IN falls below its threshold voltage.
4 (MAX6381- MAX6390)	3	3	4	4	4	4	$V_{CC}$	Supply Voltage for the device and input for fixed $V_{CC}$ reset threshold monitor.
6 (MAX6381- MAX6390)	1	1	1	1	1	1	GND	Ground

# SC70/ $\mu$ DFN, Single/Dual Low-Voltage, Low-Power $\mu$ P Reset Circuits

## Detailed Description

### RESET Output

A  $\mu$ P reset input starts the  $\mu$ P in a known state. These  $\mu$ P supervisory circuits assert reset to prevent code execution errors during power-up, power-down, or brownout conditions.

Reset asserts when  $V_{CC}$  is below the reset threshold; once  $V_{CC}$  exceeds the reset threshold, an internal timer keeps the reset output asserted for the reset timeout period. After this interval, reset output deasserts. Reset output is guaranteed to be in the correct logic state for  $V_{CC} \geq 1V$ .

### Manual Reset Input (MAX6384/MAX6385/MAX6386/MAX6390)

Many  $\mu$ P-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on  $\overline{MR}$  asserts reset. Reset remains asserted while  $\overline{MR}$  is low, and for the reset active timeout period ( $t_{RP}$ ) after  $\overline{MR}$  returns high. This input has an internal  $63k\Omega$  pullup resistor ( $1.56k\Omega$  for MAX6390), so it can be left unconnected if it is not used.  $\overline{MR}$  can be driven with TTL or CMOS logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from  $\overline{MR}$  to GND to create a manual-reset function; external debounce circuitry is not required. If  $\overline{MR}$  is driven from long cables or if the device is used in a noisy environment, connecting a  $0.1\mu F$  capacitor from  $\overline{MR}$  to GND provides additional noise immunity.

### RESET IN Comparator (MAX6387/MAX6388/MAX6389)

RESET IN is compared to an internal  $+1.27V$  reference. If the voltage at RESET IN is less than  $1.27V$ , reset asserts. Use the RESET IN comparator as a user-adjustable reset detector or as a secondary power-supply monitor by implementing a resistor-divider at RESET IN (shown in Figure 1). Reset asserts when either  $V_{CC}$  or RESET IN falls below its respective threshold voltage. Use the following equation to set the threshold:

$$V_{INTH} = V_{THRST} (R1/R2 + 1)$$

where  $V_{THRST} = +1.27V$ . To simplify the resistor selection, choose a value of  $R2$  and calculate  $R1$ :

$$R1 = R2 [(V_{INTH}/V_{THRST}) - 1]$$

Since the input current at RESET IN is  $50nA$  (max), large values can be used for  $R2$  with no significant loss in accuracy.

## Reset Thresholds (-40°C to +125°C)

SUFFIX	$V_{TH}$ (min)	$V_{TH}$ (nom)	$V_{TH}$ (max)
46	4.51	4.63	4.74
45	4.39	4.50	4.61
44	4.27	4.38	4.48
43	4.19	4.30	4.41
42	4.10	4.20	4.31
41	4.00	4.10	4.20
40	3.90	4.00	4.10
39	3.80	3.90	4.00
38	3.71	3.80	3.90
37	3.61	3.70	3.79
36	3.51	3.60	3.69
35	3.41	3.50	3.59
34	3.32	3.40	3.49
33	3.22	3.30	3.38
32	3.12	3.20	3.28
31	3.00	3.08	3.15
30	2.93	3.00	3.08
29	2.85	2.93	3.00
28	2.73	2.80	2.87
27	2.63	2.70	2.77
26	2.56	2.63	2.69
25	2.44	2.50	2.56
24	2.34	2.40	2.46
23	2.26	2.31	2.37
22	2.13	2.19	2.24
21	2.05	2.10	2.15
20	1.95	2.00	2.05
19	1.85	1.90	1.95
18	1.76	1.80	1.85
17	1.62	1.67	1.71
16	1.54	1.58	1.61

## Applications Information

### Negative-Going $V_{CC}$ Transients

In addition to issuing a reset to the  $\mu$ P during power-up, power-down, and brownout conditions, the MAX6381-MAX6390 are relatively immune to short duration negative-going  $V_{CC}$  transients (glitches).

The *Typical Operating Characteristics* section shows the Maximum Transient Durations vs. Reset Comparator Overdrive, for which the MAX6381-MAX6390 do not generate a reset pulse. This graph was generated using

# SC70/ $\mu$ DFN, Single/Dual Low-Voltage, Low-Power $\mu$ P Reset Circuits

MAX6381-MAX6390

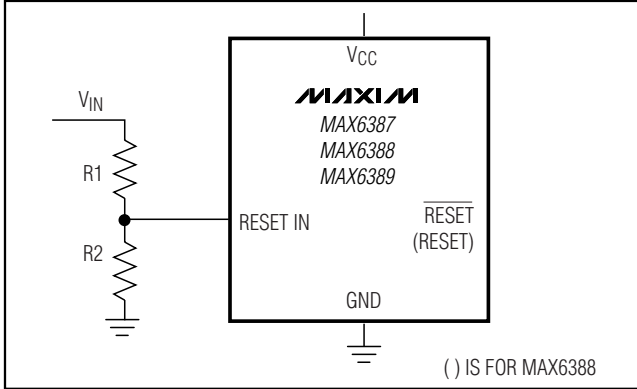


Figure 1. RESET IN Configuration

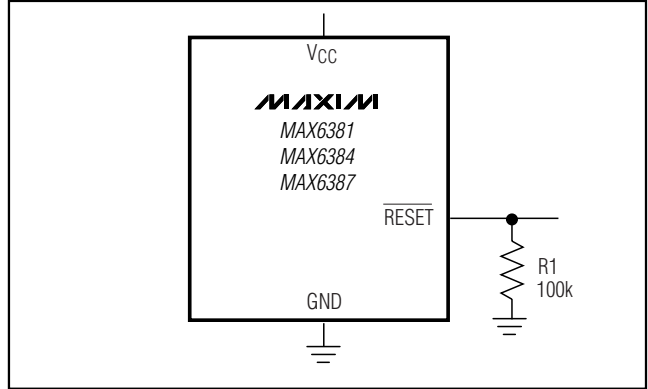


Figure 2. RESET Valid to  $V_{CC} = \text{Ground}$  Circuit

## Reset Timeout Delay

SUFFIX	MIN
D1	1ms
D2	20ms
D3	140ms
D5	280ms
D6	560ms
D4	1120ms
D7	1200ms
MAX6390_ _D4	1120/140ms*
MAX6390_ _D7	1200/150ms*

\*The MAX6390 has a 1120ms or 1200ms  $\overline{\text{RESET}}$  timeout and a 140ms or 150ms manual reset timeout.

a negative-going pulse applied to  $V_{CC}$ , starting above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the typical maximum pulse width a negative-going  $V_{CC}$  transient may have without causing a reset pulse to be issued. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. A 0.1 $\mu$ F capacitor mounted as close as possible to  $V_{CC}$  provides additional transient immunity.

### Ensuring a Valid RESET Output Down to $V_{CC} = 0V$

The MAX6381-MAX6390 are guaranteed to operate properly down to  $V_{CC} = 1V$ . In applications that require valid reset levels down to  $V_{CC} = 0V$ , a pulldown resistor to active-low outputs (push/pull only, Figure 2) and a pullup resistor to active-high outputs (push/pull only) will ensure that the reset line is valid while the reset output can no longer sink or source current. This scheme

does not work with the open-drain outputs of the MAX6383/MAX6386/MAX6389/MAX6390. The resistor value used is not critical, but it must be small enough not to load the reset output when  $V_{CC}$  is above the reset threshold. For most applications, 100k $\Omega$  is adequate.

## Standard Versions

PART	RESET THRESHOLD	RESET TIMEOUT
MAX638_	46	D3
	44	
	31	
	29	
	26	
	23	
	22	
	17	
MAX6390	46	D4
	44	
	31	
	29	
	26	
	23	
	22	
	17	
	16	

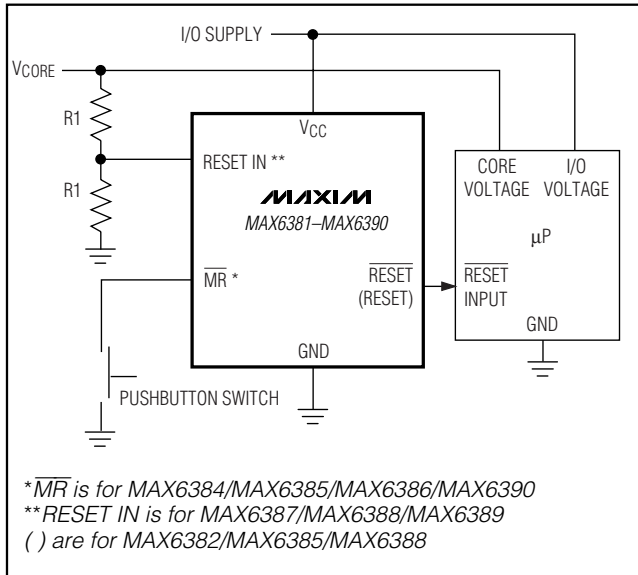
# SC70/ $\mu$ DFN, Single/Dual Low-Voltage, Low-Power $\mu$ P Reset Circuits

## Selector Guide

PART NUMBER	PUSH-PULL ACTIVE-LOW	PUSH-PULL ACTIVE-HIGH	OPEN-DRAIN ACTIVE-LOW	MANUAL RESET INPUT MR	RESET IN
MAX6381	X				
MAX6382		X			
MAX6383			X		
MAX6384	X			X	
MAX6385		X		X	
MAX6386			X	X	
MAX6390*			X	X	
MAX6387	X				X
MAX6388		X			X
MAX6389			X		X

\*The MAX6390 offers a  $V_{CC}$  reset timeout of 1120ms or 1200ms (min) and a manual reset timeout of 140ms or 150ms (min).

### Typical Operating Circuit



### Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX6383LT__D_+T	-40°C to +125°C	6 $\mu$ DFN-6	L611-1
MAX6383XR__D_+T	-40°C to +125°C	3 SC70-3	X3-2
MAX6384LT__D_+T	-40°C to +125°C	6 $\mu$ DFN-6	L611-1
MAX6384XS__D_+T	-40°C to +125°C	4 SC70-4	X4-1
MAX6385LT__D_+T	-40°C to +125°C	6 $\mu$ DFN-6	L611-1
MAX6385XS__D_+T	-40°C to +125°C	4 SC70-4	X4-1
MAX6386LT__D_+T	-40°C to +125°C	6 $\mu$ DFN-6	L611-1
MAX6386XS__D_+T	-40°C to +125°C	4 SC70-4	X4-1
MAX6387LT__D_+T	-40°C to +125°C	6 $\mu$ DFN-6	L611-1
MAX6387XS__D_+T	-40°C to +125°C	4 SC70-4	X4-1
MAX6388LT__D_+T	-40°C to +125°C	6 $\mu$ DFN-6	L611-1
MAX6388XS__D_+T	-40°C to +125°C	4 SC70-4	X4-1
MAX6389LT__D_+T	-40°C to +125°C	6 $\mu$ DFN-6	L611-1
MAX6389XS__D_+T	-40°C to +125°C	4 SC70-4	X4-1
MAX6390LT__D_+T	-40°C to +125°C	6 $\mu$ DFN-6	L611-1
MAX6390XS__D_+T*	-40°C to +125°C	4 SC70-4	X4-1

**Note:** Insert reset threshold suffix (see Reset Threshold table) after "XR", "XS", or "LT." Insert reset timeout delay (see Reset Timeout Delay table) after "D" to complete the part number. Sample stock is generally held on standard versions only (see Standard Versions table). Standard versions have an order increment requirement of 2500 pieces. Nonstandard versions have an order increment requirement of 10,000 pieces. Contact factory for availability of nonstandard versions.

\*MAX6390 is available with D4 or D7 timing only.

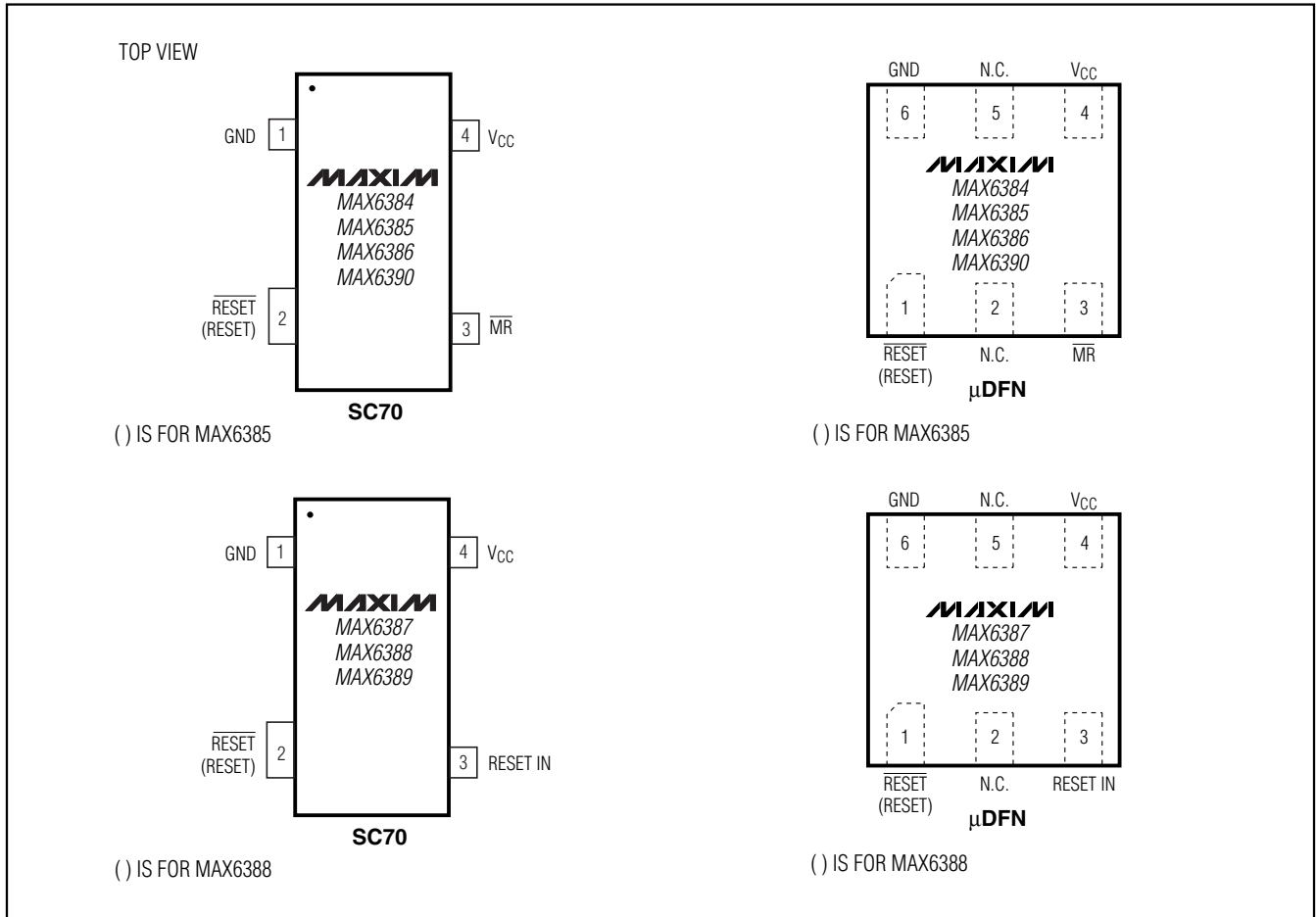
+Denotes a lead-free package.



# SC70/ $\mu$ DFN, Single/Dual Low-Voltage, Low-Power $\mu$ P Reset Circuits

## Pin Configurations (continued)

MAX6381-MAX6390



## Chip Information

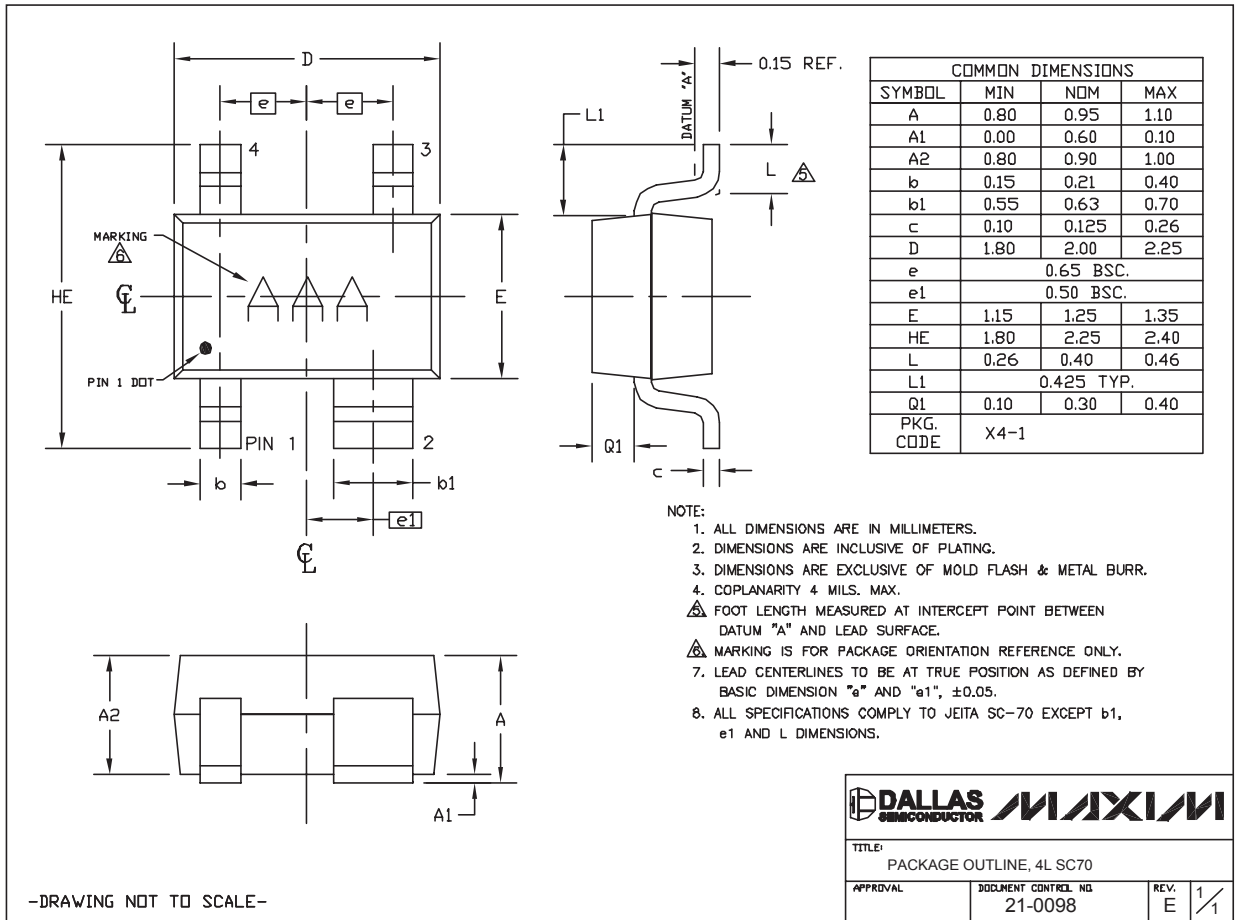
TRANSISTOR COUNT: 647

PROCESS: BiCMOS

# SC70/ $\mu$ DFN, Single/Dual Low-Voltage, Low-Power $\mu$ P Reset Circuits

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



SC70, 4L-EPS

**DALLAS SEMICONDUCTOR** **MAXIM**

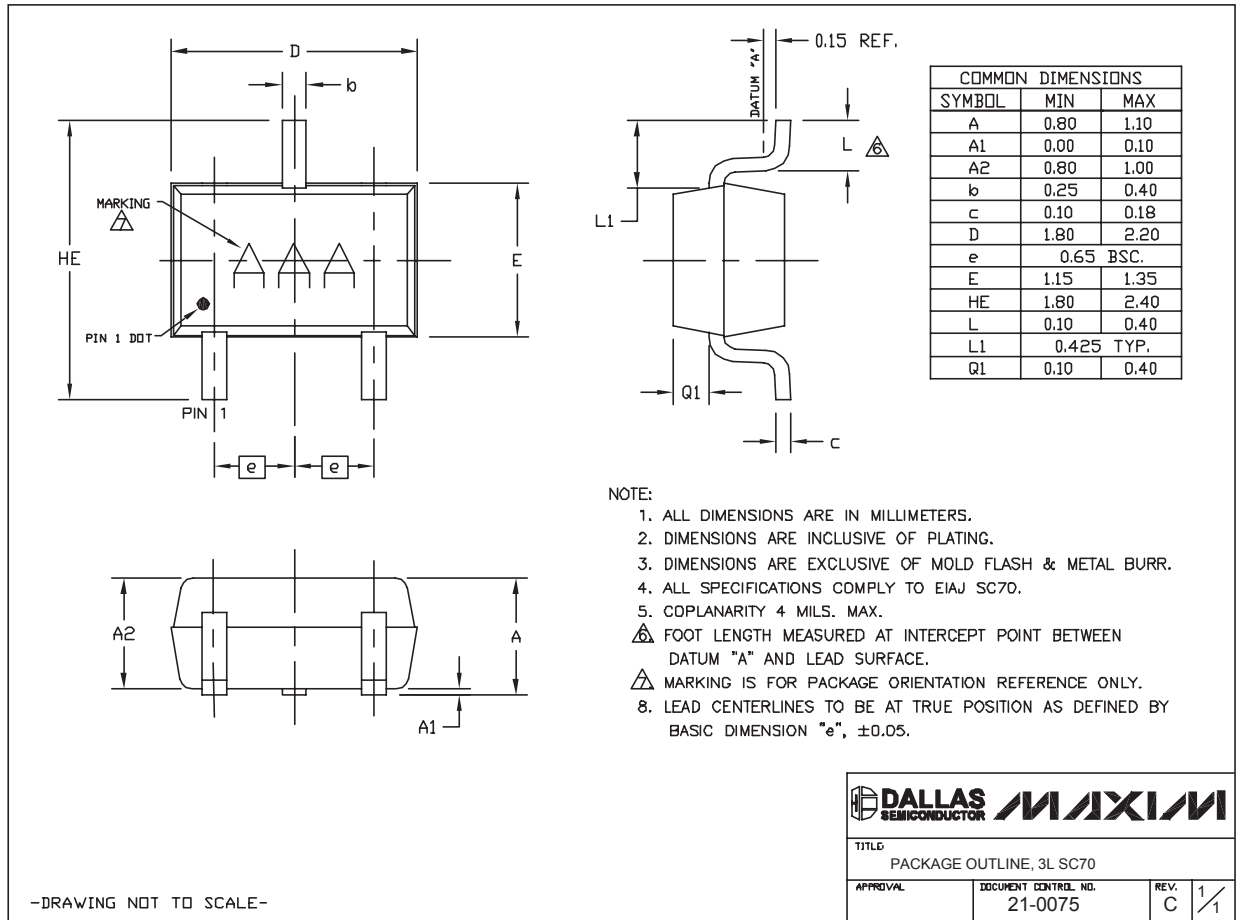
TITLE:  
PACKAGE OUTLINE, 4L SC70

APPROVAL	DOCUMENT CONTROL NO. 21-0098	REV. E	1/1
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# SC70/ $\mu$ DFN, Single/Dual Low-Voltage, Low-Power $\mu$ P Reset Circuits

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



SC70, 3LEPS

MAX6381-MAX6390

-DRAWING NOT TO SCALE-

**DALLAS SEMICONDUCTOR** **MAXIM**

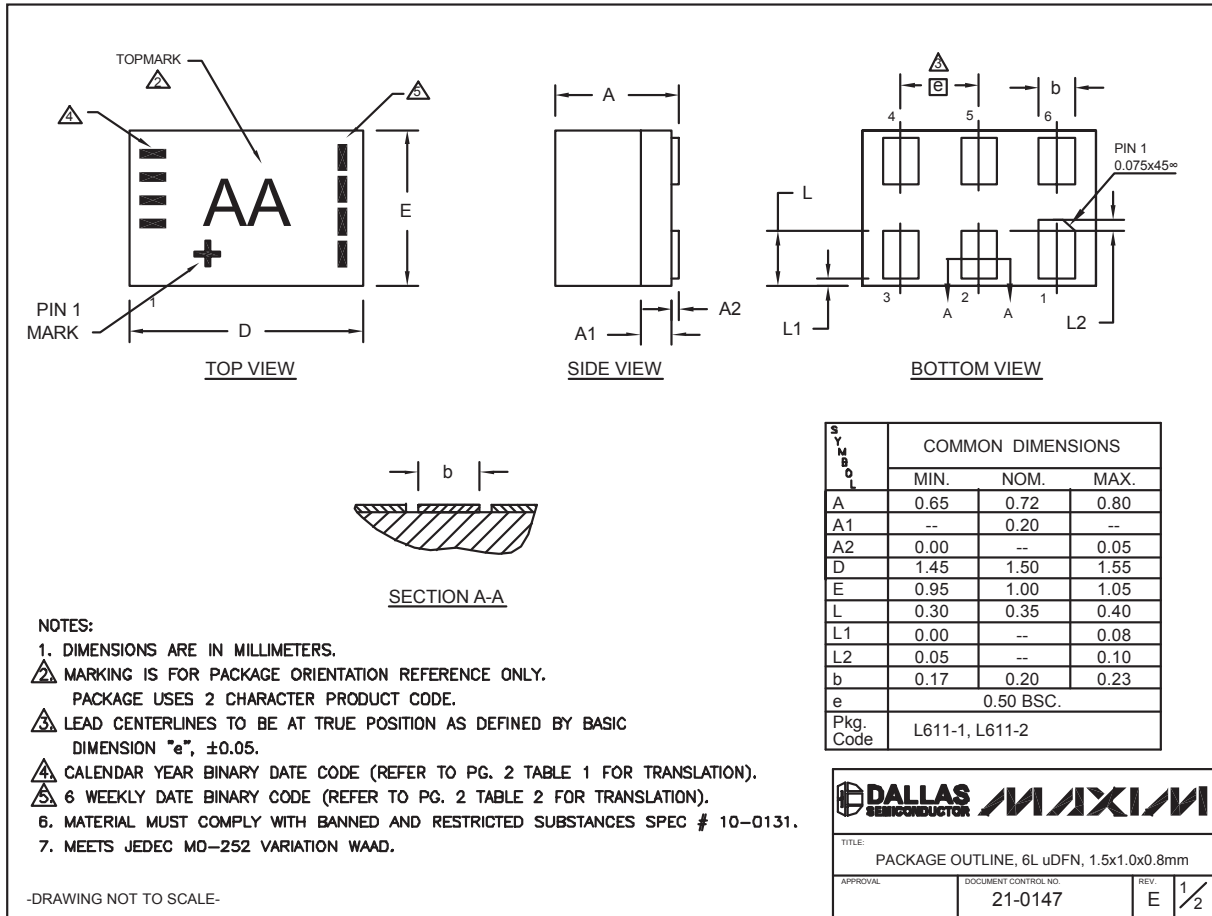
TITLE: PACKAGE OUTLINE, 3L SC70

APPROVAL	DOCUMENT CONTROL NO. 21-0075	REV. C	1/1
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# SC70/ $\mu$ DFN, Single/Dual Low-Voltage, Low-Power $\mu$ P Reset Circuits

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



**DALLAS** SEMICONDUCTOR **MAXIM**

TITLE: PACKAGE OUTLINE, 6L uDFN, 1.5x1.0x0.8mm

APPROVAL	DOCUMENT CONTROL NO. 21-0147	REV. E	1/2
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# SC70/ $\mu$ DFN, Single/Dual Low-Voltage, Low-Power $\mu$ P Reset Circuits

MAX6381-MAX6390

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

TABLE 1 Translation Table for Calendar Year Code										
Calendar Year	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014

Legend: Marked with bar    Blank space - no bar required

TABLE 2 Translation Table for Payweek Binary Coding									
Payweek	06-11	12-17	18-23	24-29	30-35	36-41	42-47	48-51	52-05

Legend: Marked with bar    Blank space - no bar required

TITLE: PACKAGE OUTLINE, 6L $\mu$ DFN, 1.5x1.0x0.8mm		
APPROVAL	DOCUMENT CONTROL NO. 21-0147	REV. E 2/2

-DRAWING NOT TO SCALE-

## Revision History

Pages changed at Rev 4: Title on all pages, 1, 2, 5, 7-13

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