

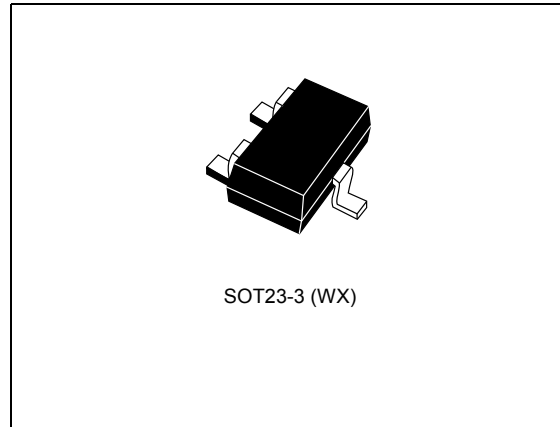


STM1810 STM1811 STM1812 STM1813 STM1815 STM1816 STM1817 STM1818

Low power reset circuit

Features

- Precision monitoring of 3 V, 3.3 V, and 5 V supply voltages
- Four output configurations:
 - Push-pull, active-high (STM1812,1817)
 - Push-pull, active-low (STM1810,1815)
 - Open-drain, active-low (STM1811,1816)
 - Open-drain, active-low with push-button detect (STM1813,1818)
- Reset pulse width - 100 ms (min.)
- Low supply current - 4 μ A (typ.)
- Guaranteed assertion down to $V_{CC} = 1.0$ V (0 °C to 105 °C)
- Factory-trimmed reset thresholds of 2.55 V, 2.88 V, 3.06 V, 4.37 V, and 4.62 V (typ.)
- Power supply transient immunity
- Push-button/manual reset detect (STM1813/1818)
- Operating temperature: -40 °C to 105 °C



- $\pm 2.5\%$ reset threshold accuracy: (-40 °C to 105 °C)
- Available in the SOT23-3 package
- Fully compatible with DS181x and MXD181x products.

Table 1. Device summary

Order codes	5 V	3.3 V/ 3.0 V	Active-low reset (push-pull)	Active-low reset (open-drain)	Active-high reset (push-pull)	Active-low reset (open-drain, bidirectional, with \overline{MR} detect)
STM1810L/M	✓		✓			
STM1811L/M	✓			✓ ⁽¹⁾		
STM1812L/M	✓				✓	
STM1813L/M	✓					✓
STM1815T/S/R		✓	✓			
STM1816T/S/R		✓		✓ ⁽¹⁾		
STM1817T/S/R		✓			✓	
STM1818T/S/R		✓				✓

1. Active-low RST with internal pull-up resistor.

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1 Description

STM181x devices are low power reset devices used to monitor power supplies for microcontrollers. They perform a single function: asserting a reset signal whenever V_{CC} supply voltage drops below a preset value and keeping it asserted until V_{CC} has risen above the preset threshold for a minimum period of time (t_{rec}). They provide excellent circuit reliability without additional external components when used with +3.0 V / +3.3 V (STM1815–STM1818), and +5 V (STM1810–STM1813) power supply systems.

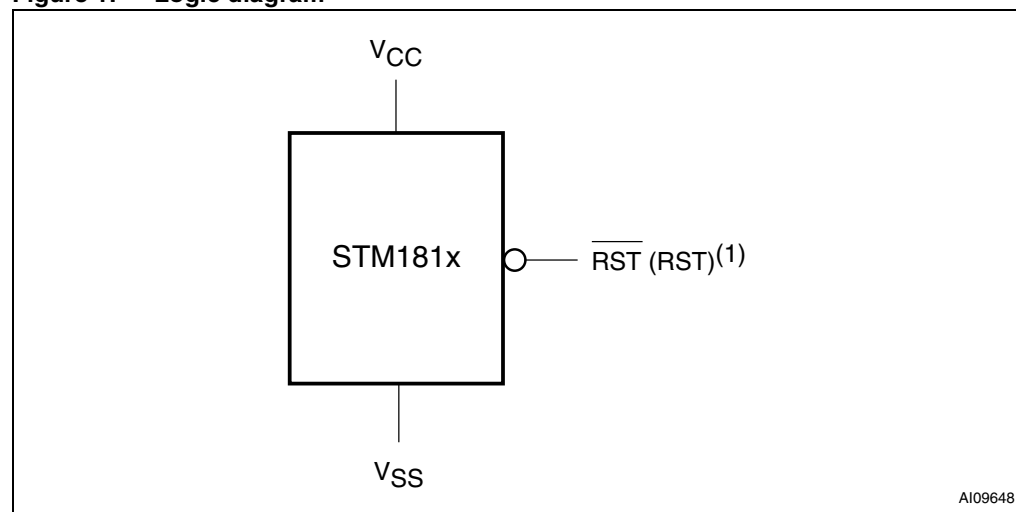
A precision voltage reference and comparator monitors the V_{CC} input for an out-of-tolerance condition. When an invalid V_{CC} condition occurs, the reset output (\overline{RST}) is forced low (or high in the case of RST) and remains asserted for t_{rec} after V_{CC} rises above the reset threshold. The STM1813/1818 also keep reset asserted for t_{rec} after the output is momentarily pulled to ground by an external push-button switch.

The STM1812 and STM1817 have an active-high, push-pull output. The STM1810 and STM1815 (push-pull) and STM1811, STM1813, STM1816, and STM1818 (open-drain) have an active-low \overline{RST} output. The open-drain devices (STM1811 / STM1813 / STM1816 / STM1818) also have an internal pull-up resistor to V_{CC} . The STM1813 and STM1818 feature a debounced manual reset feature that asserts a reset if the \overline{RST} pin is pulled low for more than 1.5 μ s. When used to initiate manual reset, \overline{RST} debounces signals from devices such as mechanical switches. For devices with this feature, the release of the external switch triggers the reset period.

The STM181x devices are guaranteed to output the correct logic state for V_{CC} down to 1.0 V (0 °C to +105 °C). They also provide a reset comparator designed to ignore fast transients on V_{CC} .

Reset thresholds are available between +2.55 V and +4.62 V. These small, low power devices are ideal for use in portable equipment. All are available in the space-saving 3-pin SOT23 package, and are specified from –40 °C to +105 °C.

Figure 1. Logic diagram

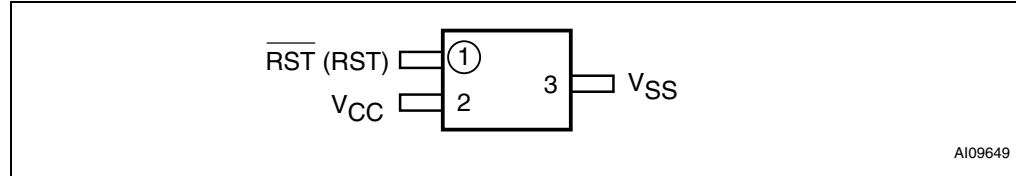


1. For STM1812, STM1817.

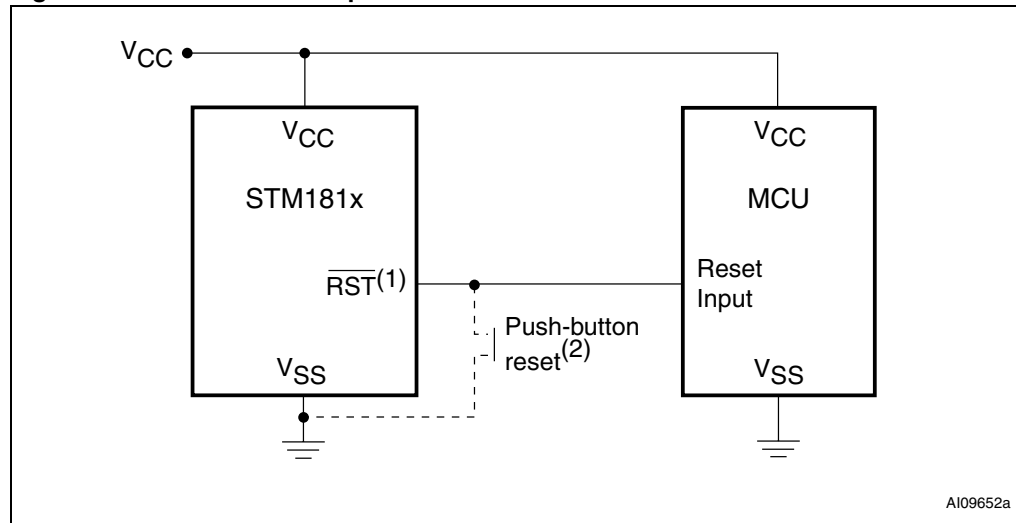
Table 2. Signal names

Symbol	Description
V_{SS}	Ground
RST	Active-low reset output
RST ⁽¹⁾	Active-high reset output
V_{CC}	Supply voltage and input for reset threshold monitor

1. For STM1812, STM1817.

Figure 2. SOT23-3 connections

2. RST for STM1812 and STM1817.

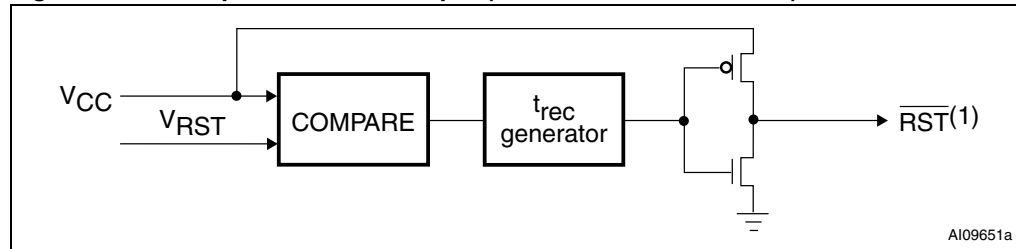
Figure 3. Hardware hookup

1. RST for STM1812 and STM1817 (see [Table 1](#)).

2. Only valid for STM1813 and STM1818.

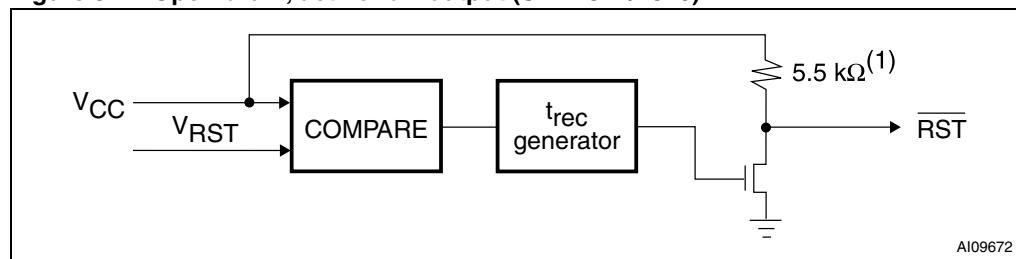
1.1 Functional block diagrams

Figure 4. Push-pull active-low output (STM1810/1812/1815/1817)



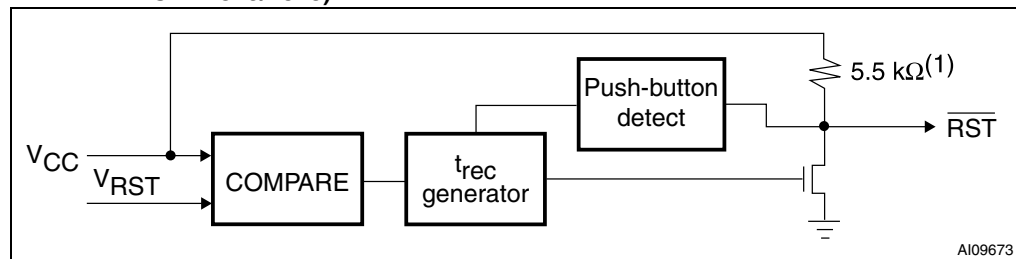
1. RST for STM1812 and STM1817.

Figure 5. Open-drain, active-low output (STM1811/1816)



1. 5.5 kΩ internal pull-up resistor.

Figure 6. Open-drain, active-low output (bidirectional, manual reset detect, STM1813/1818)



1. 5.5 kΩ internal pull-up resistor.

1.2 Pin descriptions

See [Figure 1](#) and [Table 2](#) for a brief overview of the signals connected to this device.

1.2.1 Active-low $\overline{\text{RST}}$ output (push-pull)

Pulses low when V_{CC} drops below V_{RST} , and stays low as long as V_{CC} is below the reset threshold. It remains low for t_{rec} after V_{CC} rises above the reset threshold.

1.2.2 Active-low $\overline{\text{RST}}$ output (open-drain)

Pulses low when V_{CC} drops below V_{RST} , and stays low as long as V_{CC} is below the reset threshold. It remains low for t_{rec} after V_{CC} rises above the reset threshold. $\overline{\text{RST}}$ output has an internal 5.5 kΩ pull-up resistor.

1.2.3 Active-high RST output (push-pull)

Pulses high when V_{CC} drops below V_{RST} , and stays high as long as V_{CC} is below the reset threshold. It remains high for t_{rec} after V_{CC} rises above the reset threshold.

1.2.4 Active-low \overline{RST} output (open-drain with internal 5.5 k Ω pull-up) with manual reset detect

Pulses low when V_{CC} drops below V_{RST} , or \overline{RST} is externally pulled low for at least 1.5 μ s. It remains low for t_{PBRST} after V_{CC} rises above the reset threshold, or after the external manual reset is released (see [Figure 9](#)). \overline{RST} output has an internal 5.5 k Ω pull-up resistor.

1.2.5 V_{CC}

Supply voltage and input for V_{RST} comparator.

1.2.6 V_{SS}

Ground, is the reference for the power supply. It must be connected to the system ground.

Table 3. STM1810/STM1815

Pin	Name	Function
1	\overline{RST}	Active-low reset output (push-pull)
2	V_{CC}	Supply voltage and input for reset threshold monitor
3	V_{SS}	Ground

Table 4. STM1811/STM1816

Pin	Name	Function
1	\overline{RST}	Active-low reset output (open-drain, with internal 5.5 k Ω pull-up resistor)
2	V_{CC}	Supply voltage and input for reset threshold monitor
3	V_{SS}	Ground

Table 5. STM1812/STM1817

Pin	Name	Function
1	RST	Active-high reset output (push-pull)
2	V_{CC}	Supply voltage and input for reset threshold monitor
3	V_{SS}	Ground

Table 6. STM1813/STM1818

Pin	Name	Function
1	\overline{RST}	Active-low reset output (open-drain, with internal 5.5 k Ω pull-up) with push-button/manual reset detect
2	V_{CC}	Supply voltage and input for reset threshold monitor
3	V_{SS}	Ground

2 Operation

2.1 Reset output

The STM181x asserts a reset signal to the microcontroller (MCU) whenever V_{CC} goes below the reset threshold (V_{RST}), and is guaranteed valid down to $V_{CC} = 1.0\text{ V}$ ($0\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$). A microcontroller's (MCU) reset input starts the MCU in a known state. The STM1810 - STM1813/ STM1815 - STM1818 low power reset circuits assert reset to prevent code-execution errors during power-up, power-down, and brownout conditions ([Figure 7](#)).

During power-up, once V_{CC} exceeds the reset threshold an internal timer keeps \overline{RST} low for the reset time-out period, t_{rec} . After this interval, \overline{RST} returns high.

If V_{CC} drops below the reset threshold, \overline{RST} goes low. Each time \overline{RST} is asserted, it stays low for at least the reset time-out period. Any time V_{CC} goes below the reset threshold, the internal timer clears. The reset timer starts when V_{CC} returns above the reset threshold. Reset t_{rec} is also triggered by an externally initiated rising edge on the \overline{RST} pin (STM1813/STM1818), following a low signal of $1.5\text{ }\mu\text{s}$ minimum duration.

2.2 Push-button detect reset (STM1813/1818)

Many systems require push-button reset capability ([Figure 8](#)), allowing the user or external logic circuitry to initiate reset. On the STM1813/STM1818, a logic low on \overline{RST} held for greater than $1.5\text{ }\mu\text{s}$ asserts a reset. \overline{RST} deasserts following a 100 ms minimum reset time-out delay (t_{rec}). A manual reset input shorter than $1.5\text{ }\mu\text{s}$ may release \overline{RST} without the 100 ms minimum reset time-out delay. To facilitate use with mechanical switches, the STM1813/STM1818 contain internal debounce circuitry. A debounced waveform is shown in [Figure 9](#). The \overline{RST} output has an internal $5.5\text{ k}\Omega$ pull-up resistor.

2.3 Interfacing to bidirectional microcontrollers (MCU's)

As the \overline{RST} output on the STM1811/STM1816 is open-drain, these devices interface easily with MCU's that have bidirectional reset pins. Connecting the μP supervisor's reset (\overline{RST}) output directly to the microcontroller's reset (\overline{RST}) pin allows either device to assert reset ([Figure 10](#)). No external pull-up resistor is required, as it is within the STM1811/STM1816.

2.4 Negative going V_{CC} transients

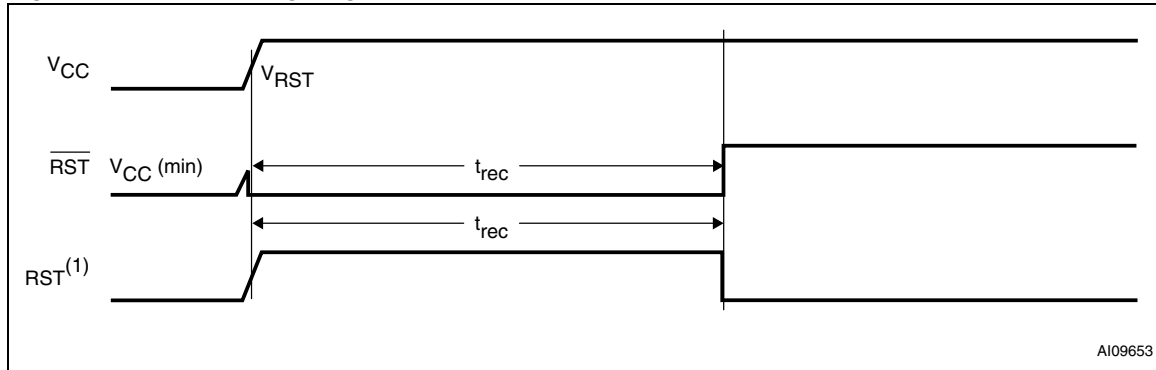
The STM181x are relatively immune to negative-going V_{CC} transients (glitches). [Figure 19](#) shows typical transient duration versus reset comparator overdrive (for which the STM181x will NOT generate a reset pulse). The graph was generated using a negative pulse applied to V_{CC} , starting at 0.5 V above the actual reset threshold and ending below it by the magnitude indicated (comparator overdrive). The graph indicates the maximum pulse width a negative V_{CC} transient can have without causing a reset pulse. As the magnitude of the transient increases (further below the threshold), the maximum allowable pulse width decreases. Any combination of duration and overdrive which lies under the curve will NOT generate a reset signal. Typically, a V_{CC} transient that goes 100 mV below the reset threshold and lasts $20\text{ }\mu\text{s}$ or less will not cause a reset pulse. A $0.1\text{ }\mu\text{F}$ bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity.

2.5 Valid $\overline{\text{RST}}$ output down to $V_{\text{CC}} = 0 \text{ V}$

When V_{CC} falls below 1 V, the $\overline{\text{RST}}$ output no longer sinks current, but becomes an open circuit. In most systems this is not a problem, as most MCUs do not operate below 1 V. However, in applications where $\overline{\text{RST}}$ output must be valid down to 0 V, a pull-down resistor may be added to hold the $\overline{\text{RST}}$ output low (see [Figure 11](#)). This resistor must be large enough to not load the $\overline{\text{RST}}$ output, and still be small enough to pull the output to ground. A 100 k Ω resistor is recommended.

Note: The same situation applies for the active-high RST of the STM1810/1812. A 100 k Ω pull-up resistor to V_{CC} should be used if RST must remain valid for $V_{\text{CC}} < 1.0 \text{ V}$.

Figure 7. Reset timing diagram



1. RST for STM1812 and STM1817.

Figure 8. Push-button manual reset with $\overline{\text{MR}}$ detect (STM1813/1818)

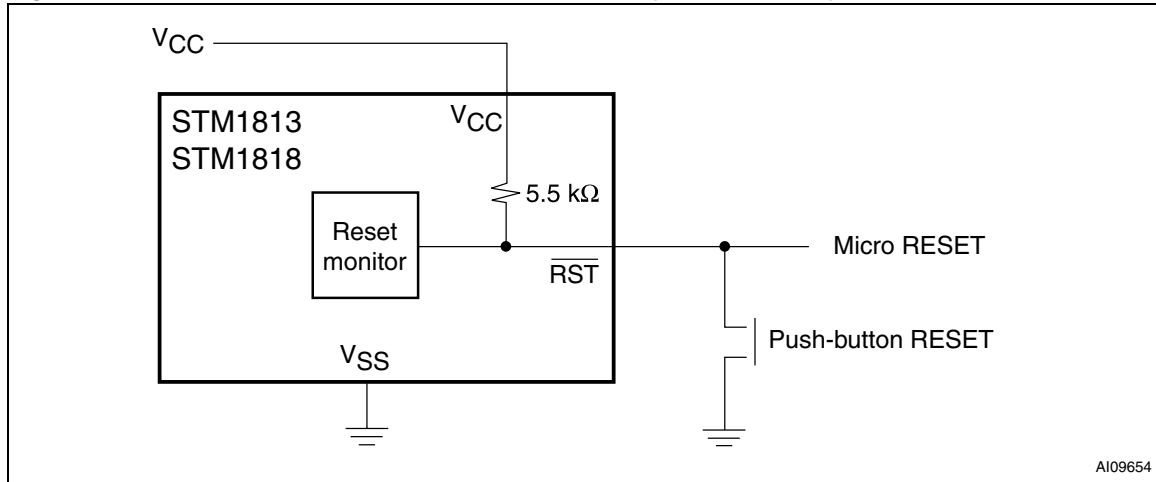
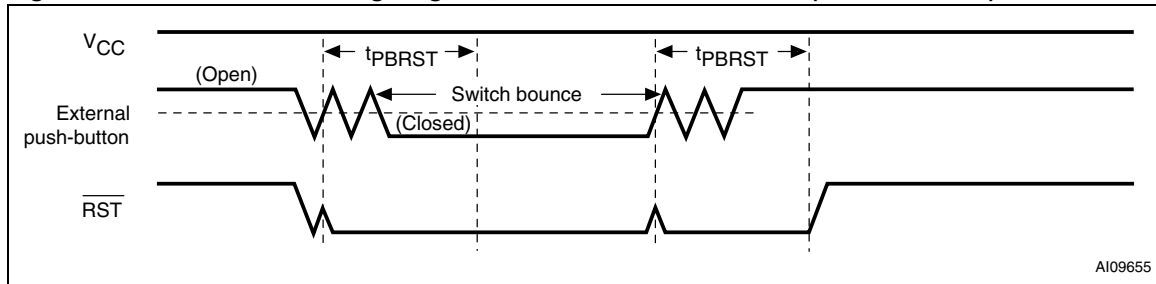
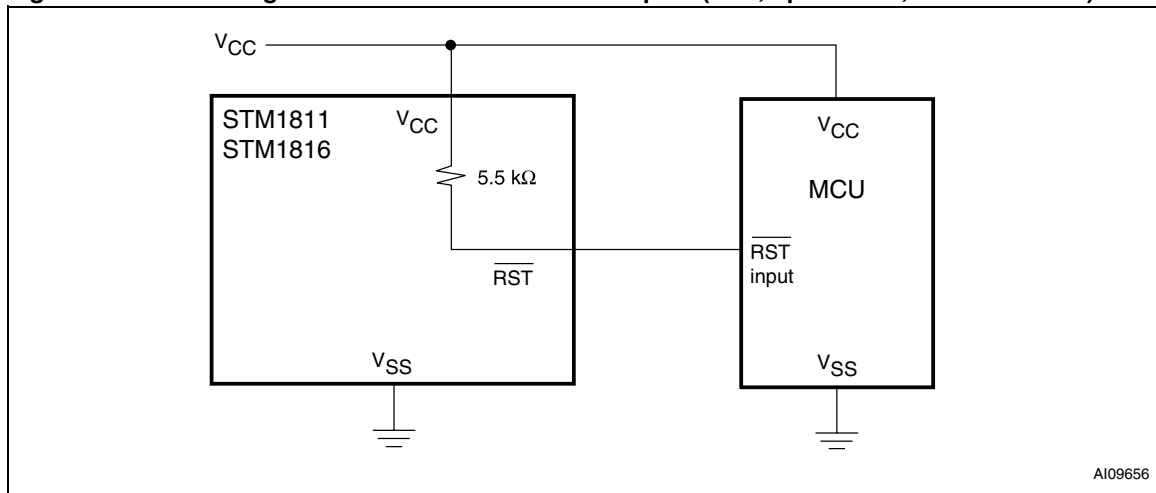


Figure 9. Manual reset timing diagram, switch bounce/debounce (STM1813/1818)



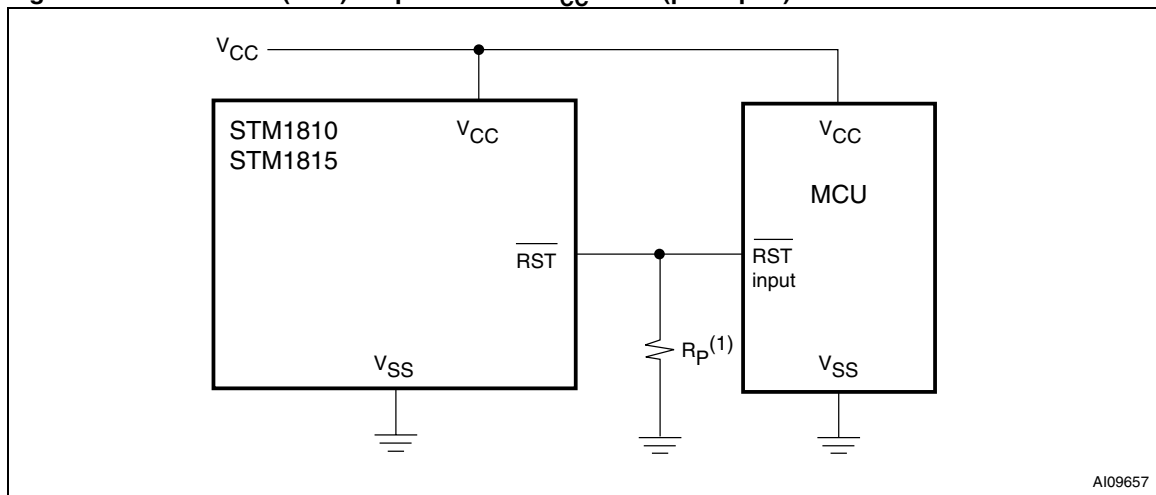
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Figure 10. Interfacing MCUs with bidirectional reset pins (\overline{RST} , open-drain, STM1811/1816)



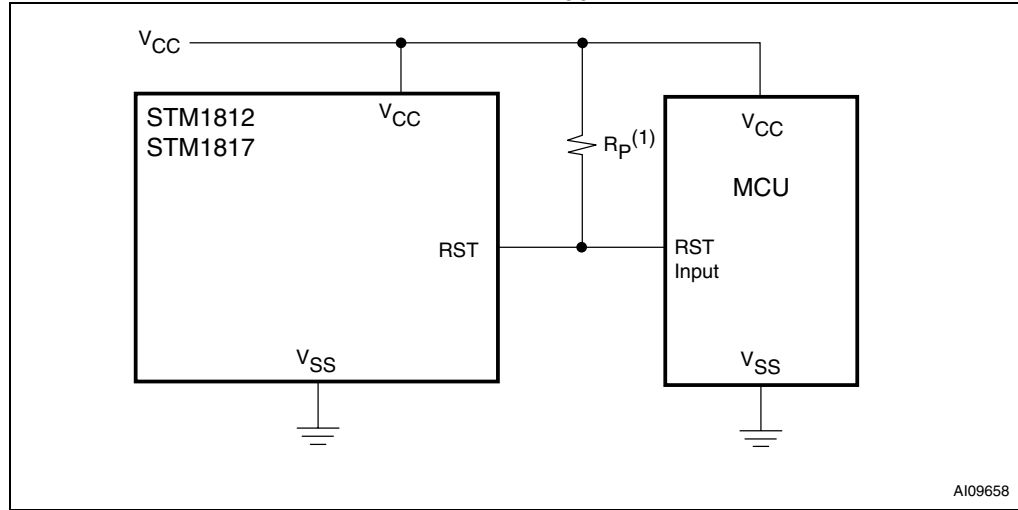
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Figure 11. Valid reset (\overline{RST}) output down to $V_{CC} = 0\text{ V}$ (push-pull)



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1. $\sim 100\text{ k}\Omega$ resistor recommended.

Figure 12. Valid reset (RST) output down to $V_{CC} = 0$ V (push-pull)

1. ~100 k Ω resistor recommended.

3 Typical operating characteristics

Typical values are at $T_A = 25\text{ }^\circ\text{C}$.

Figure 13. Supply current vs. temperature (no load)

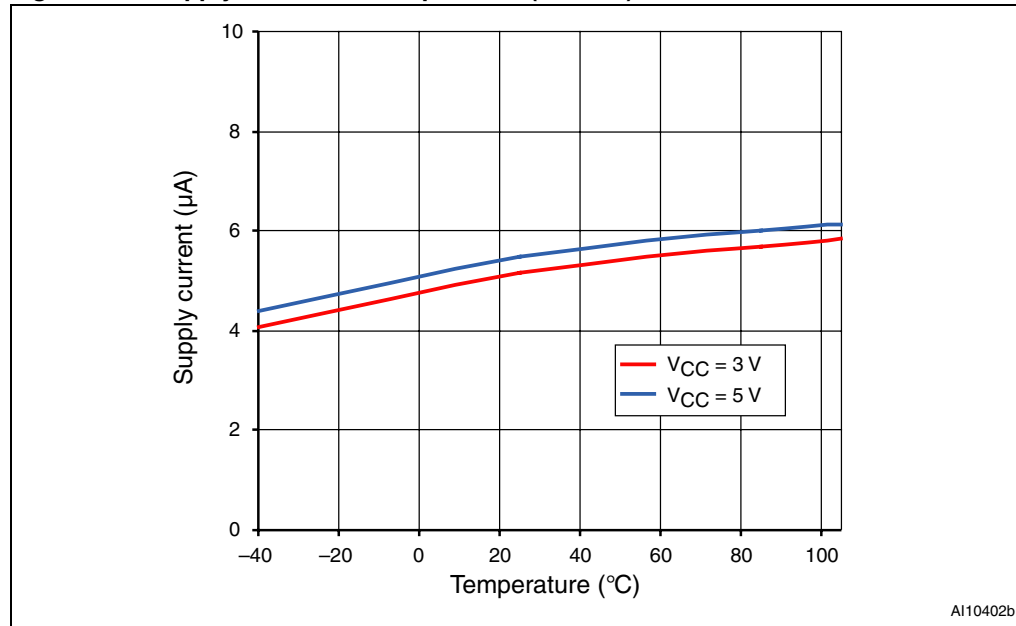


Figure 14. Normalized reset time-out period (t_{rec}) vs. temperature
 $- V_{OD} = V_{TH} - V_{CC}$

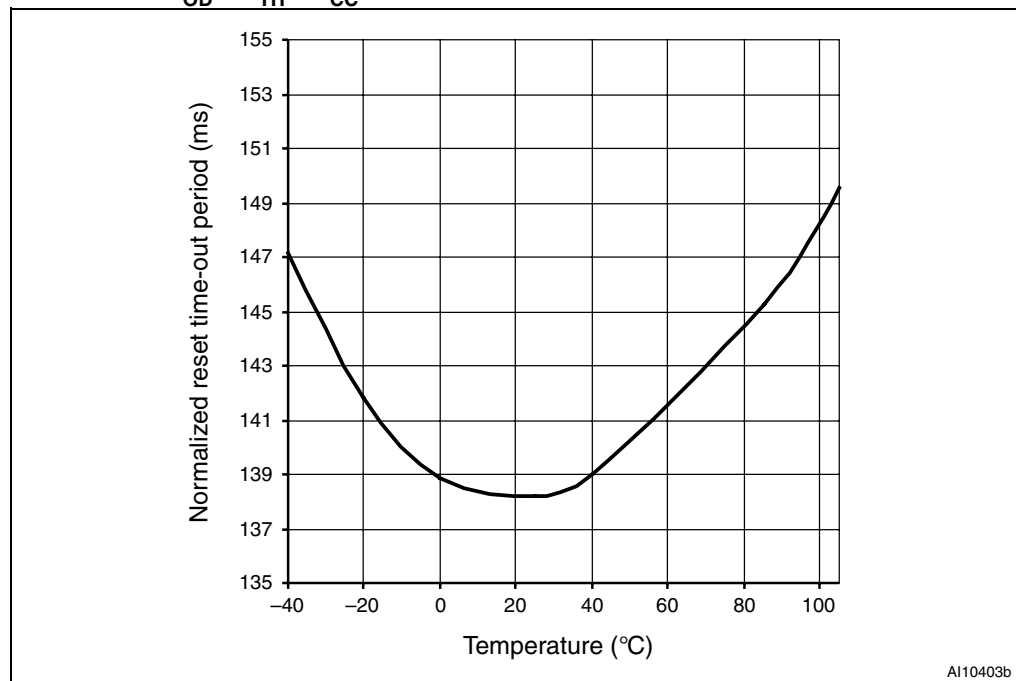


Figure 15. V_{CC} -to-reset output delay vs. temperature - $V_{OD} = V_{TH} - V_{CC}$

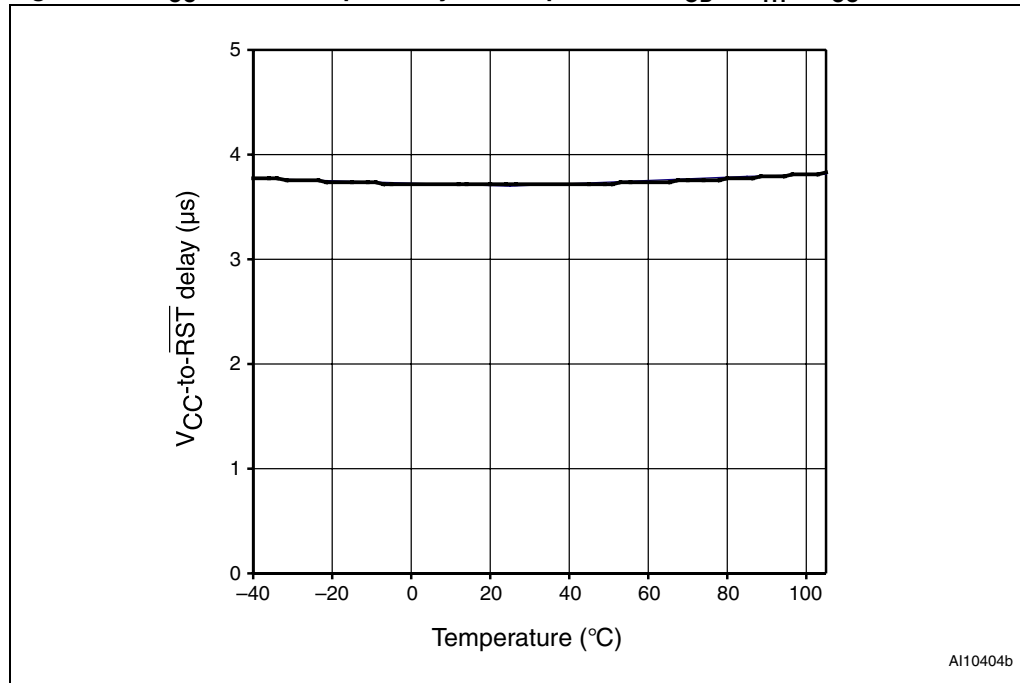


Figure 16. Voltage output low vs. I_{SINK}

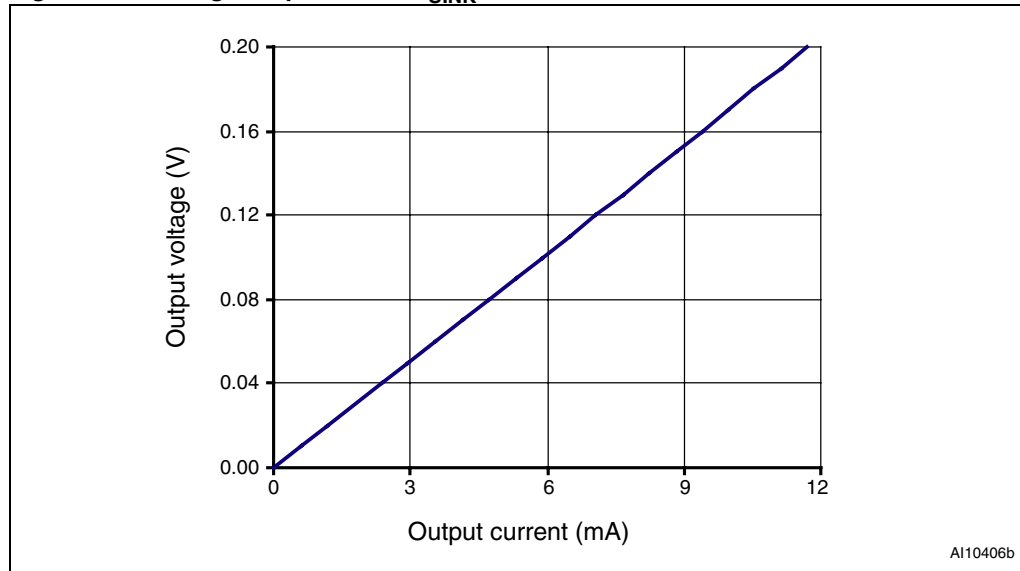


Figure 17. Voltage output high vs. I_{SOURCE}

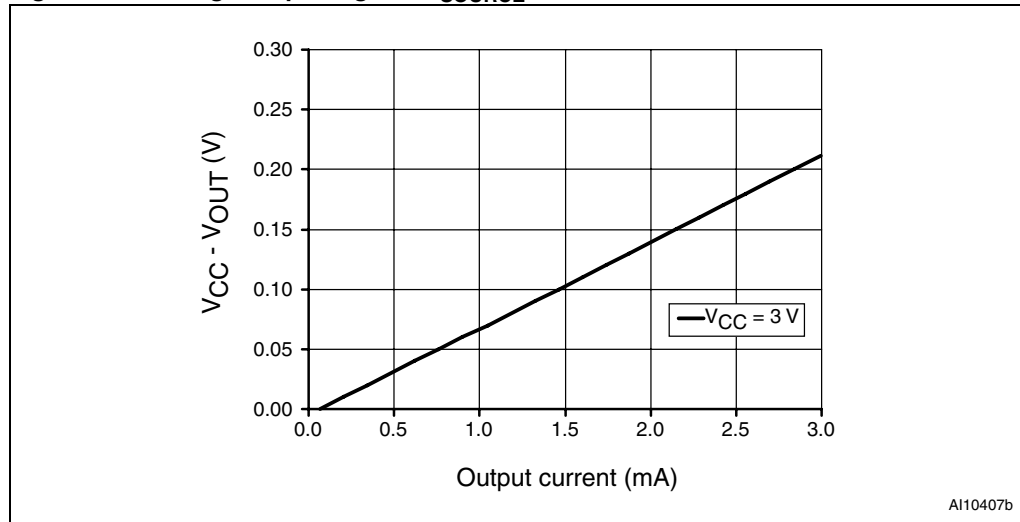
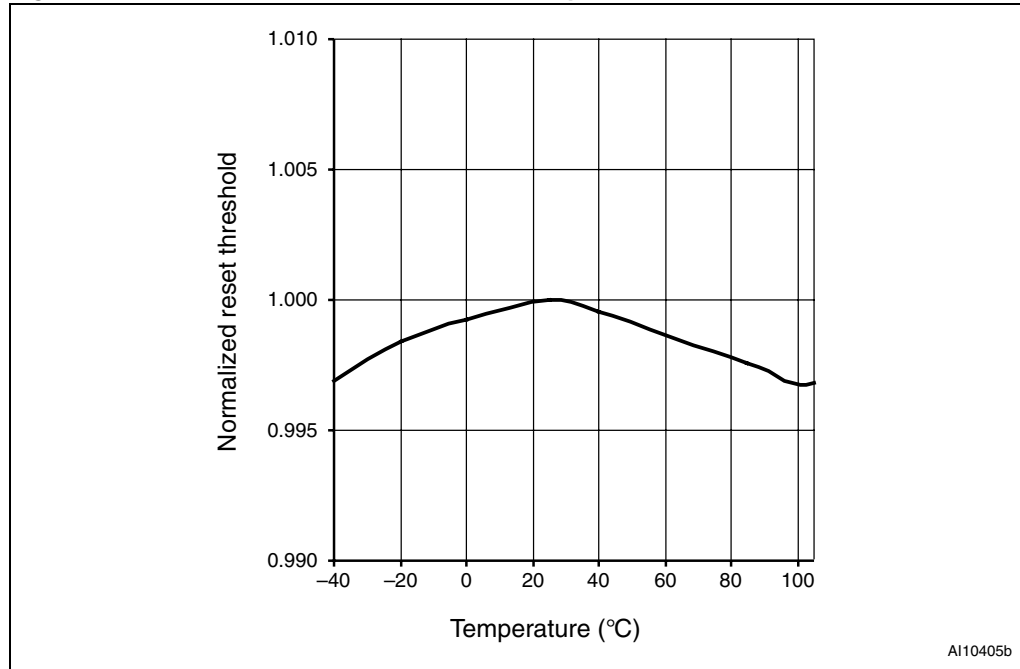
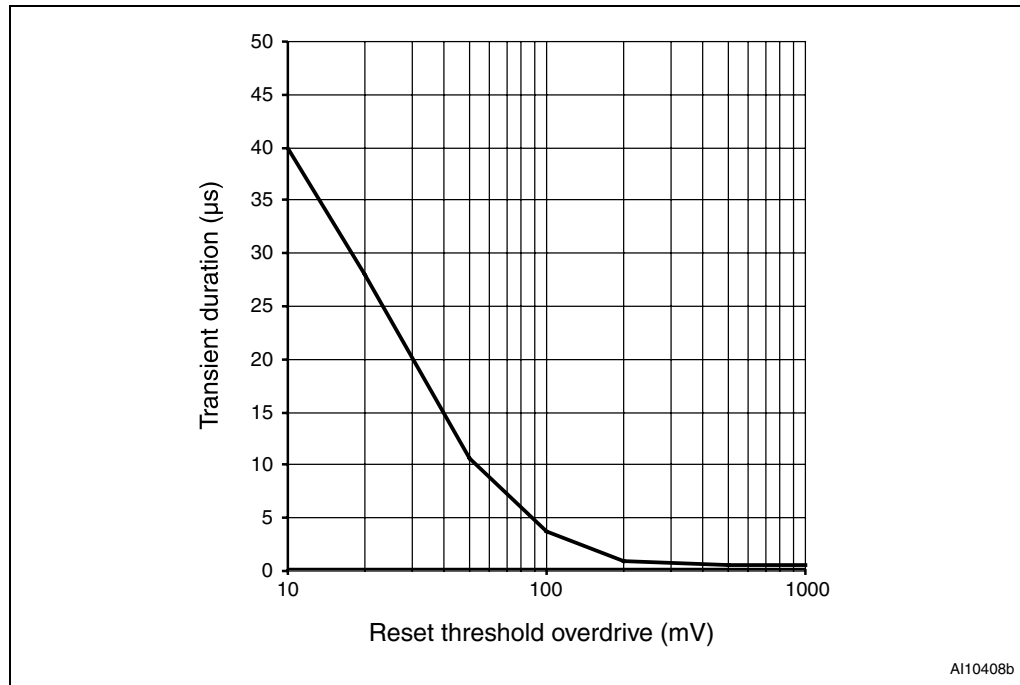


Figure 18. Normalized reset threshold vs. temperature



**Figure 19. Max. transient duration NOT causing reset pulse vs. reset threshold
overdrive**



1. Reset occurs above the line.

4 Maximum rating

Stressing the device above the rating listed in [Table 7](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the “Operating” sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics™ “SURE Program” and other relevant quality documents.

Table 7. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T _{STG}	Storage temperature (V _{CC} Off)	-55 to 150	°C
T _{SLD} ⁽¹⁾	Lead solder temperature for 10 seconds	260	°C
V _{IO}	Input or output voltage	-0.3 to V _{CC} +0.3	V
V _{CC}	Supply voltage	-0.3 to 7.0	V
I _O	Output current	20	mA
P _D	Power dissipation	320	mW

1. Reflow at peak temperature of 255 °C to 260 °C for < 30 seconds (total thermal budget not to exceed 180 °C for between 90 to 150 seconds).

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in [Table 8](#). Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 8. Operating and AC measurement conditions

Parameter	STM1810 - 1818	Unit
V_{CC} supply voltage	1.0 to 5.5	V
Ambient operating temperature (T_A)	-40 to 105	°C
Input rise and fall times	≤ 5	ns
Input pulse voltages	0.2 to 0.8 V_{CC}	V
Input and output timing ref. voltages	0.3 to 0.7 V_{CC}	V

Figure 20. AC testing input/output waveforms

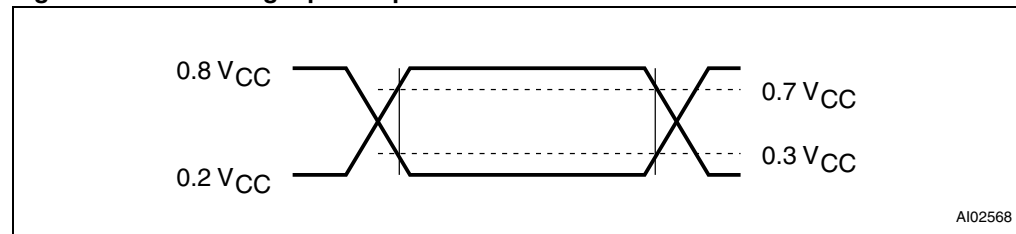


Table 9. DC and AC characteristics

Sym.	Alternative	Description	Test condition ⁽¹⁾	Min.	Typ.	Max.	Unit
V _{CC}		Operating voltage	T _A = 0 to +105 °C	1.0		5.5	V
			T _A = -40 to +105 °C	1.2		5.5	V
I _{CC}		V _{CC} supply current	V _{CC} = 3.6 V, no load		4	10	μA
			V _{CC} = 5.5 V, no load		9	16	μA
V _{IH}		Input high voltage	STM1813/1818 only	0.7 V _{CC}			V
V _{IL}		Input low voltage	STM1813/1818 only			0.4	V
V _{OH}		Output high voltage	0 < I _{OH} < 500 μA	V _{CC} - 0.5	V _{CC} - 0.1		V
I _{OH}		$\overline{\text{RST}}$ output source current	V _{CC} ≥ V _{RST} (max.), reset not asserted (STM1810/STM1815)		350		μA
		RST output source current	V _{CC} ≤ V _{RST} (min.), reset asserted (STM1812/STM1817)		350		μA
I _{OL}		$\overline{\text{RST}}$ output sink current	V _{CC} ≥ 2.7 V, reset asserted, V _{OUT} = 0.4 V (STM1810/1811/1813/1815/1816/1818)	10			mA
		RST output sink current	V _{CC} ≥ 2.7 V, reset not asserted, V _{OUT} = 0.4 V, (STM1812/1817)	10			mA
C _{OUT}		Output capacitance ⁽²⁾				10	pF
Reset thresholds							
V _{RST}		Reset threshold	STM181xL	25 °C		4.62	V
				-40 to 105 °C	4.50		4.75
			STM181xM	25 °C		4.37	V
				-40 to 105 °C	4.25		4.49
			STM181xT	25 °C		3.06	V
				-40 to 105 °C	2.98		3.15
			STM181xS	25 °C		2.88	V
				-40 to 105 °C	2.80		2.97
STM181xR	25 °C		2.55	V			
	-40 to 105 °C	2.47		2.64	V		
t _{RD}		V _{CC} to $\overline{\text{RST}}$ delay	V _{CC} = (V _{TH} + 100 mV) falling to (V _{TH} - 200 mV)		2	5	μs
	t _{rec}	$\overline{\text{RST}}$ pulse width	V _{CC} Rising	100	150	200	ms
Push-button reset detect (STM1813, STM1818)							
t _{PB}		Push-button detect to $\overline{\text{RST}}$	STM1813/1818	1.5			μs
t _{PBRST}		Push-button $\overline{\text{RST}}$ time-out	From rising edge	100	150	200	ms
		Internal pull-up resistance	STM1811/1816	3.5	5.5	7.5	kΩ
			STM1813/1818	3.1	5.5	7.5	kΩ

1. Valid for ambient operating temperature: T_A = -40 °C to 105 °C; V_{CC} = 1.2 V to 5.5 V (except where noted).

2. The STM1811/1813/1816/1818 have an internal pull-up resistor which may sink 1 mA of current.

Table 10. SOT23-3 – 3-lead small outline transistor package mechanical data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		0.89	1.12		0.035	0.044
A1		0.01	0.10		0.001	0.004
A2		0.88	1.02		0.035	0.042
b		0.30	0.50		0.012	0.020
C		0.08	0.20		0.003	0.008
D		2.80	3.04		0.110	0.120
E		2.10	2.64		0.083	0.104
E1		1.20	1.40		0.047	0.055
e		0.89	1.03		0.035	0.041
e1		1.78	2.05		0.070	0.081
L	0.54			0.021		
L1		0.40	0.60		0.016	0.024
Q		0 °	8 °		0 °	8 °
N		3			3	

7 Part numbering

Table 11. Ordering information scheme

Example	STM1810	L	WX	7	F
Device type					
STM181x					
Reset threshold voltage					
STM1810 - 1813					
L = $V_{RST} = 4.50 \text{ V to } 4.75 \text{ V (4.62 V typ.)}$					
M = $V_{RST} = 4.25 \text{ V to } 4.49 \text{ V (4.37 V typ.)}$					
STM1815 - 1818					
T = $V_{RST} = 2.98 \text{ V to } 3.15 \text{ V (3.06 V typ.)}$					
S = $V_{RST} = 2.80 \text{ V to } 2.97 \text{ V (2.88 V typ.)}$					
R = $V_{RST} = 2.47 \text{ V to } 2.64 \text{ V (2.55 V typ.)}$					
Package					
WX = SOT23-3					
Temperature range					
7 = -40 to 105 °C					
Shipping method					
F = ECOPACK package, tape and reel					

Note: Contact the local ST sales office for availability.

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

Table 12. Marking description

Part number	Reset threshold	Output	Topside marking ⁽¹⁾
STM1810L	4.62 V	Push-pull \overline{RST}	9AAx
STM1810M	4.37 V	Push-pull \overline{RST}	9ABx
STM1811L	4.62 V	Open-drain \overline{RST}	9AHx
STM1811M	4.37 V	Open-drain \overline{RST}	9AJx
STM1812L	4.62 V	Push-pull RST	9AQx
STM1812M	4.37 V	Push-pull RST	9ARx
STM1813L	4.62 V	Open-drain \overline{RST}	9AXx
STM1813M	4.37 V	Open-drain \overline{RST}	9AYx
STM1815T	3.06 V	Push-pull \overline{RST}	9BGx
STM1815S	2.88 V	Push-pull \overline{RST}	9BHx
STM1815R	2.55 V	Push-pull \overline{RST}	9BJx
STM1816T	3.06 V	Open-drain \overline{RST}	9BPx
STM1816S	2.88 V	Open-drain \overline{RST}	9BQx
STM1816R	2.55 V	Open-drain \overline{RST}	9BRx
STM1817T	3.06 V	Push-pull RST	9BWx
STM1817S	2.88 V	Push-pull RST	9BXx
STM1817R	2.55 V	Push-pull RST	9BYx
STM1818T	3.06 V	Open-drain \overline{RST}	9CDx
STM1818S	2.88 V	Open-drain \overline{RST}	9CEx
STM1818R	2.55 V	Open-drain \overline{RST}	9CFx

1. x = letter assigned to indicate assembly work week (i.e., A = WW01 and WW02, B = WW03 and WW04, C = WW05 and WW06..., Z = WW51, WW52, and WW53).

8 Revision history

Table 13. Document revision history

Date	Revision	Changes
26-Aug-04	1.0	First Issue.
05-Oct-04	2.0	Update reset characteristics, add typical graphs, remove SC70 references (Figure 1 , 3 , 6 , 10 , 11 , 13 , 14 , 15 , 16 , 17 , 18 , 19 ; and 20 , Table 9 , 11 , and 12).
19-Nov-04	3.0	Update dimensions (Table 10).
07-Dec-04	4.0	Remove some voltage options (Table 1 , 10 , 11 , and 12).
29-Jun-05	5.0	Temperature range change (Figure 13 , 14 , 15 , and 18 ; Table 8 , 9 , and 11).
11-Oct-05	6.0	Update typical operating characteristics, Lead-free text (Figure 13 , 14 , 15 , 16 , 17 , 18 , and 19 ; Table 11 , and 12).
28-Aug-2007	7	Document reformatted. Update Table 12 .
02-Sep-2010	8	Document reformatted, updated Section 6.1: ECOPACK® , corrected typo in Table 9 , Table 11 and Table 12 .

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