National Semiconductor

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CLC5665
Low Distortion Amplifier with Disable

General Description

The CLC5665 is a low cost, wideband amplifier that provides very low 2nd and 3rd harmonic distortion at 1MHz (−89/−92dBc). The great slew rate of 1800V/µs, bandwidth of 90MHz (A_V = +1) and fast disable make it an excellent choice for many high speed multiplexing applications. Like all current feedback op amps, the CLC5665 allows the frequency response to be optimized (or adjusted) by the selection of the feedback resistor. For demanding video applications, the 0.1 dB bandwidth to 20MHz and differential gain/phase of 0.05%/0.05° make the CLC5665 the preferred component for broadcast quality NTSC and PAL video systems.

The large voltage swing ($28V_{PP}$) , continuous output current (85mA) and slew rate (1800V/µs) provide high fidelity signal conditioning for applications such as CCDs, transmission lines and low impedance circuits.

xDSL, video distribution, multimedia and general purpose applications will benefit from the CLC5665's wide bandwidth and disable feature. Power is reduced and the output becomes a high impedance when disabled. The wide gain range of the CLC5665 makes this general purpose op amp an improved solution for circuits such as active filters, differential-to-single-ended drivers, DAC transimpedance amplifiers and MOSFET drivers.

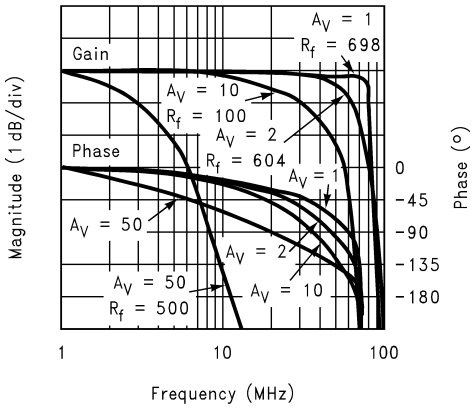
Features

- 0.1dB gain flatness to 20MHz (A_V = +2)
- 90MHz bandwidth (A_V = +1)
- Large signal BW 25MHz
- 1800V/µs slew rate
- 0.05%/0.05° differential gain/phase
- ±5V, ±15V or single supplies
- 200ns disable to high impedance output
- Wide gain range
- −89/−92dBc HD2/HD3 (R_L=500Ω)
- Low cost

Applications

- xDSL driver
- Twisted pair driver
- Cable driver
- Video distribution
- CCD clock driver
- Multimedia systems
- DAC output buffers
- Imaging systems

Non-Inverting Frequency Response



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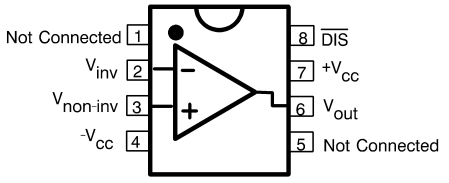
Connection Diagram



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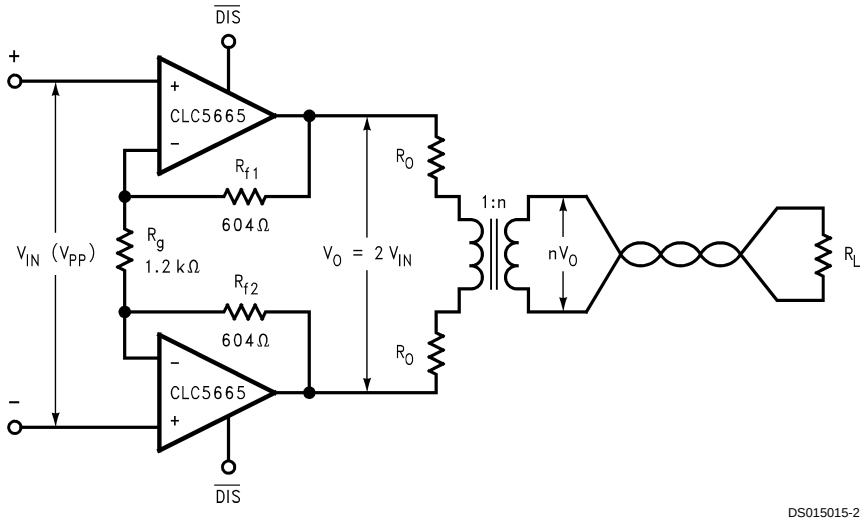
Pinout
DIP & SOIC

Typical Application



Differential Line Driver for xDSL

Ordering Information

Package	Temperature Range Industrial	Packaging Marking	NSC Drawing
8-pin plastic DIP	−40˚C to +85˚C	CLC5665IN	N08E
8-pin plastic SOIC	−40˚C to +85˚C	CLC5665IM	M08A
		CLC5665IMX	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±16V
Short Circuit Current	(see (Note 4))
Common-Mode Input Voltage	$\pm V_{CC}$
Maximum Junction Temperature	+150˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (soldering 10 sec)	+300˚C

Operating Ratings

Thermal Resistance

Package	(θ_{JC})	(θ_{JA})
MDIP	65˚C/W	130˚C/W
SOIC	50˚C/W	145˚C/W

Electrical Characteristics

V_{CC} = ±15V, A_V= +2V/V; R_f =604Ω, R_L =100Ω; unless specified

Symbol	Parameter	Conditions	V_{CC}	Typ	Min/Max Ratings (Note 2)			Units
Ambient Temperature		CLC5665IN/IM		+25˚C	+25˚C	0 to 70˚C	−40 to 85˚C	
Frequency Domain Response								
	Small-Signal Bandwidth (A_V = +1)	V_{OUT} <1.0V_{PP}	±15	90				MHz
	Small-Signal Bandwidth	V_{OUT}<1.0V_{PP}	±15	70				MHz
		V_{OUT}<1.0V_{PP}	±5	50				MHz
	0.1dB Bandwidth	V_{OUT}<1.0V_{PP}	±15	20				MHz
		V_{OUT}<1.0V_{PP}	±5	15				MHz
	Large-Signal Bandwidth	V_{OUT}< 10V_{PP}		25				MHz
	Gain Flatness	V_{OUT} < 1.0V_{PP}						
	Peaking	DC to 10MHz		0.03				dB
	Rolloff	DC to 20MHz		0.1				dB
	Linear Phase Deviation	DC to 20MHz		0.7				deg
	Differential Gain	R_L = 150Ω, 4.43MHz	±15	0.05				%
		R_L = 150Ω, 4.43MHz	±5	0.05				%
	Differential Phase	R_L = 150Ω, 4.43MHz	±15	0.05				deg
		R_L = 150Ω, 4.43MHz	±5	0.1				deg
Time Domain Response								
	Rise and Fall Time	2V Step		5				ns
		10V Step		10				ns
	Settling Time to 0.05%	2V Step		35				ns
	Overshoot	2V Step		5				%
	Slew Rate	20V Step		1800				V/µs
Distortion And Noise Response								
	2nd Harmonic DIstortion	1V_{PP},1MHz, R_L = 500Ω		−89				dBc
	3rd Harmonic Distortion	2V_{PP},1MHz, R_L = 500Ω		−92				dBc
	Input Voltage Noise	>1MHz		3.0				nV/$\sqrt{Hz}$
	Non-Inverting Input Current Noise	>1MHz		3.2				pA/$\sqrt{Hz}$
	Inverting Input Current Noise	>1MHz		15				pA/$\sqrt{Hz}$
DC Performance								
	Input Offset Voltage (Note 3)		±15	1.0	7.5	9.0	10.0	mV
	Average Drift			25				µV/˚C

Electrical Characteristics (Continued)

V_{CC} = ±15V, A_V= +2V/V; R_f =604Ω, R_L =100Ω; unless specified

Symbol	Parameter	Conditions	V_{CC}	Typ	Min/Max Ratings (Note 2)			Units
DC Performance								
	Input Bias Current (Note 3)	Non-Inverting	±15, ±5	3	20	20	20	µA
	Average Drift			10				nA/˚C
	Input Bias Current (Note 3)	Inverting	±15, ±5	3	20	20	20	µA
	Average Drift			10				nA/˚C
	Power Supply Rejection Ratio	DC		60	55	50	50	dB
	Common-Mode Rejection Ratio	DC		60	55	50	50	dB
	Supply Current (Note 3)	R_L=∞	±15, ±5	11,8.5	12	14	15	mA
	Disabled (Note 3)	R_L=∞	±15, ±5	1.5	2.5	2.5	2.5	mA
Switching Performance								
	Turn on Time			400	500	550	550	ns
	Turn Off Time	(Note 5)		200	800	800	800	ns
	Off Isolation	10MHz		59	56	56	56	dB
	High Input Voltage	V_{IH}	±15	11.8	12.5	12.7		V
			±5	1.8	2.5	2.7		V
	Low Input Voltage	V_{IL}	±15	10.8	10.5	10.0		V
			±5	0.8	0.6	0.1		V
Miscellaneous Performance								
	Non-Inverting Input Resistance			8.0	3.0	2.5	1.7	MΩ
	Non-Inverting Input Capacitance			0.5	1.0	1.0	1.0	pF
	Input Voltage Range	Common Mode	±15	±12.5	±12.3	±12.1	±11.8	Ω
		Common Mode	±5	±2.5	±2.3	±2.2	±1.9	V
	Output Voltage Range	R_L = ∞	±15	±14	±13.7	±13.7	±13.6	V
		R_L = ∞	±5	±4.0	±3.9	±3.8	±3.7	V
	Output Current			±85	±60	±50	±45	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

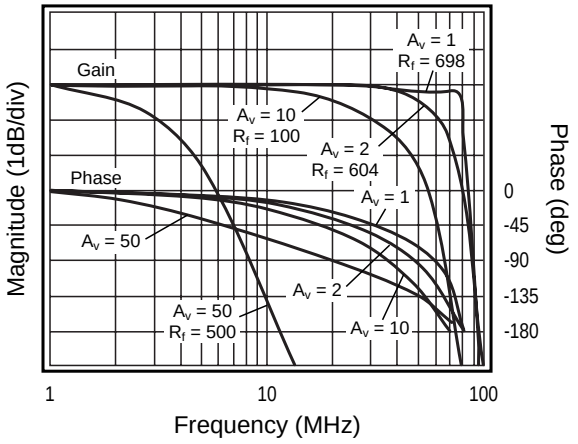
Note 3: AJ-level: spec. is 100% tested at +25˚C.

Note 4: Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 125mA.

Note 5: To >50dB attenuation @10MHz.

Typical Performance Characteristics (V_{CC} = ±15V, A_V = +2V/V; R_f = 604Ω, R_L = 100;Ω unless specified)

Non-Inverting Frequency Response



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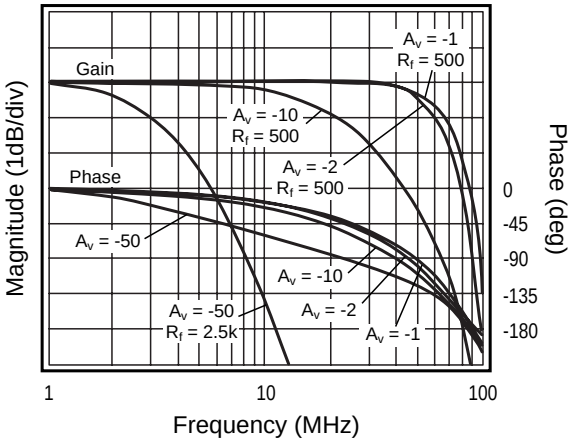
Inverting Frequency Response



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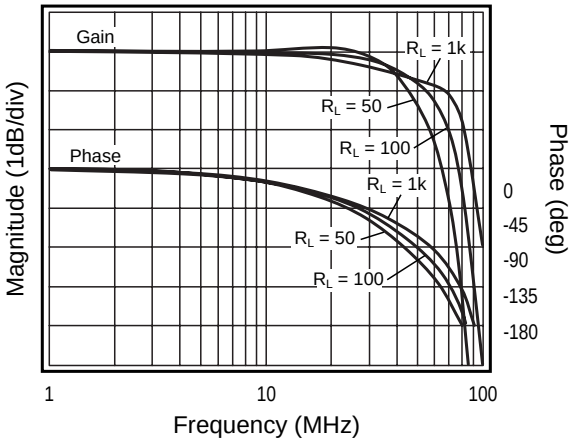
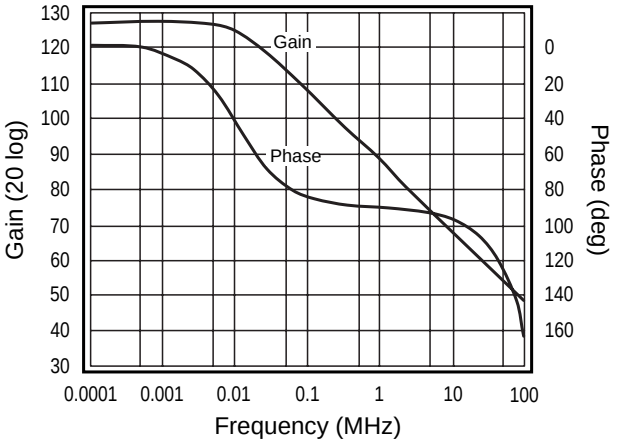
Frequency Response vs. Load



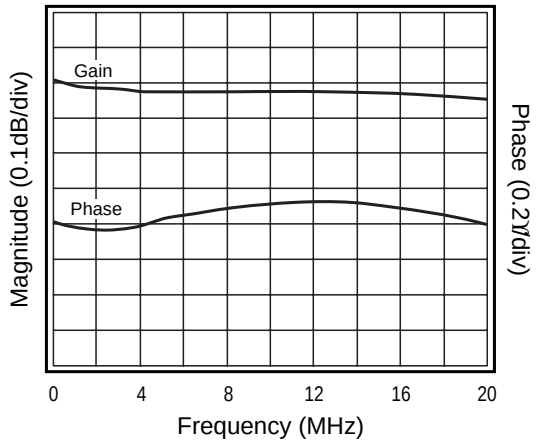
DS015015-6

Open-Loop Transimpedance Gain (Zs)



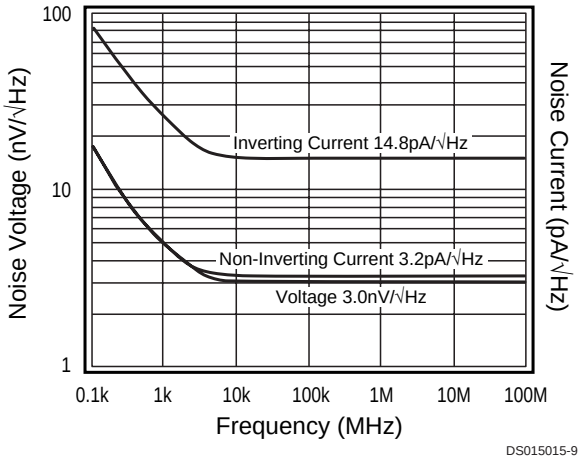
DS015015-7

Flatness Gain and Linear Phase



DS015015-8

Equivalent Input Noise



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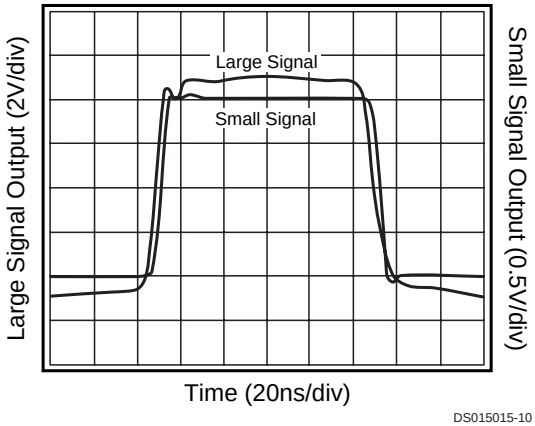
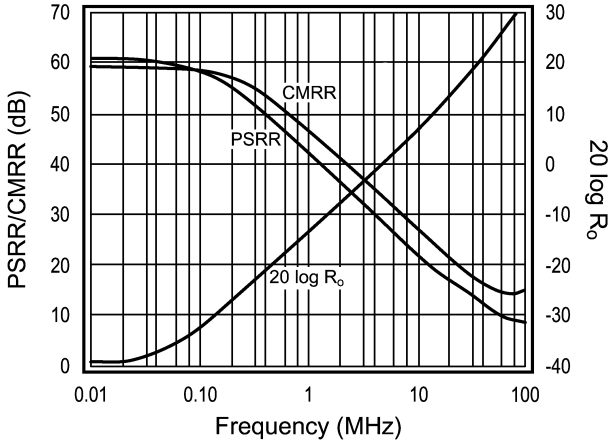
Typical Performance Characteristics (V_{CC} = ±15V, A_V = +2V/V; R_f = 604Ω, R_L = 100;Ω unless specified)) (Continued)

Signal Pulse Response



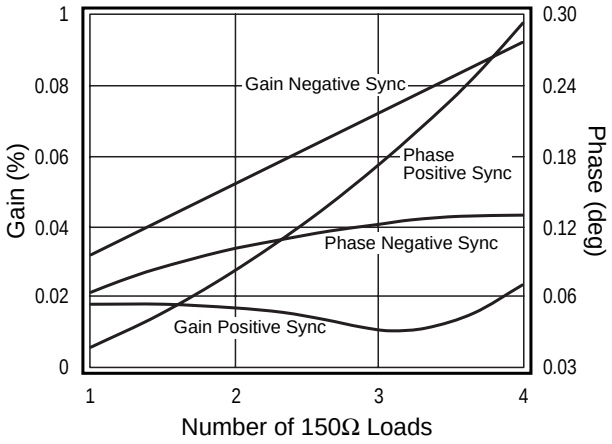
DS015015-10

PSRR, CMRR and Closed Loop R_O



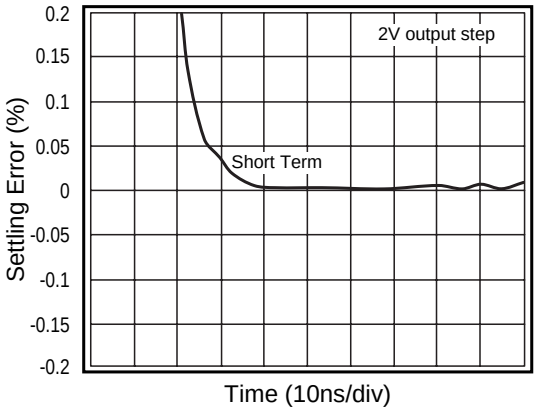
DS015015-11

Differential Gain and Phase (3.58MHz)



DS015015-12

Short Term Settling Time



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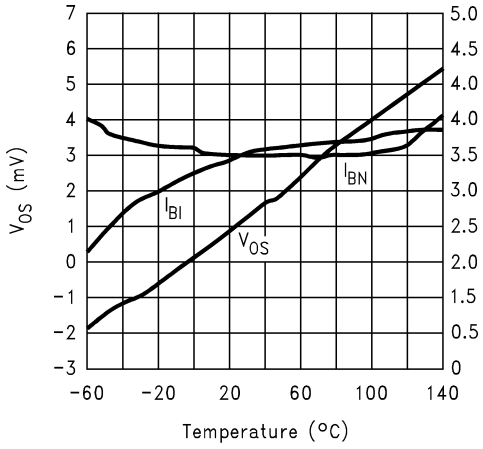
I_{BI}, I_{BN}, V_{OS} vs. Temperature



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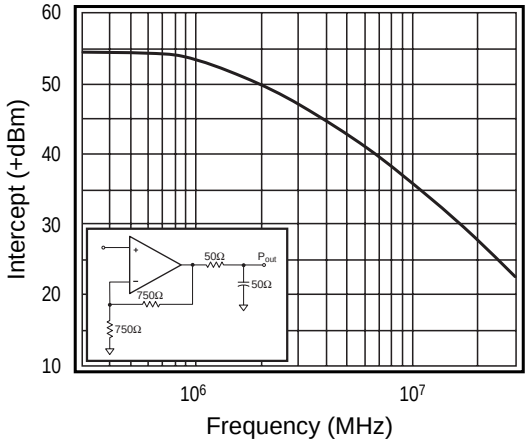
2-Tone, 3rd Order Intermodulation Intercept



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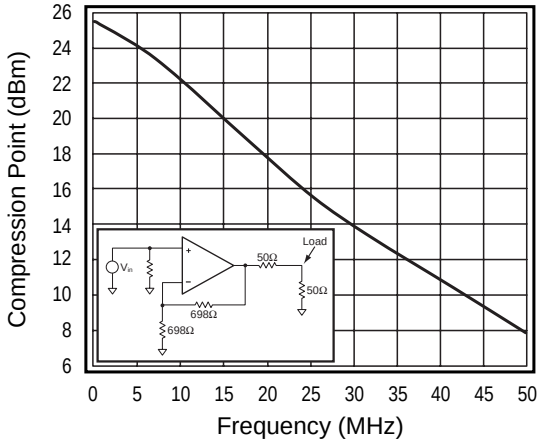
Typical Performance Characteristics (V_{CC} = ±15V, A_V = +2V/V; R_f = 604Ω, R_L = 100;Ω unless specified)) (Continued)

−1dBm Compression to Load



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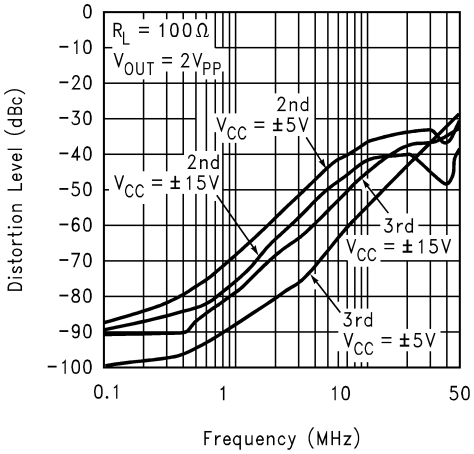
Harmonic Distortion vs. Frequency



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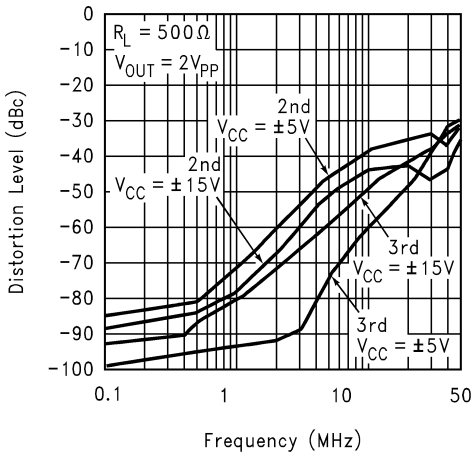
Harmonic Distortion vs. Frequency



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Application Division

General Design Considerations

The CLC5665 is a general purpose current-feedback amplifier for use in a variety of small- and large-signal applications. Use the feedback resistor to fine tune the gain flatness and −3dB bandwidth for any gain setting. National provides information for the performance at a gain of +2 for small and large signal bandwidths. The plots show feedback resistor values for selected gains.

Gain

Use the following equations to set the CLC5665's non-inverting or inverting gain:

$$\text{Non}-\text{Inverting Gain} = 1 + \frac{R_f}{R_g}$$

$$\text{Inverting Gain} = \frac{-R_f}{R_g}$$

Choose the resistor values for non-inverting or inverting gain by the following steps.

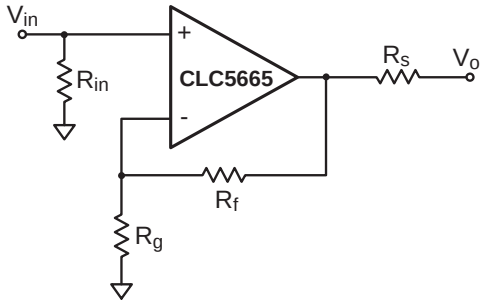


FIGURE 1. Component Identification

1) Select the recommended feedback resistor R_f (refer to plot in the plot section entitled R_f vs. Gain).

2) Choose the value of R_g to set gain.

3) Select R_s to set the circuit output impedance.

4) Select R_{in} for input impedance and input bias.

High Gains

Current feedback closed-loop bandwidth is independent of gain-bandwidth-product for small gain changes. For larger gain changes the optimum feedback resister R_f is derived by the following:

$$R_f = 724\Omega - 60\Omega \cdot (A_V)$$

As gain is increased, the feedback resistor allows bandwidth to be held constant over a wide gain range. For a more complete explanation refer to application note OA-25 **Stability Analysis of Current-Feedback Amplifiers**.

Resistors have varying parasitics that affect circuit performance in high speed design. For best results, use leaded metal film resistors or surface mount resistors. A SPICE model for the CLC430 is available to simulate overall circuit performance.

Enable/Disable Function

The CLC430 amplifier features an enable/disable function that changes the output and inverting input from low to high impedance. The pin 8 enable/disable logic levels are as follows:

V_{CC}	±15V	±5V
Enable	>12.7V	>2.7V
Disable	<10.0V	<0.8V

The amplifier is enabled with pin 8 left open due to the 2kΩ pull-up resistor, shown in *Figure 2*.

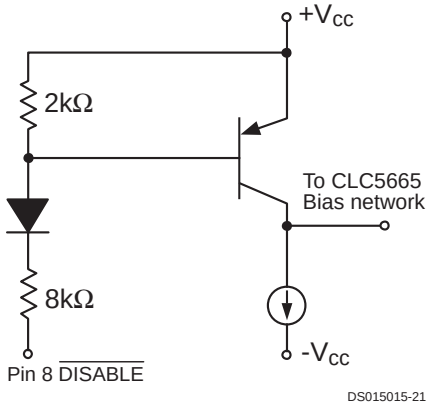
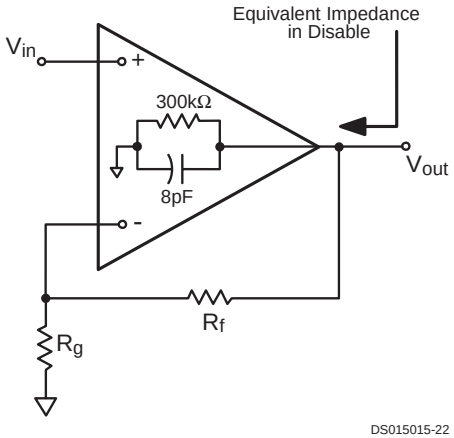


FIGURE 2. Pin 8 Equivalent Disable Circuit

Open-collector or CMOS interfaces are recommended to drive pin 8. The turn on and off time depends on the speed of the digital interface.

The equivalent output impedance when disabled is shown in *Figure 3*. With R_g connected to ground, the sum of R_f and R_g dominates and reduces the disabled output impedance. To raise the output impedance in the disabled state, connect the CLC5665 as a unity-gain voltage follower by removing R_g. Current-feedback op amps need the recommended R_f in a unity-gain follower circuit. For high density circuit layouts consider using the dual CLC431 (with disable) or the dual CLC432 (without disable).



Application Division (Continued)

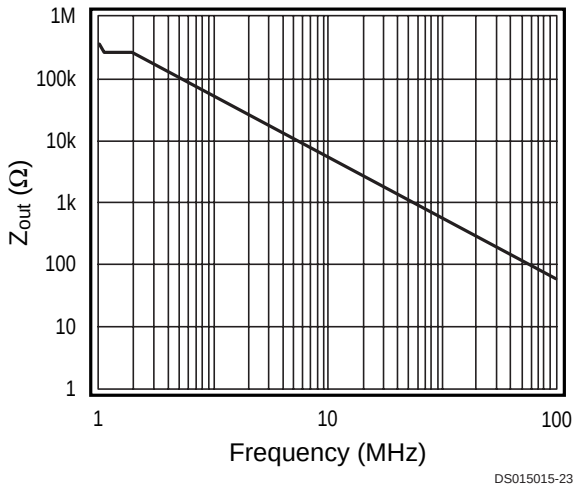


FIGURE 3. Equivalent Disabled Output Impedance

2nd and 3rd Harmonic Distortion

To meet low distortion requirements, recognize the effect of the feedback resistor. Increasing the feedback resistor will decrease the loop gain and increase distortion. Decreasing the load impedance increases 3rd harmonic distortion more than 2nd.

Differential Gain and Differential Phase

The CLC5665 has low DG and DP errors for video applications. Add an external pulldown resistor to the CLC5665's output to improve DG and DP as seen in *Figure 4*. A 604Ω R_P will improve DG and DP to 0.01% and 0.02˚.

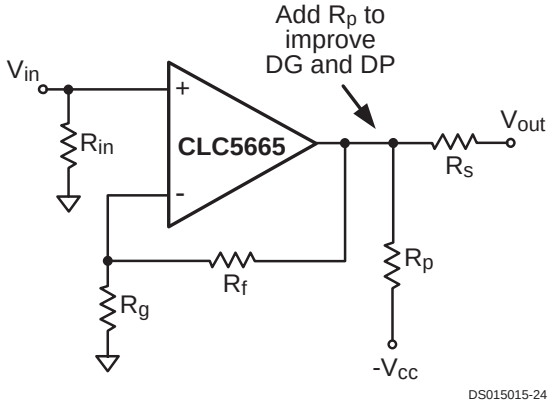


FIGURE 4. Improved DG and DP Video Amplifier

Printed Circuit Layout

To get the best amplifier performance careful placement of the amplifier, components and printed circuit traces must be observed. Place the 0.1µF ceramic decoupling capacitors less than 0.1″ (3mm) from the power supply pins. Place the 6.8µF tantalum capacitors less than 0.75″ (20mm) from the power supply pins. Shorten traces between the inverting pin and components to less than 0.25″ (6mm). Clear ground plane 0.1″ (3mm) away from pads and traces that connect to the inverting, non-inverting and output pins. Do not place ground or power plane beneath the op amp package. National provides literature and evaluation boards 730013 DIP or 730027 SOIC illustrating the recommended op amp layout.

Applications Circuits

Level Shifting

The circuit shown in *Figure 5* implements level shifting by AC coupling the input signal and summing a DC voltage. The resistor R_{in} and the capacitor C set the high pass break frequency. The amplifier closed-loop bandwidth is fixed by the selection of R_f. The DC and AC gains for circuit of *Figure 5* are different. The AC gain is set by the ratio of R_f and R_g. And the DC gain is set by the parallel combination of R_g and R_2.

$$V_{out} = V_{in_{ac}} \left(1 + \left(\frac{R_f}{R_g \| R_2}\right)\right) - V_{in_{DC}} \left(\frac{R_f}{R_2}\right)$$

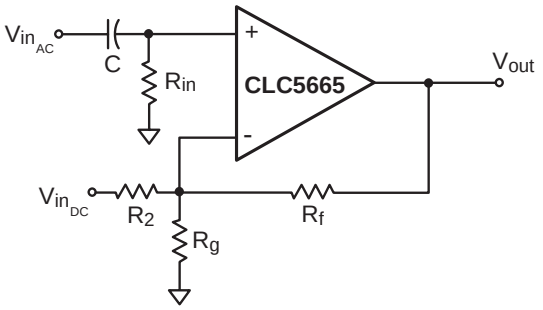


FIGURE 5. Level Shifting Circuit

Multiplexing

Multiple signal switching is easily handled with the disable function of the CLC5665. Board trace capacitance at the output pin will affect the frequency response and switching transients. To lessen the effects of output capacitance place a resistor (R_o) within the feedback loop to isolate the outputs as shown in *Figure 6*. To match the mux output impedance to a transmission line, add a resistor (R_s) in series with the output.

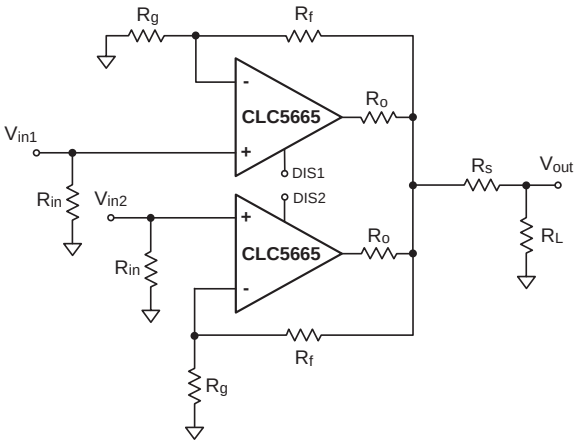


FIGURE 6. Output Connection for Multiplexing Circuits

Differential Line Driver With Load Impedance Conversion

The circuit shown in *Figure 7*, operates as a differential line driver. The transformer converts the load impedance to a value that best matches the CLC5665's output capabilities. The single-ended input signal is converted to a differential signal by the CLC5665. The line's characteristic impedance

Application Division (Continued)

is matched at both the input and the output. The schematic shows Unshielded Twisted Pair for the transmission line; other types of lines can also be driven.

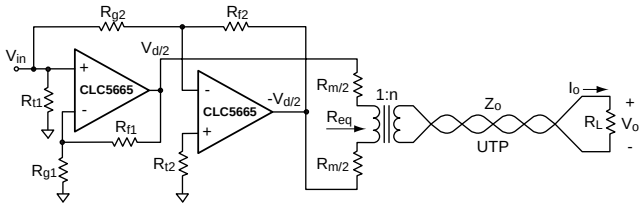


FIGURE 7. Differential Line Driver with Load Impedance Conversion

Set up the CLC5665 as a difference amplifier. V_d is determined by:

$$\frac{V_d}{V_{in}} = 2 \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) = 2 \cdot \frac{R_{f2}}{R_{g2}}$$

Make the best use of the CLC5665's output drive capability as follows:

$$R_m + R_{eq} = \frac{2 \cdot V_{max}}{I_{max}}$$

where R_{eq} is the transformed value of the load impedance, V_{max} is the Output Voltage Range, and I_{max} is the maximum Output Current.

Match the line's characteristic impedance:

$$R_L = Z_o$$
$$R_m = R_{eq}$$
$$n = \sqrt{\frac{R_L}{R_{eq}}}$$

Select the transformer so that it loads the line with a value very near Z_O over frequency range. The output impedance of the CLC5665 also affects the match. With an ideal transformer we obtain:

$$\text{Return Loss} = -20 \cdot \log_{10} \left| \frac{n^2 \cdot Z_{O(5665)}(j\omega)}{Z_O} \right|, \text{dB}$$

where $Z_{o(5665)}(j\omega)$ is the output impedance of the CLC5665 and $|Z_{O(5665)}(j\omega)| << R_m$.

The load voltage and current will fall in the ranges:

$$\left| V_O \right| \le n \cdot V_{max}$$
$$\left| I_O \right| \le \frac{I_{max}}{n}$$

The CLC5665's high output drive current and low distortion make it a good choice for this application.

Full Duplex Cable Driver

The circuit shown in Figure 8 below, operates as a full duplex cable driver which allows simultaneous transmission and reception of signals on one transmission line. The circuit on either side of the transmission line uses are CLC5665 as a cable driver, and the second CLC5665 as a receiver. V_{oA} is an attenuated version of V_{inA}, while V_{oB} is a attenuated version of V_{inB}.

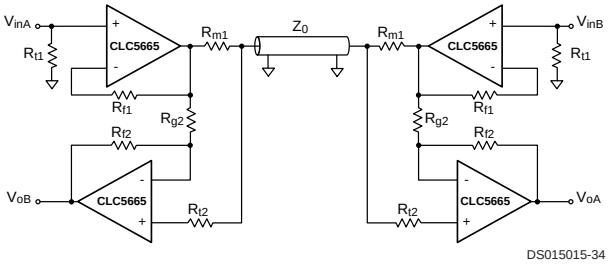


FIGURE 8. Full Duplex Cable Driver

R_{m1} is used to match the transmission line. R_{f2} and R_{g2} set the DC gain of the CLC5665, which is used in a difference mode. R_{t2} provides good CMRR and DC offset. The transmitting CLC5665's are shown in a unity gain configuration because they consume the least power of any gain, for a given load. For proper operation we need $R_{f2} = R_{g2}$.

The receiver output voltages are:

$$V_{outA(B)} \approx V_{inA(B)} \cdot A + \frac{V_{inB(A)}}{2} \cdot \left(1 - \frac{R_{f2}}{R_{g2}} + \frac{Z_{o(5665)}(j\omega)}{R_{m1}}\right)$$

where A is the attenuation of the cable, $Z_{o(5665)}(j\omega)$ is the ouput impedance of the CLC5665, and $|Z_{o(5665)}(j\omega)| << R_{m1}$.

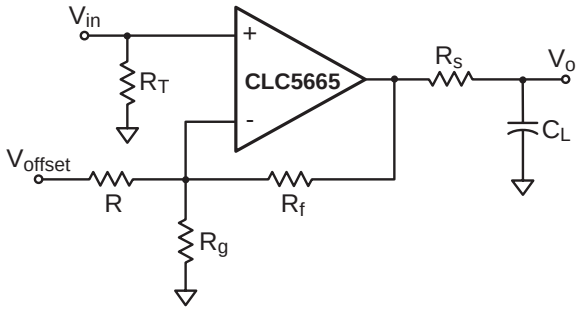
We selected the component values as follows:

- R_f1 1.2kΩ, the recommended value for CLC5665 at unity gain
- $R_{m1}Z_o$=50, the characteristic impedance of the transmission line
- $R_{f2} = R_{g2}$ 750Ω ≥ Rm1, the recommended value for the CLC5665 at A_V=2
- $R_{t2} = (R_{f2}||R_{g2}) - R_{m1}/2 = 25\Omega$

These values give excellent isolation from the other input:

$$\frac{V_{oA(B)}}{V_{inB(A)}} \approx -38\text{dB}, \; f = 5.0\text{MHz}$$

The CLC5665 provides large output current drive, while consuming little supply current, at the nominal bias point. It also produces low distortion with large signal swings and heavy loads. These features make the CLC5665 an excellent choice for driving transmission lines.



Application Division (Continued)

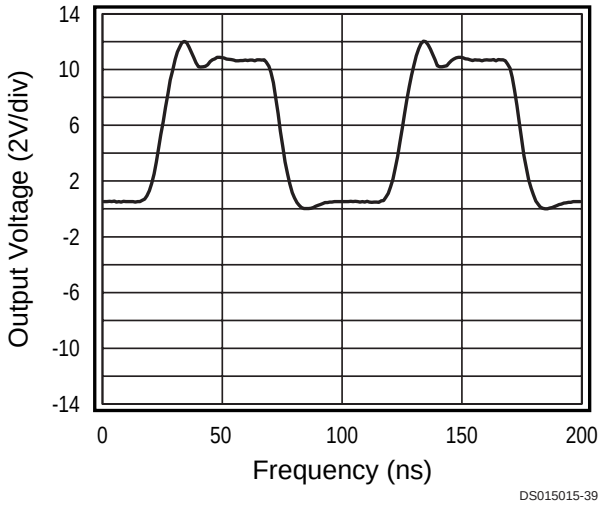
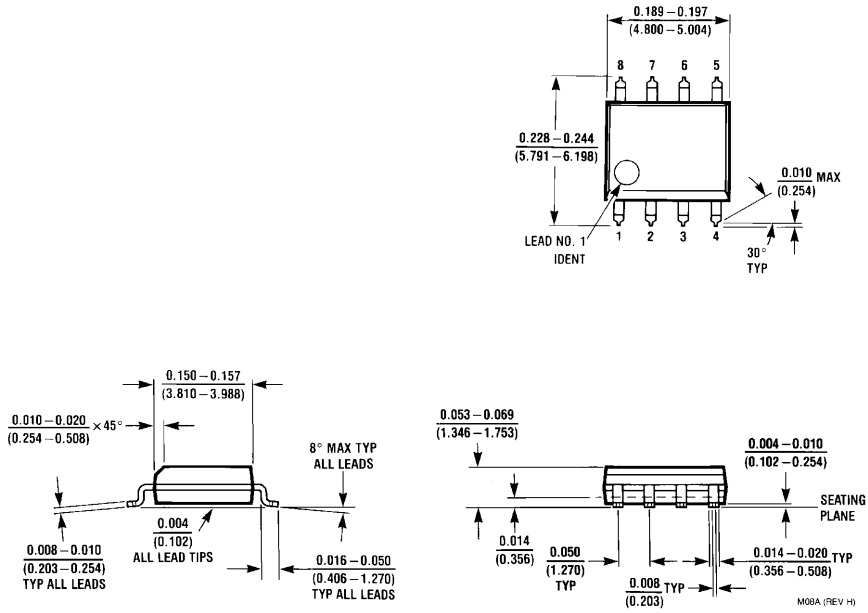
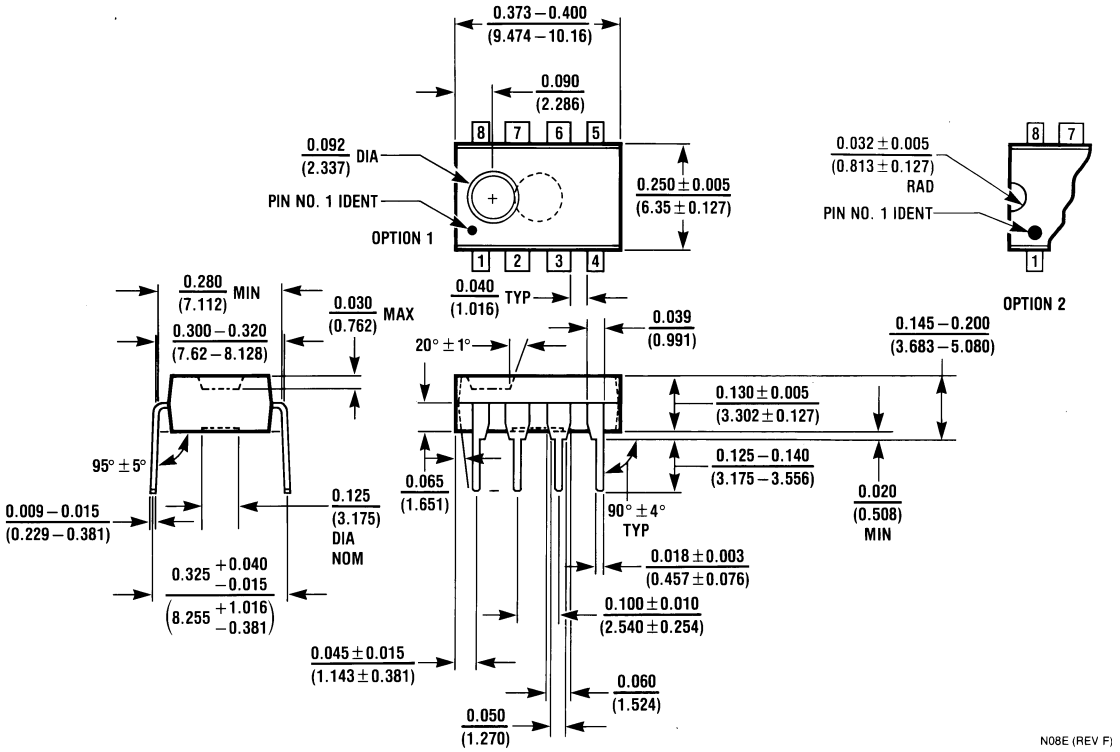


FIGURE 9. CCD Clock Driver

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NSC Package Number M08A



8-Pin MDIP
NSC Package Number N08E

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