Low Cost CMOS, High Speed, Rail-to-Rail Amplifiers

ADA4891-1/ADA4891-2

FEATURES

- **Low cost**
- **High speed and fast settling**
  - **−3 dB bandwidth: 240 MHz (G = +1)**
  - **Slew rate: 170 V/µs**
  - **Settling time to 0.1%: 28 ns**
- **Video specifications (G = +2, R_L = 150 Ω)**
  - **0.1 dB gain flatness: 25 MHz**
  - **Differential gain error: 0.05%**
  - **Differential phase error: 0.25°**
- **Single-supply operation**
  - **Wide supply range: 2.7 V to 5.5 V**
  - **Output swings to within 50 mV of supply rails**
- **Low distortion: 79 dBc SFDR @ 1 MHz**
- **Linear output current: 150 mA @ −50 dBc**
- **Low power of 4.4 mA per amplifier**

APPLICATIONS

- **Imaging**
- **Consumer video**
- **Active filters**
- **Coaxial cable drivers**
- **Clock buffers**
- **Photodiode preamp**
- **Contact image sensor and buffers**

GENERAL DESCRIPTION

The ADA4891-1 (single) and ADA4891-2 (dual) are CMOS, high speed amplifiers that offer high performance at a low cost. The amplifiers feature true single-supply capability, with an input voltage range that extends 300 mV below the negative rail.

In spite of their low cost, the ADA4891 family provides high performance and versatility. The rail-to-rail output stage enables the output to swing within 50 mV of each rail, enabling maximum dynamic range.

The ADA4891 family of amplifiers are ideal for imaging applications, such as consumer video, CCD buffers, and contact image sensor buffers. Low distortion and fast settling time also make them ideal for active filter applications.

The ADA4891-1/ADA4891-2 are available in a wide variety of packages. The ADA4891-1 is available in 8-lead SOIC and 5-lead SOT-23 packages. The ADA4891-2 is available in 8-lead SOIC and 8-lead MSOP packages. The amplifiers are specified to operate over the extended temperature range of −40°C to +125°C.

CONNECTION DIAGRAMS

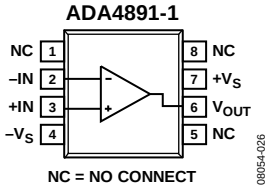

Figure 1. 8-Lead SOIC (R-8)

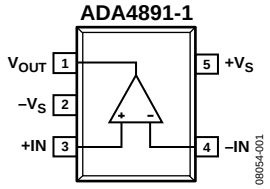

Figure 2. 5-Lead SOT-23 (RJ-5)

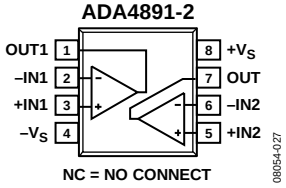

Figure 3. 8-Lead SOIC (R-8) and 8-Lead MSOP (RM-8)

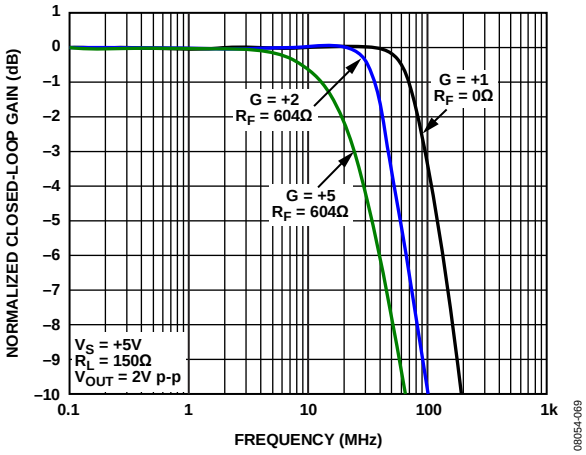

Figure 4. Large Signal Frequency Response vs. Gain, V_S = 5 V

Rev. A

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2/10—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 5 V, R_L = 1 kΩ to 2.5 V, unless otherwise noted.

Table 1.

Parameter	Test Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p		240		MHz
	G = +2, V_O = 0.2 V p-p, R_L = 150 Ω to 2.5 V, R_F = 604 Ω		90		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 2 V p-p, R_L = 150 Ω to 2.5 V, R_F = 604 Ω		25		MHz
Slew Rate (t_R/t_F)	G = +2, V_O = 2 V step		170/210		V/µs
Large Signal Frequency Response	G = +2, V_O = 2 V p-p, R_L = 150 Ω		40		MHz
Settling Time to 0.1%	G = +2, V_O = 2 V step		28		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion, HD2/HD3	f_C = 1 MHz, V_O = 2 V p-p, G = +1		−79/−93		dBc
Harmonic Distortion, HD2/HD3	f_C = 1 MHz, V_O = 2 V p-p, G = −1		−75/−91		dBc
Input Voltage Noise	f = 1 MHz		10		nV/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω to 2.5 V		0.05		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω to 2.5 V		0.25		Degrees
Crosstalk	f = 5 MHz, G = +2, V_O = 2 V p-p		−80		dB
DC PERFORMANCE					
Input Offset Voltage			±2.5	±10	mV
	T_{MIN} to T_{MAX}		±3.2		mV
Offset Drift			6		µV/°C
Input Bias Current		−50	+2	+50	pA
Open-Loop Gain		77	83		dB
	R_L = 150 Ω to 2.5 V		71		dB
INPUT CHARACTERISTICS					
Input Resistance			5		GΩ
Input Capacitance			3.2		pF
Input Common-Mode Voltage Range			$-V_S$ − 0.3 to $+V_S$ − 0.8		V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0 V to 3.0 V		71		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ to 2.5 V		0.005 to 4.985		V
	R_L = 150 Ω to 2.5 V		0.065 to 4.9		V
Output Current	1% THD with 1 MHz, 2 V p-p output		150		mA
Short-Circuit Current	Sourcing		250		mA
	Sinking		225		mA
Capacitive Load Drive	G = +1, <30% overshoot		15		pF
POWER SUPPLY					
Operating Range		2.7		5.5	V
Quiescent Current per Amplifier			4.4		mA
Positive Power Supply Rejection Ratio (PSRR)	$+V_S$ = 5 V to 5.25 V, $-V_S$ = 0 V		65		dB
Negative Power Supply Rejection Ratio (PSRR)	$+V_S$ = 5 V, $-V_S$ = −0.25 V to 0 V		63		dB
OPERATING TEMPERATURE RANGE		−40		+125	°C

T_A = 25°C, V_S = 3.0 V, R_L = 1 kΩ to 1.5 V, unless otherwise noted.

Table 2.

Parameter	Test Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p		190		MHz
	G = +2, V_O = 0.2 V p-p, R_L = 150 Ω to 2.5 V, R_F = 604 Ω		75		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 2 V p-p, R_L = 150 Ω to 2.5 V, R_F = 604 Ω		18		MHz
Slew Rate (t_R/t_F)	G = +2, V_O = 2 V step		140/230		V/µs
Large Signal Frequency Response	G = +2, V_O = 2 V p-p, R_L = 150 Ω		40		MHz
Settling Time to 0.1%	G = +2, V_O = 2 V step		30		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 1 MHz, V_O = 2 V p-p, G = −1		−70/−89		dBc
Input Voltage Noise	f = 1 MHz		10		nV/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω to 0.5 V, $+V_S$ = 2 V, $-V_S$ = −1 V		0.23		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω to 0.5 V, $+V_S$ = 2 V, $-V_S$ = −1 V		0.77		Degrees
Crosstalk	f = 5 MHz, G = +2		−80		dB
DC PERFORMANCE					
Input Offset Voltage			±2.5	±10	mV
	T_{MIN} to T_{MAX}		±3.2		mV
Offset Drift			6		µV/°C
Input Bias Current		−50	+2	+50	pA
Open-Loop Gain		72	76		dB
	R_L = 150 Ω to 1.5 V		65		dB
INPUT CHARACTERISTICS					
Input Resistance			5		GΩ
Input Capacitance			3.2		pF
Input Common-Mode Voltage Range			$-V_S$ − 0.3 to $+V_S$ − 0.8		V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0 V to 1.5 V		68		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ to 1.5 V		0.005 to 2.985		V
	R_L = 150 Ω to 1.5 V		0.095 to 2.965		V
Output Current	1% THD with 1 MHz, 2 V p-p output		50		mA
Short-Circuit Current	Sourcing		150		mA
	Sinking		95		mA
Capacitive Load Drive	G = +1		15		pF
POWER SUPPLY					
Operating Range		2.7		5.5	V
Quiescent Current per Amplifier			3.5		mA
Positive Power Supply Rejection Ratio (PSRR)	$+V_S$ = 3 V to 3.15 V, $-V_S$ = 0 V		76		dB
Negative Power Supply Rejection Ratio (PSRR)	$+V_S$ = 3 V, $-V_S$ = −0.15 V to 0 V		72		dB
OPERATING TEMPERATURE RANGE		−40		+125	°C

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage (Common Mode)	$-V_S$ – 0.5 V to $+V_S$
Differential Input Voltage	$\pm V_S$
Storage Temperature Range (R)	−65°C to +125°C
Operating Temperature Range (A Grade)	−40°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the ADA4891-1/ADA4891-2 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit can cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

The still-air thermal properties of the package (θ_{JA}), the ambient temperature (T_A), and the total power dissipated in the package (P_D) can be used to determine the junction temperature of the die.

The junction temperature can be calculated as

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. It can be calculated by

$$P_D = (V_S \times I_S) + (V_S - V_{OUT}) \times V_{OUT}/R_L \quad (2)$$

where:
V_S is the positive supply rail.
I_S is the quiescent current.
V_{OUT} is the output of the amplifier.
R_L is the output load of the amplifier.

To ensure proper operating, it is necessary to observe the maximum power derating curve in Figure 5, where it is derived by setting T_J = 150°C in Equation 1. Figure 5 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 5-lead SOT-23 (146°C/W), the 8-lead SOIC (115°C/W), and the 8-Lead MSOP (133°C/W) on a JEDEC standard 4-layer board.

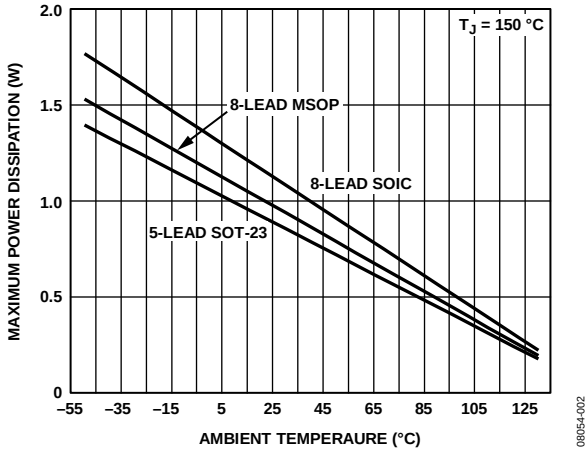


Figure 5. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

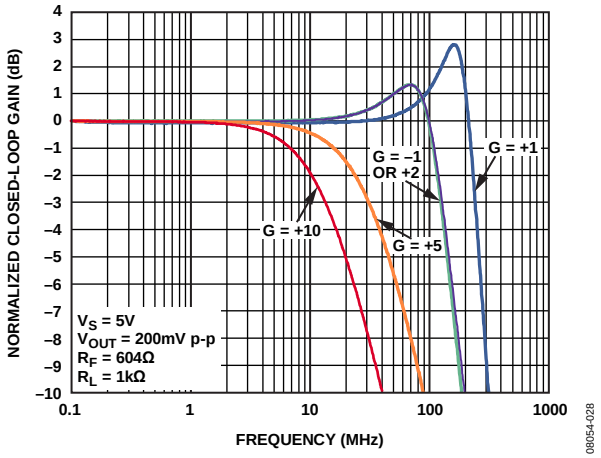


Figure 6. Small Signal Frequency Response vs. Gain, V_S = 5 V

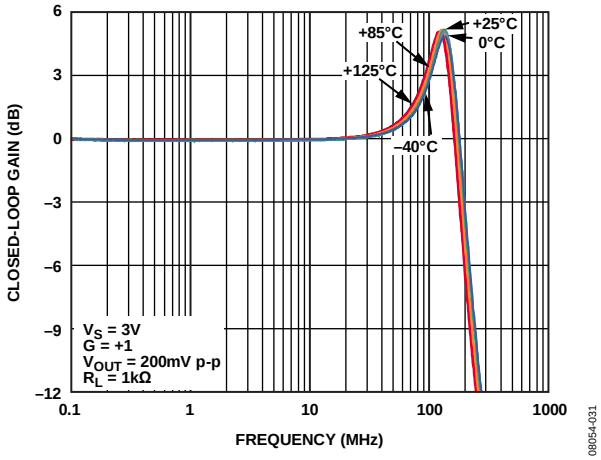


Figure 9. Small Signal Frequency Response vs. Temperature, V_S = 3 V

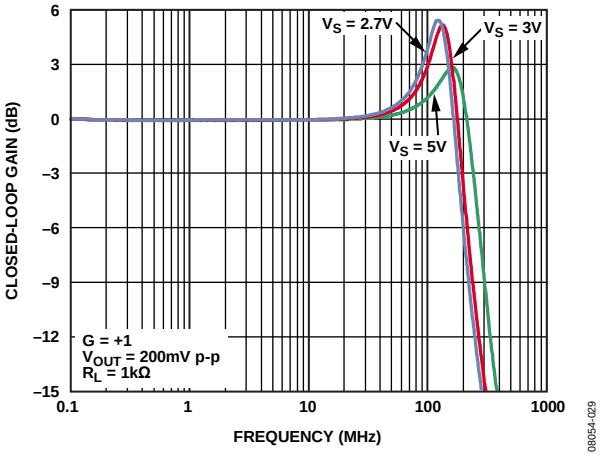


Figure 7. Small Signal Frequency Response vs. Supply Voltage

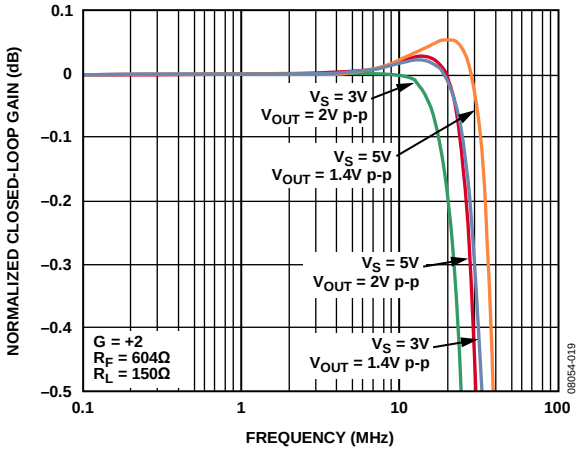


Figure 10. 0.1 dB Gain Flatness vs. Frequency, G = +2

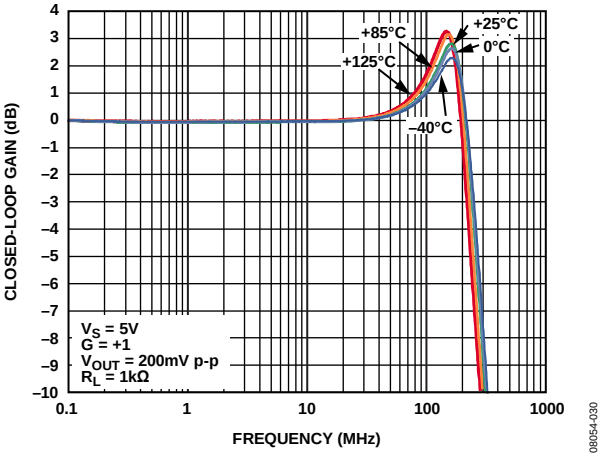


Figure 8. Small Signal Frequency Response vs. Temperature, V_S = 5 V

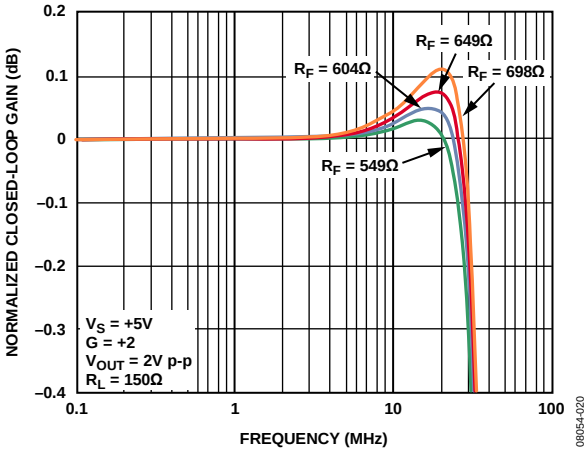


Figure 11. 0.1 dB Gain Flatness vs. R_F, V_S = 5 V

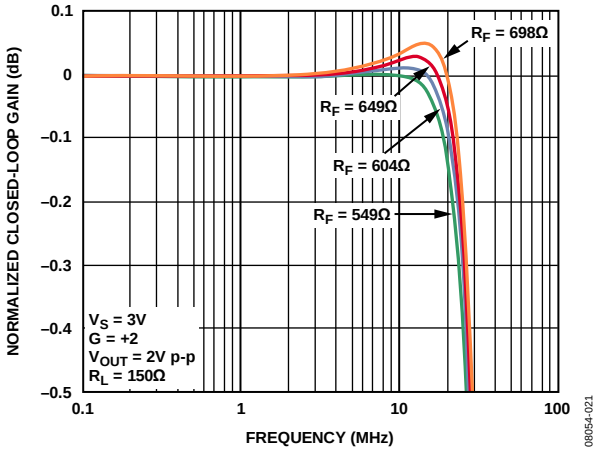


Figure 12. 0.1 dB Gain Flatness vs. R_F, V_S = 3 V

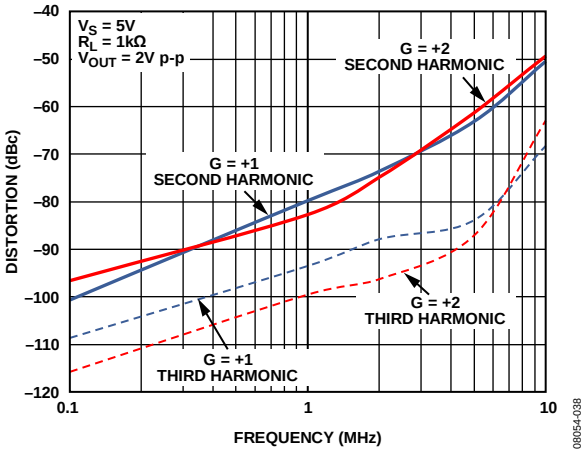


Figure 15. Harmonic Distortion (HD2, HD3) vs. Frequency, V_S = 5 V

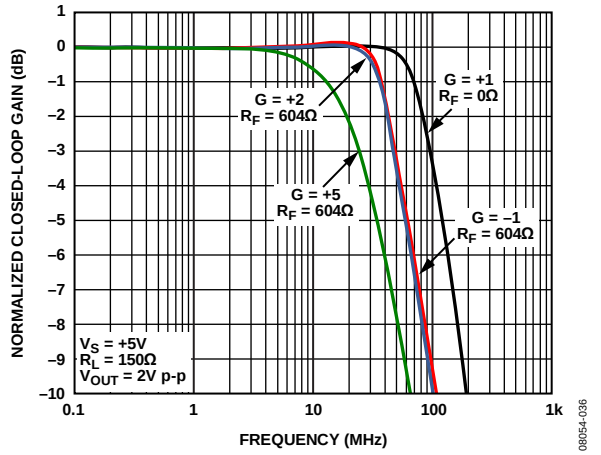


Figure 13. Large Signal Frequency Response vs. Gain, V_S = 5 V

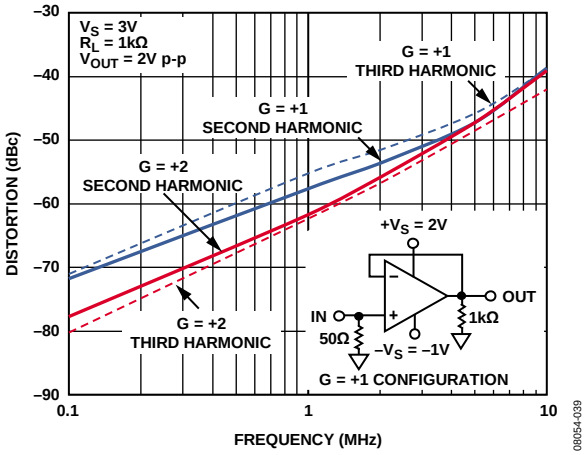


Figure 16. Harmonic Distortion (HD2, HD3) vs. Frequency, V_S = 3 V

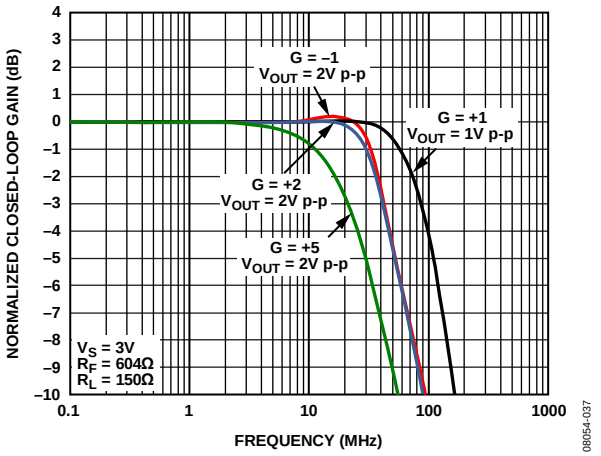


Figure 14. Large Signal Frequency Response vs. Gain, V_S = 3 V

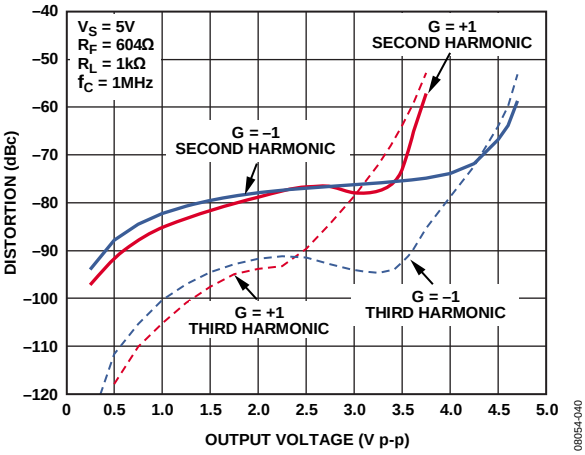


Figure 17. Harmonic Distortion vs. Output Voltage, V_S = 5 V

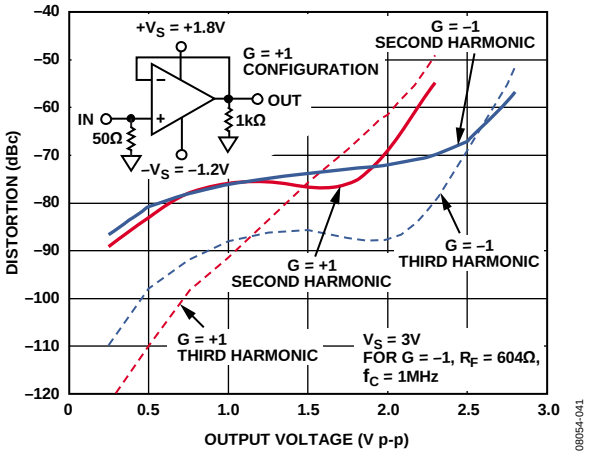


Figure 18. Harmonic Distortion vs. Output Voltage, V_S = 3 V

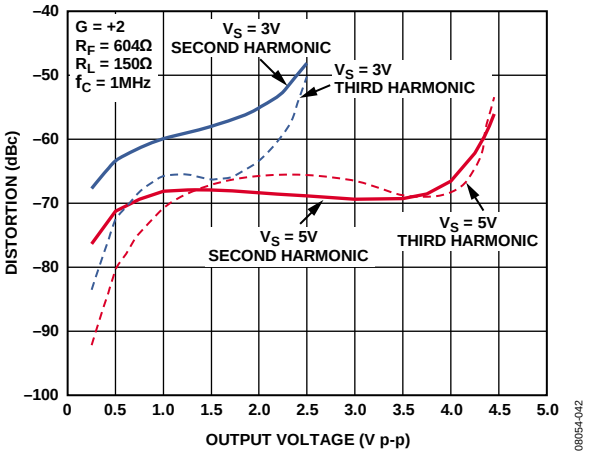


Figure 19. Harmonic Distortion vs. Output Voltage, G = +2

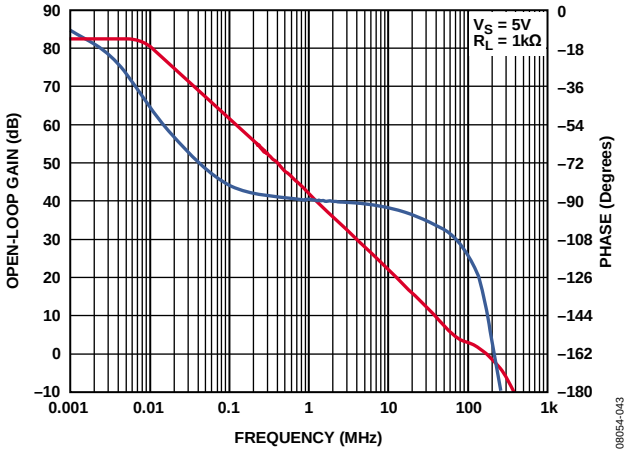


Figure 20. Open-Loop Gain and Phase vs. Frequency

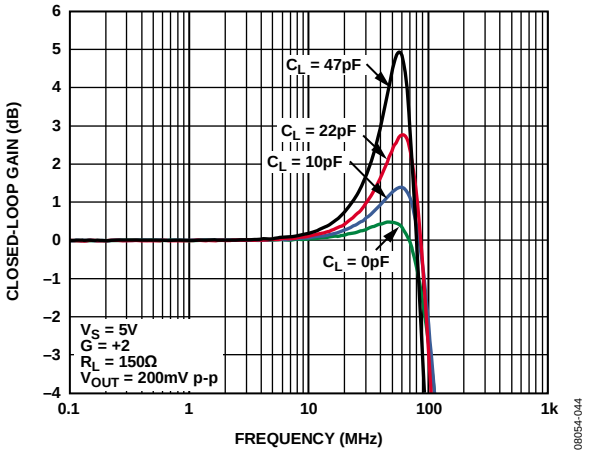


Figure 21. Small Signal Frequency Response vs. C_{LOAD} (C_L)

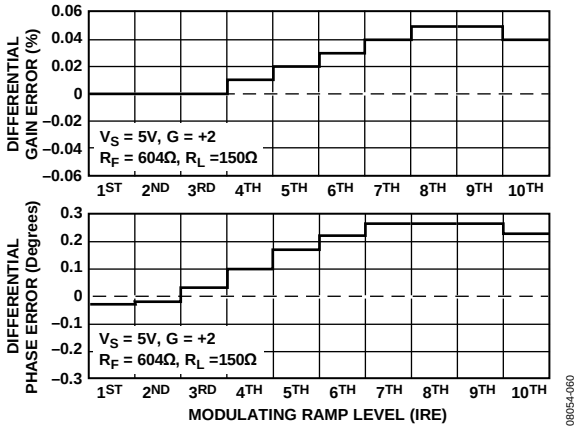


Figure 22. Differential Gain and Phase Errors

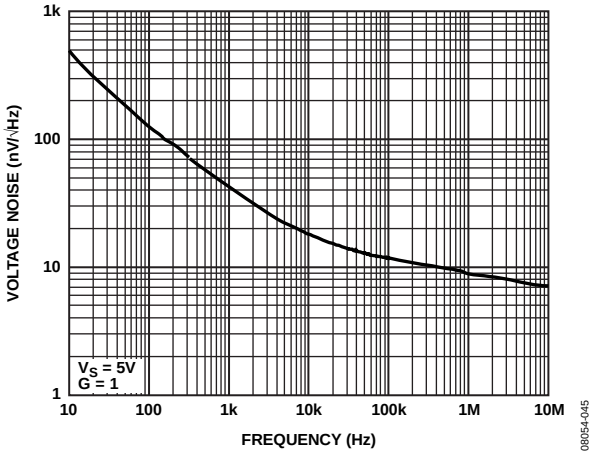


Figure 23. Input Voltage Noise vs. Frequency

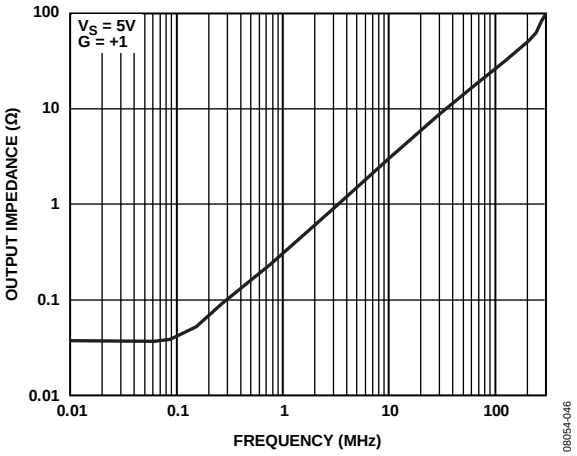


Figure 24. Closed-Loop Output Impedance vs. Frequency

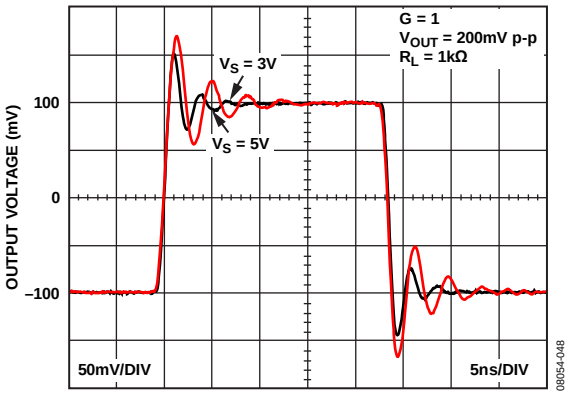


Figure 25. Small Signal Step Response, G = +1

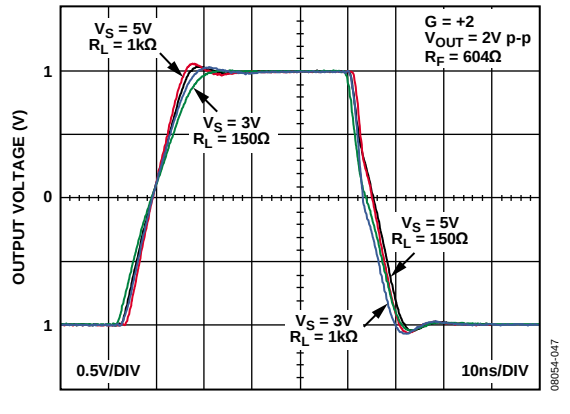


Figure 26. Large Signal Step Response, G = +2

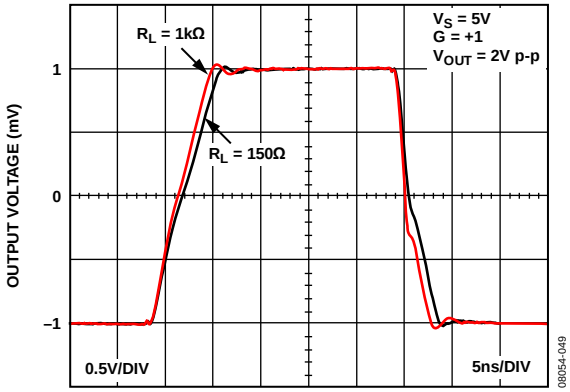


Figure 27. Large Signal Step Response, V_S = 5 V

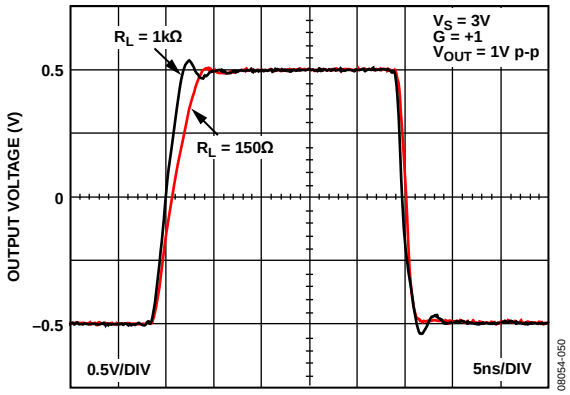


Figure 28. Large Signal Step Response, V_S = 3 V

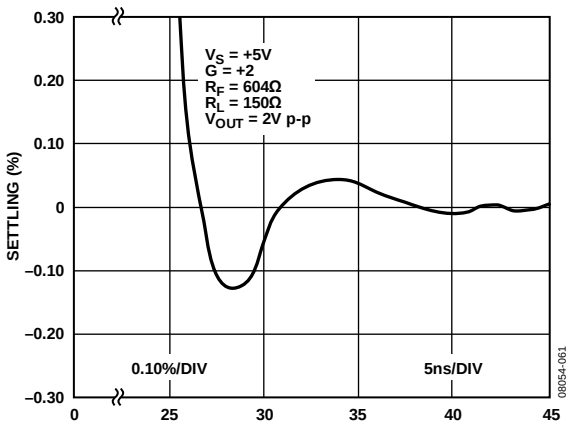


Figure 29. Short-Term Settling Time to 0.1%

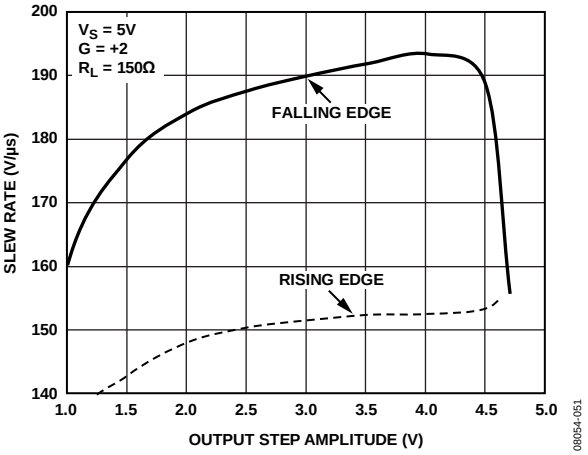


Figure 30. Slew Rate vs. Output Step

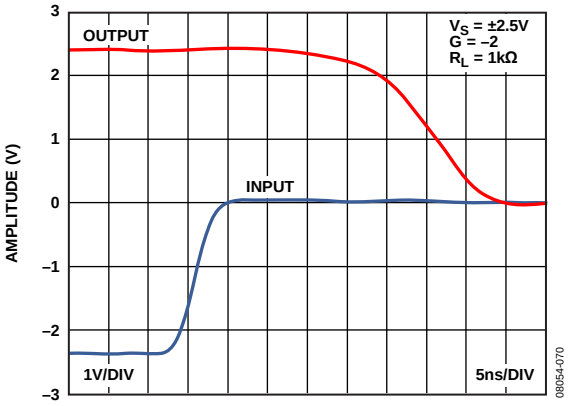


Figure 33. Output Overdrive Recovery from Positive Rail

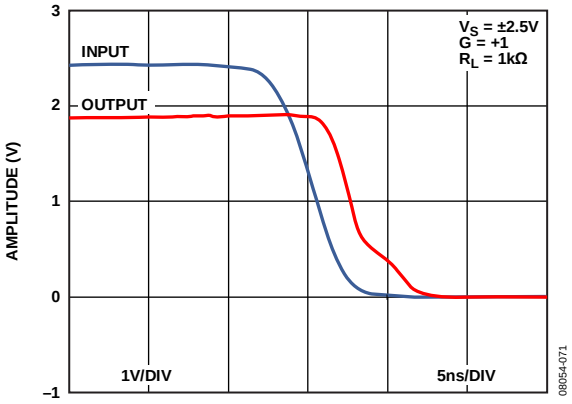


Figure 31. Input Overdrive Recovery From Positive Rail

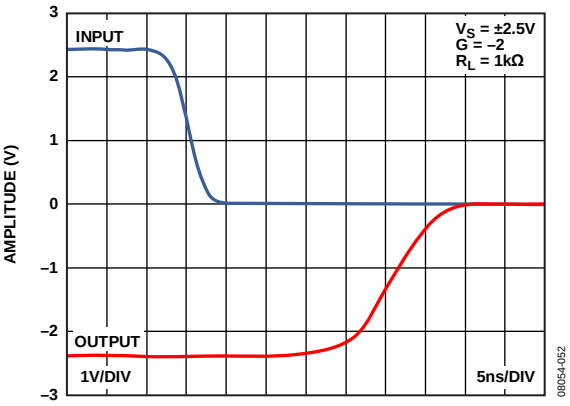


Figure 34. Output Overdrive Recovery from Negative Rail

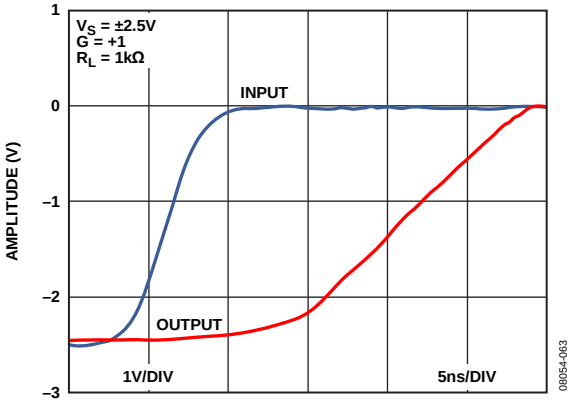


Figure 32. Input Overdrive Recovery from Negative Rail

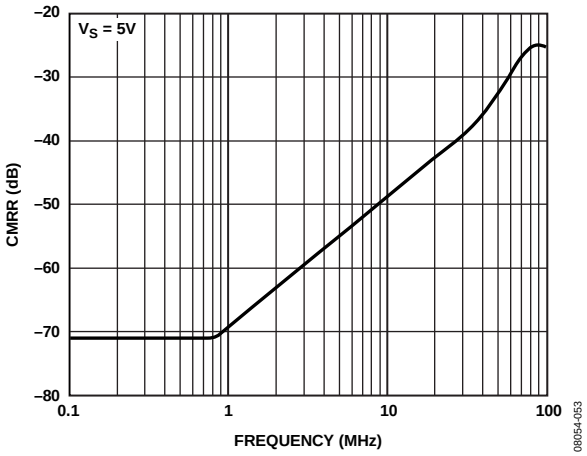


Figure 35. CMRR vs. Frequency

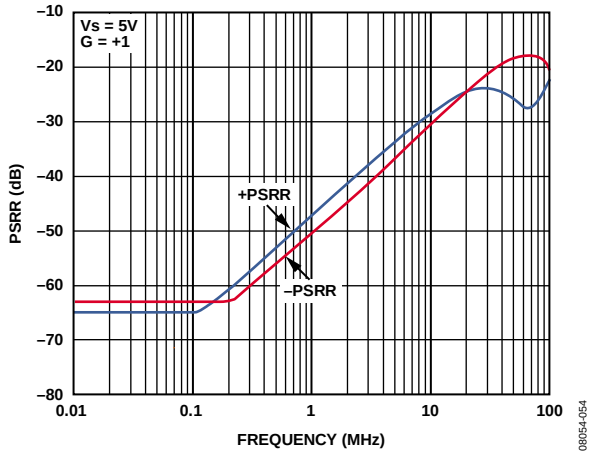


Figure 36. PSRR vs. Frequency

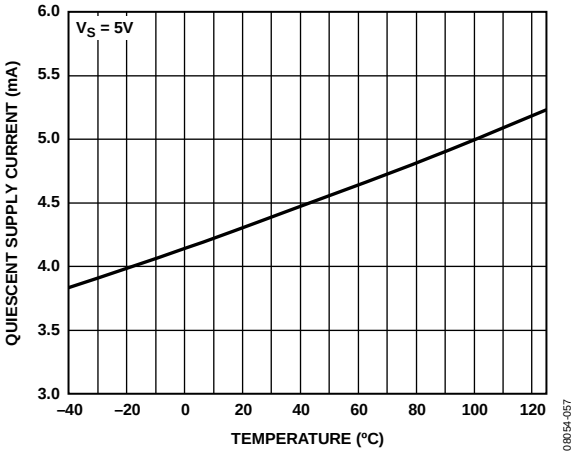


Figure 39. Supply Current per Amplifier vs. Temperature

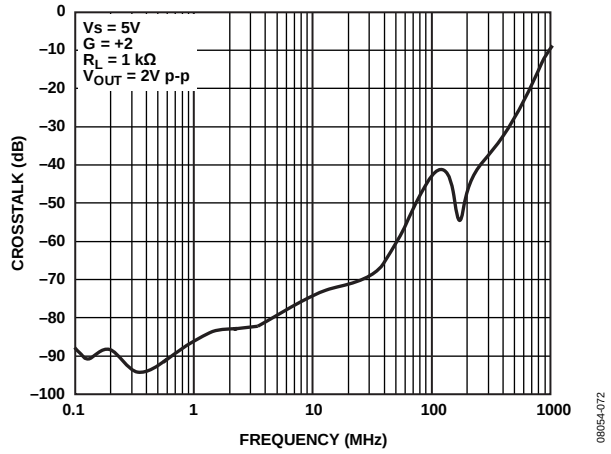


Figure 37. ADA4891-2 (SOIC) Crosstalk (Output-to-Output) vs. Frequency

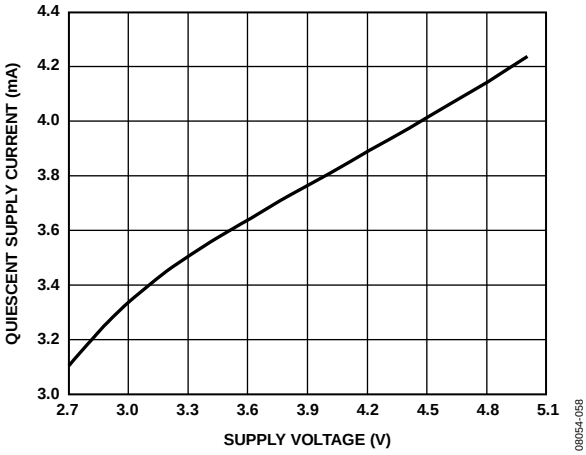


Figure 40. Supply Current per Amplifier vs. Supply Voltage

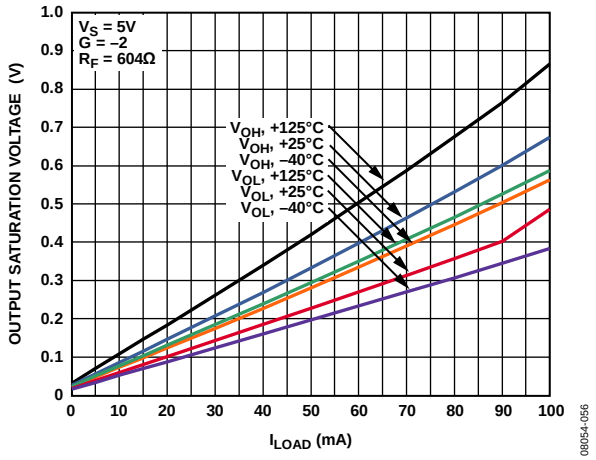


Figure 38. Output Saturation Voltage vs. Load Current vs. Temperature

APPLICATIONS INFORMATION

USING THE ADA4891

Understanding the subtleties of the ADA4891 family gives users insight into how to exact its peak performance. In this section, how the gain, component values, and parasitics affect the performance of the ADA4891 are discussed. The wideband, noninverting configuration of the ADA4891 is shown in Figure 41, while the wideband, inverting configuration of the ADA4891 is shown in Figure 42.

WIDEBAND, NONINVERTING OPERATION

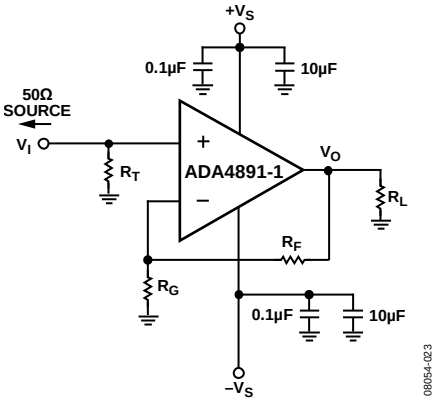


Figure 41. Noninverting Configuration

In Figure 41, R_F and R_G denote the feedback and the gain resistor, respectively. Together, R_F and R_G determine the noise gain of the amplifier, and the value of R_F defines the 0.1 dB bandwidth. The effect of R_F on the 0.1 dB gain flatness is discussed in the Effect of R_F on 0.1 dB Gain Flatness section. Typical R_F values range from 549 Ω to 698 Ω.

In a controlled impedance signal path, R_T is used as the input termination resistor designed to match that of the input source impedance. Note that it is not required for normal operation. R_T is generally set to match the input source impedance.

WIDEBAND, INVERTING GAIN OPERATION

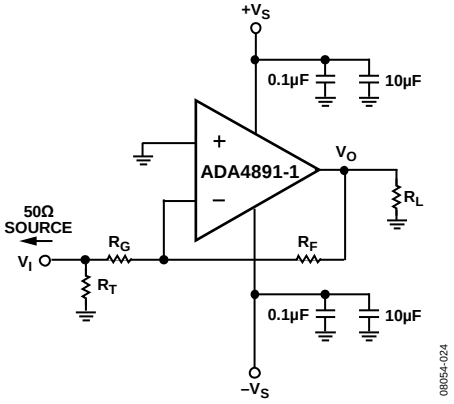


Figure 42. Inverting Configuration

Figure 42 shows the inverting gain configuration. To match the input source impedance for the inverting gain configuration, set the parallel combination of R_T//R_G to match that of the input source impedance.

Note that a bias current cancellation resistor is not required in the noninverting input of the amplifier because the input bias current of the ADA4891 is very low (less than 10 pA). Therefore, the dc errors caused by the bias current are negligible.

For both configurations, it is often useful to increase the R_F value to decrease the loading on the output. Increasing the R_F value improves the harmonic distortion at the expense of reducing the 0.1 dB bandwidth of the amplifier. This effect is discussed further in the Effect of R_F on 0.1 dB Gain Flatness section.

RECOMMENDED VALUES

Table 4 provides a handy reference for various configurations and shows the effect of gain on the −3 dB small signal bandwidth, slew rate, and peaking of the ADA4891-1/ADA4891-2. Note that as the gain increases, the small signal bandwidth decreases as is expected from the gain bandwidth product relationship. In addition, the phase margin improves with higher gains, and the amplifier becomes more stable. As a result, the peaking in the frequency response is reduced (see Figure 6).

Table 4. Recommended Values for the ADA4891-1/ADA4891-2 Performance

	Feedback Network Values		−3 dB Small Signal Bandwidth (MHz)	Slew Rate (V/µs)		
Gain	R_F	R_G	V_{OUT} = 200 mV p-p	t_R	t_F	Peaking (dB)
−1	604	604	118	188	192	1.3
+1	0	0	236	154	263	2.6
+2	604	604	120	178	204	1.4
+5	604	151	32.5	149	154	0
+10	604	67.1	12.7	71	72	0

EFFECT OF R_F ON 0.1 dB GAIN FLATNESS

Gain flatness is an important specification in video applications. It represents the maximum allowable deviation in the signal amplitude within the pass band. Tests have revealed that the human eye is unable to distinguish brightness variations of less than 1%, which translates into a 0.1 dB signal drop within the pass band, or put simply, 0.1 dB gain flatness.

The PCB layout configuration and bond pads of the chip often contribute to stray capacitance. The stray capacitance at the inverting input forms a pole with the feedback and gain resistor. This additional pole adds phase shift and reduces phase margin in the closed-loop phase response, causing instability in the amplifier and peaking in the frequency response.

Figure 43 shows the effect of using various values of Feedback Resistor R_F on the 0.1 dB gain flatness. Note that a larger R_F value causes more peaking because the additional pole formed by R_F, and the input stray capacitance, shifts down in frequency and interacts significantly with the internal poles of the amplifier.

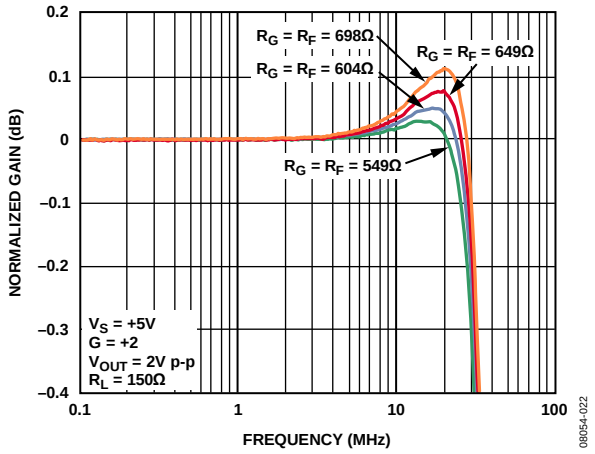


Figure 43. Noninverting Configuration

To get the desired 0.1 dB bandwidth, adjust the feedback resistor, R_F, as shown in Figure 43. If R_F cannot be adjusted, a small capacitor can be placed in parallel with R_F to reduce peaking.

The feedback capacitor, C_F, forms a zero with the feedback resistor, which cancels out the pole formed by the input stray capacitance and the gain and feedback resistor. For a first pass in determining the C_F value, use the equation $R_G \times C_S = R_F \times C_F$, where R_G is the gain resistor, C_S is the input stray capacitance, R_F is the feedback resistor, and C_F is the feedback capacitor. This is the condition where the original closed-loop frequency response of the amplifier is restored as if there is no stray input capacitance. Most often, however, the value of C_F is determined empirically.

Figure 44 shows the effect of using various values for the feedback capacitors to reduce peaking. In this case, $R_F = R_G = 604\ \Omega$. The input stray capacitance, together with the board parasitics, is approximately 2 pF.

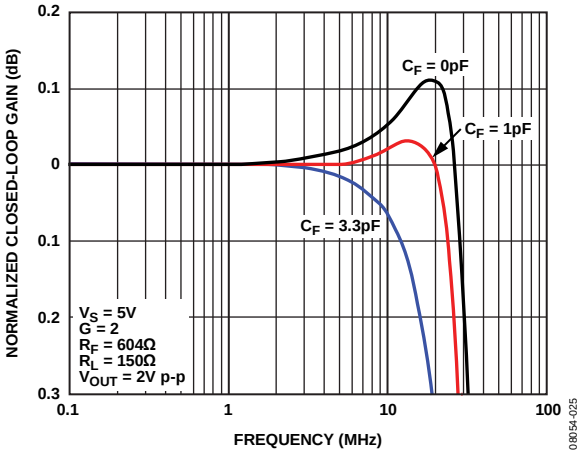


Figure 44. 0.1 dB Gain Flatness vs. C_F, V_S = 5 V

DRIVING CAPACITIVE LOADS

A highly capacitive load reacts with the output impedance of the amplifiers, causing a loss of phase margin and subsequent peaking or even oscillation, as is shown in Figure 45 and Figure 46. Four methods that minimize the output capacitive loading effect include:

- Reducing the output resistive load. This pushes the pole further away and, hence, improves the phase margin.
- Increase the phase margin with higher noise gains. As the closed-loop gain is increased, the larger phase margin allows for large capacitor loads with less peaking.
- Adding a parallel capacitor, C_F with R_F, from –IN to the output. This adds a zero in the closed-loop frequency response, which tends to cancel out the pole formed by the capacitive load and output impedance of the amplifier. Refer to the Effect of R_F on 0.1 dB Gain Flatness section for more details.
- Putting a small value resistor, R_S, in series with the output to isolate the load capacitor from the output stage of the amplifier.

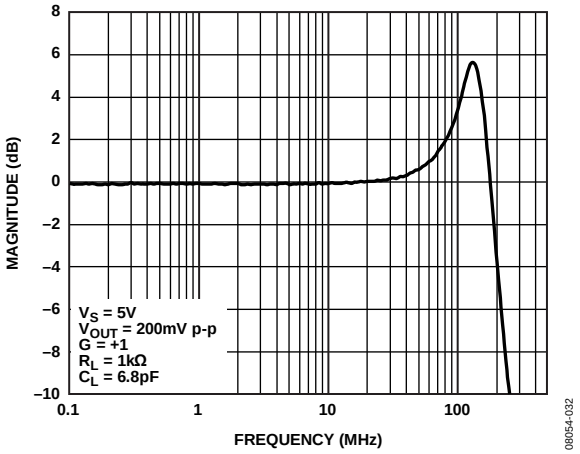


Figure 45. Closed-Loop Frequency Response, C_L = 6.8 pF

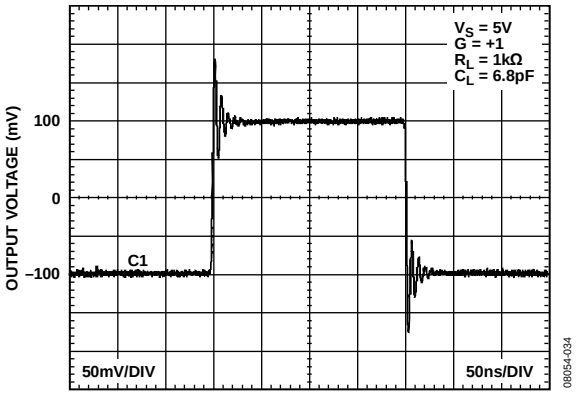


Figure 46. 200 mV Step Response, C_L = 6.8 pF

Figure 47 shows the effect of using a snub resistor (R_S) on reducing the peaking in the worst-case frequency response (gain of +1). Using R_S = 100 Ω reduces the peaking by 3 dB, with the tradeoff that the closed-loop gain is reduced by 0.9 dB due to attenuation at the output. R_S can be adjusted from 0 Ω to 100 Ω to maintain an acceptable level of peaking and closed-loop gain, as shown in Figure 48.

Figure 48 shows that the transient response is also much improved by the snub resistor R_S = 100 Ω, compared to that of Figure 46.

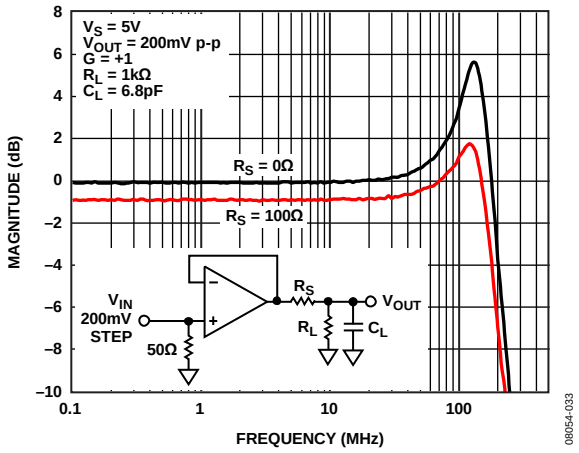


Figure 47. Capacitive Load Drive vs. Closed-Loop Gain

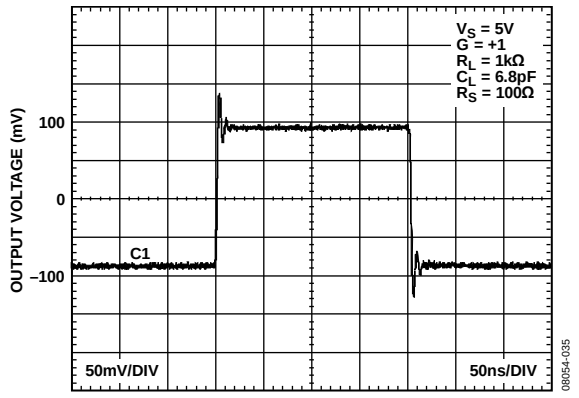


Figure 48. 200 mV Step Response, C_L = 50 pF

TERMINATING UNUSED AMPLIFIERS

Terminating unused amplifiers in a multiamplifier package is an important step to ensuring proper operation of the functional amplifier. Unterminated amplifiers can oscillate and draw excessive power if left unattended. The recommended procedure for terminating unused amplifiers is to connect any unused amplifiers in a unity-gain configuration and connect the noninverting input to midsupply voltage. With symmetrical bipolar power supplies, this means connecting the noninverting input to ground, as shown in Figure 49. In single power supply applications, a synthetic midsupply source must be created. This can be accomplished with a simple resistive voltage divider. Figure 50 shows the proper connection for terminating an unused amplifier in a single-supply configuration.

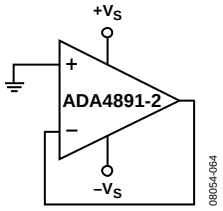


Figure 49. Terminating Unused Amplifier with Symmetrical Bipolar Power Supplies

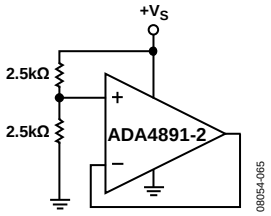


Figure 50. Terminating Unused Amplifier with Single Power Supply

VIDEO RECONSTRUCTION FILTER

A common application for active filters is at the output of video digital-to-analog converters (DACs)/encoders. The filter, or more appropriately, the video reconstruction filter, is used at the output of a video DAC/encoder to eliminate the multiple images that are created during the sampling process within the DAC. For portable video applications, the ADA4891 is an ideal choice due to its lower power requirements and high performance.

For active filters, a good rule of thumb is that the amplifiers −3 dB bandwidth be at least 10 times higher than the corner frequency of the filter. This ensures that no initial roll-off is introduced by the amplifier and that the pass band is flat until the cutoff frequency.

An example of a 15 MHz, 3-pole Sallen-Key, low-pass, video reconstruction filter is shown in Figure 51. This circuit features a gain of 2, has a 0.1 dB bandwidth of 7.3 MHz, and over 17 dB attenuation at 29.7 MHz (see Figure 52). The filter has three poles; two are active with a third passive pole (R6 and C4) placed at the output. C3 improves the filter roll-off. R6, R7, and R8 comprise the video load of 150 Ω. Components R6, C4, R7, R8, and the input termination of the network analyzer form a 6 dB attenuator; therefore, the reference level is roughly 0 dB, as shown in Figure 52.

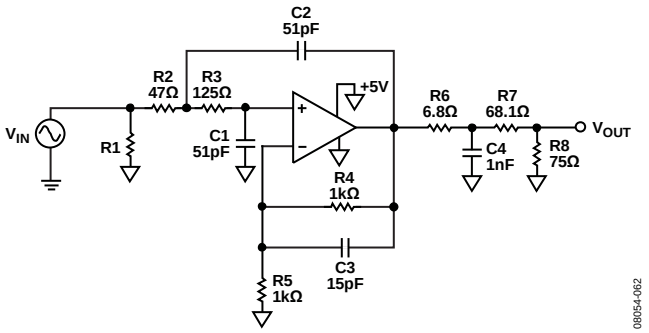


Figure 51. 13 MHz Video Reconstruction Filter Schematic

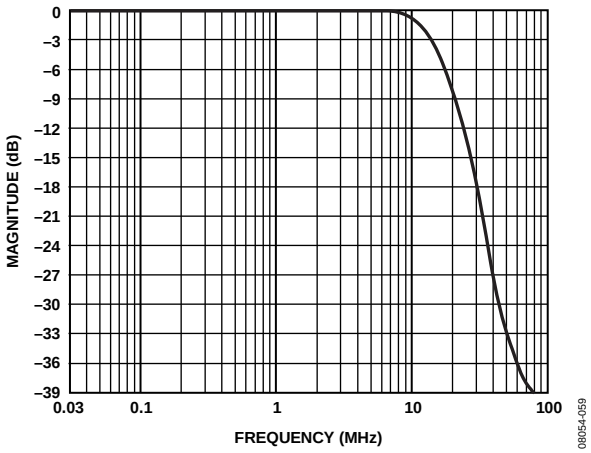


Figure 52. Video Reconstruction Filter Frequency Performance

LAYOUT, GROUNDING, AND BYPASSING

POWER SUPPLY BYPASSING

Power supply pins are additional op amp inputs, and care must be taken so that a noise-free stable dc voltage is applied. The purpose of bypass capacitors is to create a low impedance path from the supply to ground over a range of frequencies, thereby shunting or filtering the majority of the noise to ground. Bypassing is also critical for stability, frequency response, distortion, and PSRR performance.

Chip capacitors of 0.1 µF (X7R or NPO) are critical and should be as close as possible to the amplifier package. The 0508 case size for such a capacitor is recommended because it offers low series inductance and excellent high frequency performance. Larger chip capacitors, such as 0.1 µF capacitors, can be shared among a few closely spaced active components in the same signal path. A 10 µF tantalum capacitor is less critical for high frequency bypassing, but does provide additional bypassing for lower frequencies.

GROUNDING

When possible, ground and power planes should be used. Ground and power planes reduce the resistance and inductance of the power supply feeds and ground returns. If multiple planes are used, they should be stitched together with multiple vias. The returns for the input, output terminations, bypass capacitors, and R_G should all be kept as close to the ADA4891 as possible. Ground vias should be placed at the very end of the component mounting pads to provide a solid ground return. The output load ground and the bypass capacitor grounds should be returned to a common point on the ground plane to minimize parasitic inductance that can help improve distortion performance.

INPUT AND OUTPUT CAPACITANCE

Parasitic capacitance can cause peaking and instability and, therefore, should be minimized to ensure stable operation.

High speed amplifiers are sensitive to parasitic capacitance between the inputs and ground. A few picofarads of capacitance reduces the input impedance at high frequencies, in turn increasing the gain of the amplifier and causing peaking of the frequency response or even oscillations, if severe enough. It is recommended that the external passive components, which are connected to the input pins, be placed as close as possible to the inputs to avoid parasitic capacitance.

In addition, all ground and power planes under the pins of the ADA4891 should be cleared of copper to prevent parasitic capacitance between the input and output pins to ground. This is because a single mounting pad on a SOIC footprint can add as much as 0.2 pF of capacitance to ground if the ground or power plane is not cleared under the ADA4891 pins. In fact, the ground and power planes should be kept at a distance of at least 0.05 mm from the input pins on all layers of the board.

INPUT-TO-OUTPUT COUPLING

To minimize capacitive coupling between the inputs and output and to avoid any positive feedback, the input and output signal traces should not be parallel. In addition, the input traces should not be close to each other. A minimum of 7 mils between the two inputs is recommended.

LEAKAGE CURRENTS

In extremely low input bias current amplifier applications, stray leakage current paths must be kept to a minimum. Any voltage differential between the amplifier inputs and nearby traces sets up a leakage path through the PCB. Consider a 1 V signal and 100 GΩ to ground present at the input of the amplifier. The resultant leakage current is 10 pA; this is 5× the typical input bias current of the amplifier. Poor PCB layout, contamination, and the board material can create large leakage currents. Common contaminants on boards are skin oils, moisture, solder flux, and cleaning agents. Therefore, it is imperative that the board be thoroughly cleaned and the board surface be free of contaminants to take full advantage of the low input bias currents of the ADA4891.

To significantly reduce leakage paths, a guard-ring/shield should be used around the inputs. The guard-ring circles the input pins and is driven to the same potential as the input signal, thereby reducing the potential difference between pins. For the guard ring to be completely effective, it must be driven by a relatively low impedance source and should completely surround the input leads on all sides, above, and below, using a multilayer board (see Figure 53). The SOT-23-5 package presents a challenge in keeping the leakage paths to a minimum. The pin spacing is very tight, so extra care must be used when constructing the guard ring (see Figure 54 for recommended guard-ring construction).

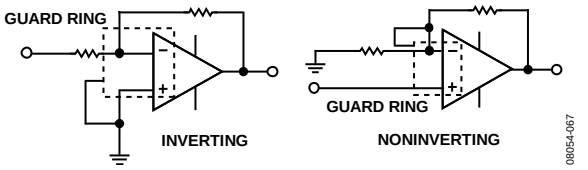


Figure 53. Guard-Ring Configurations

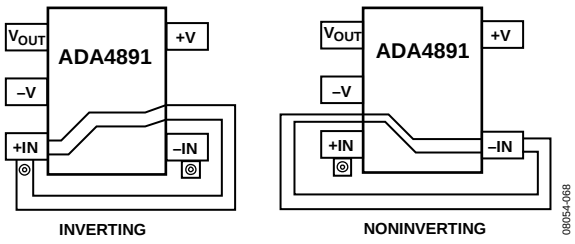
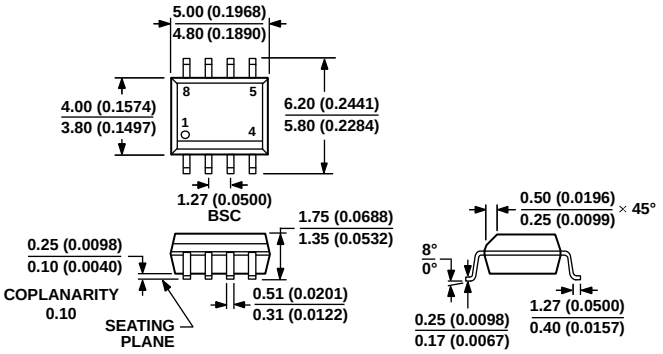


Figure 54. Guard-Ring Layout SOT-23-5

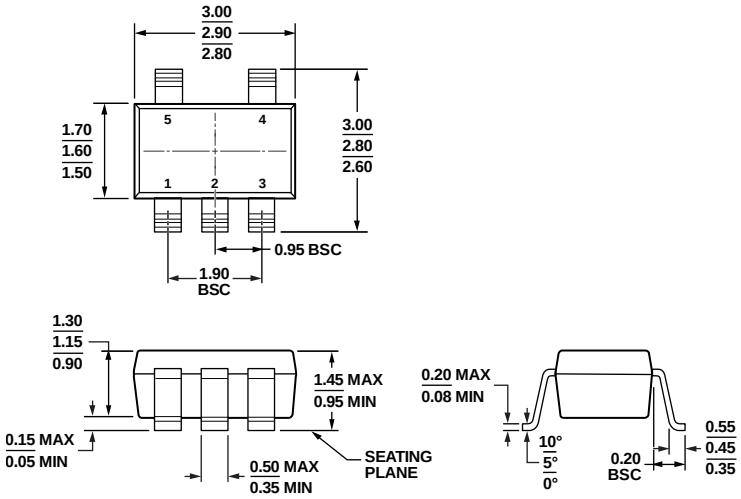
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 55. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-178-AA

121608-A

Figure 56. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters

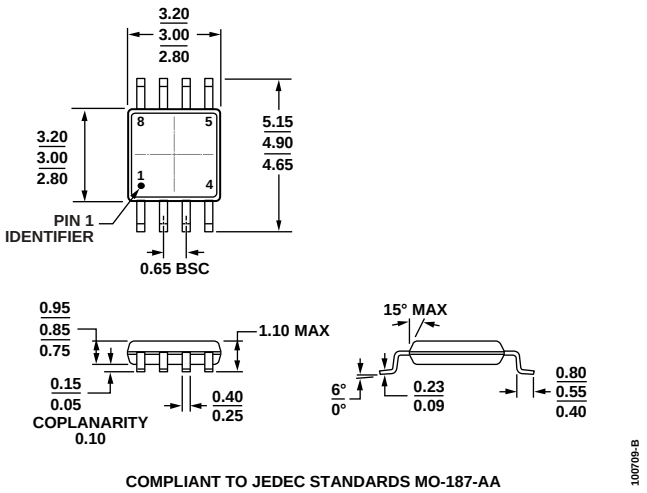


Figure 57. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4891-1ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4891-1ARZ-RL	−40°C to +125°C	8-Lead SOIC_N, 13″ Tape and Reel	R-8	
ADA4891-1ARZ-R7	−40°C to +125°C	8-Lead SOIC_N, 7″ Tape and Reel	R-8	
ADA4891-1ARJZ-R7	−40°C to +125°C	5-Lead SOT-23, 7″ Tape and Reel	RJ-5	H1W
ADA4891-1ARJZ-RL	−40°C to +125°C	5-Lead SOT-23, 13″ Tape and Reel	RJ-5	H1W
ADA4891-2ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4891-2ARZ-RL	−40°C to +125°C	8-Lead SOIC_N, 13″ Tape and Reel	R-8	
ADA4891-2ARZ-R7	−40°C to +125°C	8-Lead SOIC_N, 7″ Tape and Reel	R-8	
ADA4891-2ARMZ	−40°C to +125°C	8-Lead MSOP	RM-8	H1U
ADA4891-2ARMZ-RL	−40°C to +125°C	8-Lead MSOP, 13" Tape and Reel	RM-8	H1U
ADA4891-2ARMZ-R7	−40°C to +125°C	8-Lead MSOP, 7" Tape and Reel	RM-8	H1U

[1] Z = RoHS Compliant Part.

NOTES

NOTES