Data Sheet | January 23, 2006 | FN4152.4

Quad, 350MHz, Low Power, Programmable Gain Buffer Amplifier

The HFA1412 is a quad closed loop Buffer featuring user programmable gain and high speed video performance.

A unique feature of the HFA1412's pinout allows the user to select a voltage gain of +1, -1, or +2 (see the "Application Information" section). The on-chip gain setting resistors eliminate eight external resistors, thus saving board space or freeing up space for termination resistors. The on-chip feedback resistor is preset at the optimum value, and also eliminates worries about parasitic feedback capacitance. Additionally, the capacitance sensitive summing node is buried inside the package where it is unaffected by PCB parasitics. Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.

The HFA1412 is an excellent choice for component and composite video systems as indicated by the excellent gain flatness, and 0.03%/0.02 Degree Differential Gain/Phase specifications (R_L = 150Ω). Its ability to deliver a gain of +2 with no external resistors makes it particularly desirable for applications driving double terminated cables.

For Military product, refer to the HFA1412/883 data sheet.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HFA1412IP	HFA1412IP	-40 to 85	14 Ld PDIP	E14.3
HFA1412IPZ (Note)	HFA1412IPZ	-40 to 85	14 Ld PDIP* (Pb-free)	E14.3
HFA1412IB	HFA1412IB	-40 to 85	14 Ld SOIC	M14.15
HFA1412IBZ (Note)	HFA1412IBZ	-40 to 85	14 Ld SOIC (Pb-free)	M14.15
HA5025EVAL		DIP Evaluation Board For Quad Op Amp		

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

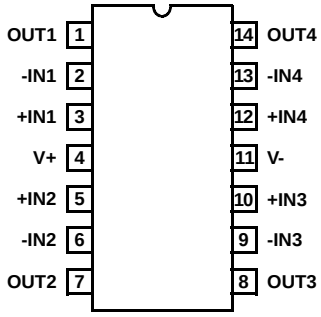
- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Wide -3dB Bandwidth 350MHz
- Low Supply Current 6mA/Buffer
- Excellent Gain Flatness (to 100MHz) . . . . . ±0.08dB
- Low Differential Gain and Phase . . . . 0.03%/0.02 Degree
- Very Fast Slew Rate 1650V/µs
- Fast Settling Time (0.1%) 28ns
- High Output Current 55mA
- Excellent Gain Accuracy 0.99V/V
- Overdrive Recovery . . . . . <10ns
- Standard Operational Amplifier Pinout
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

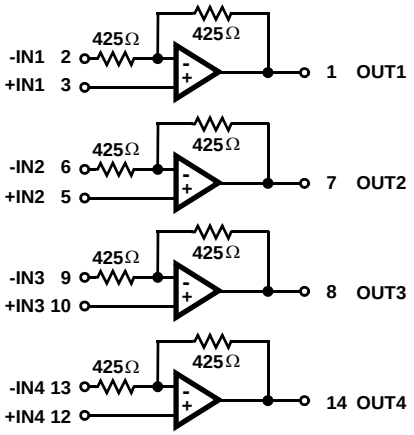
- Video Distribution Amps
- Flash A/D Drivers
- Video Cable Drivers
- Video Switchers and Routers
- Medical Imaging Systems
- RGB Video Processing
- High Speed Oscilloscopes and Analyzers

Pinout

HFA1412 (PDIP, SOIC)
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . . V_{SUPPLY}
Output Current (Note 1) . . . . . Short Circuit Protected
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 600V

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package*	100
SOIC Package	120

Maximum Junction Temperature (Die) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC-Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 30mA for maximum reliability.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Output Offset Voltage		A	25	-	2	10	mV
		A	Full	-	3	15	mV
Average Output Offset Voltage Drift		B	Full	-	22	70	µV/°C
Channel-to-Channel Output Offset Voltage Mismatch		A	25	-	-	15	mV
		A	Full	-	-	30	mV
Common-Mode Rejection Ratio	ΔV_{CM} = ±1.8V	A	25	42	45	-	dB
	ΔV_{CM} = ±1.8V	A	85	40	44	-	dB
	ΔV_{CM} = ±1.2V	A	-40	40	45	-	dB
Power Supply Rejection Ratio	ΔV_{PS} = ±1.8V	A	25	45	49	-	dB
	ΔV_{PS} = ±1.8V	A	85	43	48	-	dB
	ΔV_{PS} = ±1.2V	A	-40	43	48	-	dB
Non-Inverting Input Bias Current		A	25	-	1	15	µA
		A	Full	-	3	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	30	80	nA/°C
Channel-to-Channel Non-Inverting Input Bias Current Mismatch		A	25	-	-	15	µA
		A	Full	-	-	25	µA
Non-Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.25V	A	25	-	0.5	1	µA/V
		A	Full	-	-	3	µA/V
Non-Inverting Input Resistance	ΔV_{CM} = ±1.8V	A	25	0.8	1.1	-	MΩ
	ΔV_{CM} = ±1.8V	A	85	0.5	1.4	-	MΩ
	ΔV_{CM} = ±1.2V	A	-40	0.5	1.3	-	MΩ
Inverting Input Resistance		C	25	-	425	-	Ω
Input Capacitance (either input)		C	25	-	2	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR and $+R_{IN}$ tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density (Note 4)	f = 100kHz	B	25	-	7	-	nV/√Hz

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
Non-Inverting Input Noise Current Density (Note 4)	f = 100kHz	B	25	-	3	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Gain (V_{IN} = -1V to +1V)	A_V = -1	A	25	-0.98	-0.996	-1.02	V/V
		A	Full	-0.975	-1.000	-1.025	V/V
	A_V = +1	A	25	0.98	0.992	1.02	V/V
		A	Full	0.975	0.993	1.025	V/V
	A_V = +2	A	25	1.96	1.988	2.04	V/V
		A	Full	1.95	1.990	2.05	V/V
Channel-to-Channel Gain Mismatch	A_V = -1	A	25	-	-	±0.02	V/V
		A	Full	-	-	±0.025	V/V
	A_V = +1	A	25	-	-	±0.025	V/V
		A	Full	-	-	±0.025	V/V
	A_V = +2	A	25	-	-	±0.04	V/V
		A	Full	-	-	±0.05	V/V
AC CHARACTERISTICS							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Note 4)	A_V = -1	B	25	200	320	-	MHz
		B	Full	190	280	-	MHz
	A_V = +1, $+R_S$ = 620Ω	B	25	160	230	-	MHz
		B	Full	150	210	-	MHz
	A_V = +2	B	25	220	350	-	MHz
		B	Full	190	300	-	MHz
Full Power Bandwidth (V_{OUT} = 5V_{P-P} at A_V = +2 or -1, V_{OUT} = 4V_{P-P} at A_V = +1, Note 4)	A_V = -1	B	25	-	225	-	MHz
	A_V = +1, $+R_S$ = 620Ω	B	25	-	190	-	MHz
	A_V = +2	B	25	-	160	-	MHz
Gain Flatness (V_{OUT} = 0.2V_{P-P}, Note 4)	A_V = +1, to 25MHz, $+R_S$ = 620Ω	B	25	-	±0.10	±0.18	dB
		B	Full	-	±0.12	±0.20	dB
	A_V = -1, to 50MHz	B	25	-	±0.06	±0.10	dB
		B	Full	-	±0.08	±0.16	dB
	A_V = -1, to 100MHz	B	25	-	±0.08	±0.20	dB
		B	Full	-	±0.13	±0.30	dB
	A_V = +2, to 50MHz	B	25	-	±0.05	±0.09	dB
		B	Full	-	±0.06	±0.10	dB
	A_V = +2, to 100MHz	B	25	-	±0.08	±0.16	dB
		B	Full	-	±0.16	±0.30	dB
Crosstalk (All Channels Hostile, Note 4)	5MHz	B	25	-	-53	-	dB
	10MHz	B	25	-	-50	-	dB
OUTPUT CHARACTERISTICS							
Output Voltage Swing (Note 4)	A_V = -1	A	25	±3.0	±3.2	-	V
		A	Full	±2.8	±3.0	-	V

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
Output Current (Note 4)	A_V = -1, R_L = 50Ω	A	25, 85	50	55	-	mA
		A	-40	28	42	-	mA
Output Short Circuit Current		B	25	-	100	-	mA
DC Closed Loop Output Impedance	A_V = +2	B	25	-	0.2	-	Ω
Second Harmonic Distortion (A_V = +2, V_{OUT} = $2V_{P-P}$, Note 4)	10MHz	B	25	-47	-50	-	dBc
		B	Full	-45	-48	-	dBc
	20MHz	B	25	-40	-43	-	dBc
		B	Full	-39	-41	-	dBc
Third Harmonic Distortion (A_V = +2, V_{OUT} = $2V_{P-P}$, Note 4)	10MHz	B	25	-55	-60	-	dBc
		B	Full	-55	-60	-	dBc
	20MHz	B	25	-46	-53	-	dBc
		B	Full	-46	-50	-	dBc
Reverse Isolation (S_{12}, Note 4)	30MHz, A_V = +2	B	25	-	-65	-	dB
TRANSIENT RESPONSE A_V = +2, Unless Otherwise Specified							
Rise and Fall Times (V_{OUT} = $0.5V_{P-P}$)	Rise Time	B	25	-	1.0	-	ns
	Fall Time	B	25	-	1.25	-	ns
Overshoot (V_{OUT} = $0.5V_{P-P}$, V_{IN} t_{RISE} = 500ps, Notes 4, 5)	+OS	B	25	-	3	-	%
	-OS	B	25	-	9	-	%
Slew Rate (V_{OUT} = $5V_{P-P}$ at A_V = +2 or -1, V_{OUT} = $4V_{P-P}$ at A_V = +1)	A_V = -1	B	25	1150	1700	-	V/µs
		B	Full	1100	1650	-	V/µs
	A_V = +1, $+R_S$ = 620Ω	B	25	700	1000	-	V/µs
		B	Full	650	950	-	V/µs
	A_V = +2	B	25	900	1250	-	V/µs
		B	Full	800	1150	-	V/µs
Settling Time (V_{OUT} = +2V to 0V Step, Note 4)	To 0.1%	B	25	-	28	-	ns
	To 0.05%	B	25	-	33	-	ns
	To 0.02%	B	25	-	38	-	ns
Overdrive Recovery Time	V_{IN} = ±2V	B	25	-	8.5	-	ns
VIDEO CHARACTERISTICS							
Differential Gain (f = 3.58MHz, A_V = +2)	R_L = 150Ω	B	25	-	0.03	-	%
	R_L = 75Ω	B	25	-	0.05	-	%
Differential Phase (f = 3.58MHz, A_V = +2)	R_L = 150Ω	B	25	-	0.02	-	Degrees
	R_L = 75Ω	B	25	-	0.05	-	Degrees
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V
Power Supply Current (Note 4)		A	25	-	5.9	6.1	mA/Op Amp
		A	Full	-	6.1	6.3	mA/Op Amp

NOTES:

3. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
4. See Typical Performance Curves for more information.
5. Negative overshoot dominates for output signal swings below GND (e.g. $0.5V_{P-P}$), yielding a higher overshoot limit compared to the V_{OUT} = 0V to 0.5V condition. See the “Application Information” section for details.

Application Information

HFA1412 Advantages

The HFA1412 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space. Implementing a quad, gain of 2, cable driver with this IC eliminates the eight gain setting resistors, which frees up board space for termination resistors.

Like most newer high performance amplifiers, the HFA1412 is a current feedback amplifier (CFA). CFAs offer high bandwidth and slew rate at low supply currents, but can be difficult to use because of their sensitivity to feedback capacitance and parasitics on the inverting input (summing node). The HFA1412 eliminates these concerns by bringing the gain setting resistors on-chip. This yields the optimum placement and value of the feedback resistor, while minimizing feedback and summing node parasitics. Because there is no access to the summing node, the PCB parasitics do not impact performance at gains of +2 or -1 (see “Unity Gain Considerations” for discussion of parasitic impact on unity gain performance).

The HFA1412’s closed loop gain implementation provides better gain accuracy, lower offset and output impedance, and better distortion compared with open loop buffers.

Closed Loop Gain Selection

This “buffer” operates in closed loop gains of -1, +1, or +2, with gain selection accomplished via connections to the ±inputs. Applying the input signal to +IN and floating -IN selects a gain of +1 (see next section for layout caveats), while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded through a 50Ω resistor.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT	-INPUT
-1	50Ω to GND	Input
+1	Input	NC (Floating)
+2	Input	GND

Unity Gain Considerations

Unity gain selection is accomplished by floating the -Input of the HFA1412. Anything that tends to short the -Input to GND, such as stray capacitance at high frequencies, will cause the amplifier gain to increase toward a gain of +2. The result is excessive high frequency peaking, and possible instability. Even the minimal amount of capacitance associated with attaching the -Input lead to the PCB results in approximately 6dB of gain peaking. At a minimum this requires due care to ensure the minimum capacitance at the -Input connection.

Table 1 lists five alternate methods for configuring the HFA1412 as a unity gain buffer, and the corresponding performance. The implementations vary in complexity and involve performance trade-offs. The easiest approach to implement is simply shorting the two input pins together, and applying the input signal to this common node. The amplifier bandwidth decreases from 550MHz to 370MHz, but excellent gain flatness is the benefit. A drawback to this approach is that the amplifier input noise voltage and input offset voltage terms see a gain of +2, resulting in higher noise and output offset voltages. Alternately, a 100pF capacitor between the inputs shorts them only at high frequencies, which prevents the increased output offset voltage but delivers less gain flatness.

Another straightforward approach is to add a 620Ω resistor in series with the amplifier’s positive input. This resistor and the HFA1412 input capacitance form a low pass filter which rolls off the signal bandwidth before gain peaking occurs. This configuration was employed to obtain the data sheet AC and transient parameters for a gain of +1.

Pulse Overshoot

The HFA1412 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased overshoot on the negative portion of the output waveform (see Figure 5, Figure 7, and Figure 9). This overshoot isn’t present for small bipolar signals (see Figure 4, Figure 6, and Figure 8) or large positive signals. Figure 28 through Figure 31 illustrate the amplifier’s overshoot dependency on input transition time, and signal polarity.

TABLE 1. UNITY GAIN PERFORMANCE FOR VARIOUS IMPLEMENTATIONS

APPROACH	PEAKING (dB)	BW (MHz)	SR (V/µs)	±0.1dB GAIN FLATNESS (MHz)
Remove -IN Pin	5.0	550	1300	18
$+R_S$ = 620Ω	1.0	230	1000	25
$+R_S$ = 620Ω and Remove -IN Pin	0.7	225	1000	28
Short +IN to -IN (e.g., Pins 2 and 3)	0.1	370	500	170
100pF Capacitor Between +IN and -IN	0.3	380	550	130

PC Board Layout

This amplifier's frequency response depends greatly on the care taken in designing the PC board (PCB). **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

An example of a good high frequency layout is the Evaluation Board shown in Figure 3.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 350MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth decreases as the load capacitance increases. For example, at A_V = +2, R_S = 22Ω, C_L = 100pF, the overall bandwidth is 125MHz, and bandwidth drops to 100MHz at R_S = 12Ω, C_L = 220pF.

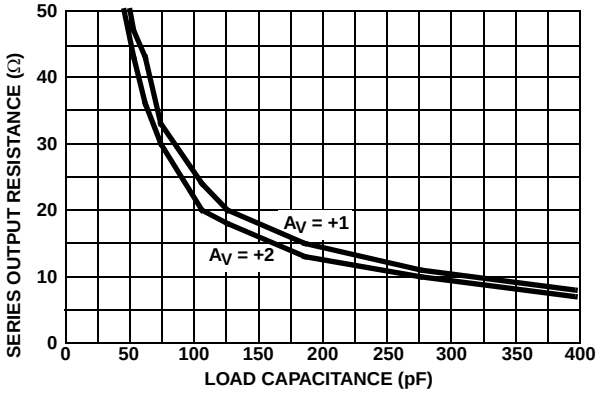


FIGURE 1. RECOMMENDED SERIES RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1412 may be evaluated using the HA5025 Evaluation Board, slightly modified as follows:

1. Remove the four feedback resistors, and leave the connections open.
2. a. For A_V = +1 evaluation, remove the gain setting resistors (R_1), and leave pins 2, 6, 9, and 13 floating.
   b. For A_V = +2, replace the gain setting resistors (R_1) with 0Ω resistors to GND.
3. Replace the 0Ω series output resistors with 50Ω.

The modified schematic for amplifier 1, and the board layout are shown in Figures 2 and 3.

To order evaluation boards (part number HA5025EVAL), please contact your local sales office.

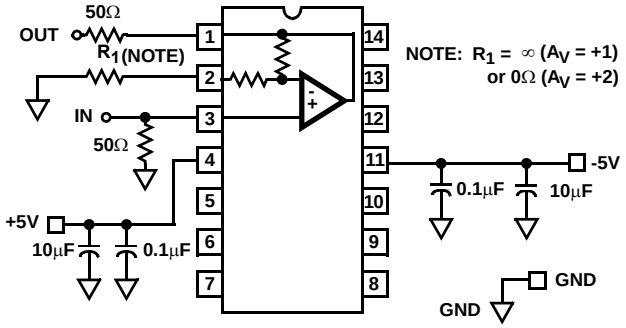


FIGURE 2. MODIFIED EVALUATION BOARD SCHEMATIC

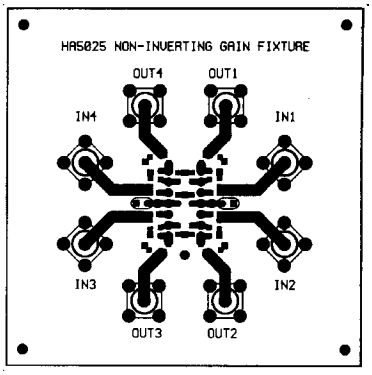


FIGURE 3A. TOP LAYOUT

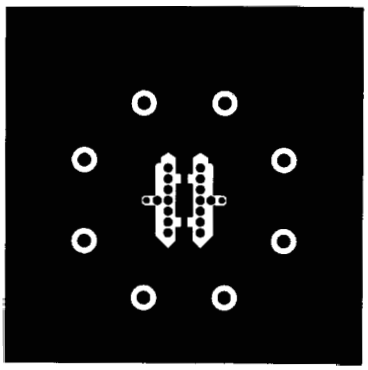


FIGURE 3B. BOTTOM LAYOUT

FIGURE 3. EVALUATION BOARD LAYOUT

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25°C$, $R_L = 100\Omega$, Unless Otherwise Specified

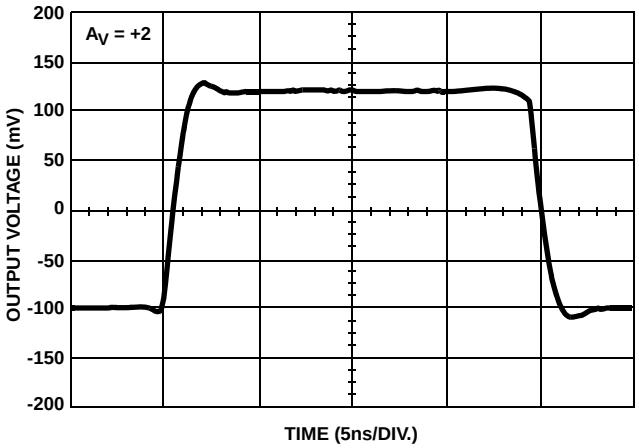


FIGURE 4. SMALL SIGNAL PULSE RESPONSE

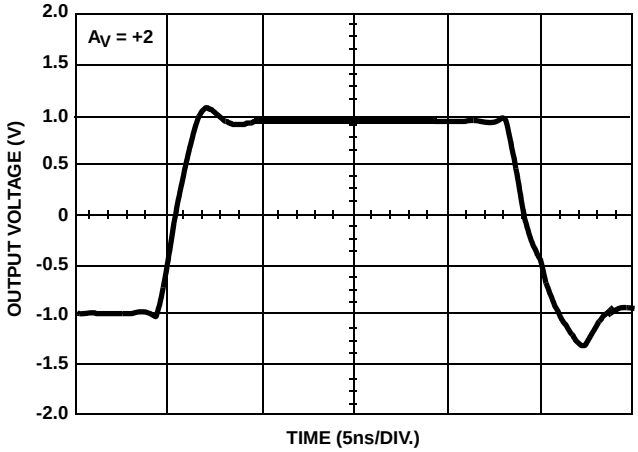


FIGURE 5. LARGE SIGNAL PULSE RESPONSE

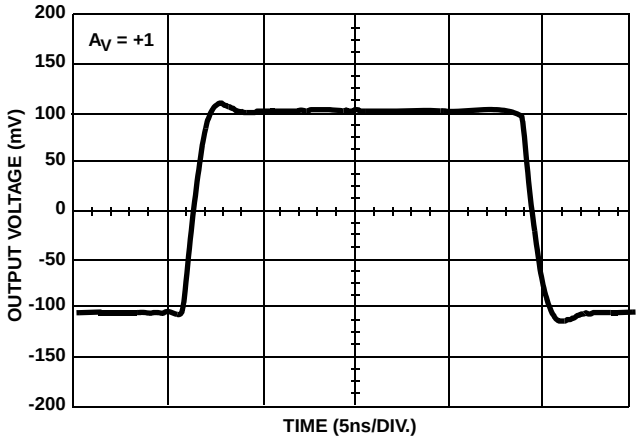


FIGURE 6. SMALL SIGNAL PULSE RESPONSE

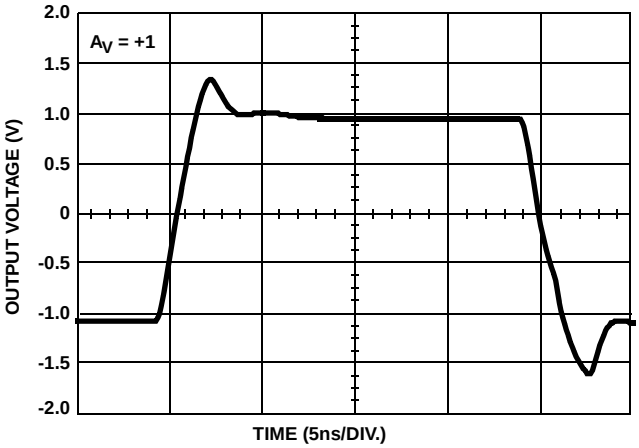


FIGURE 7. LARGE SIGNAL PULSE RESPONSE

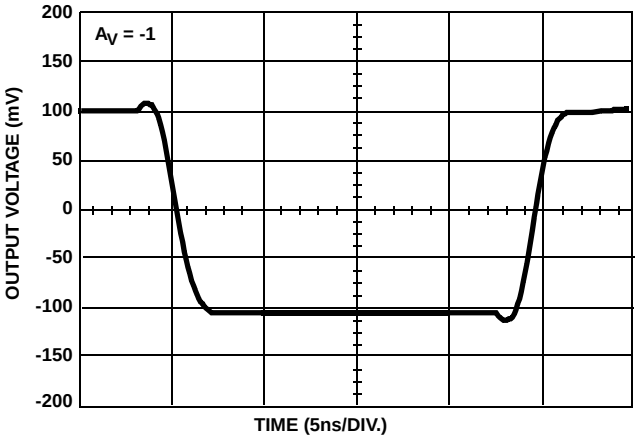


FIGURE 8. SMALL SIGNAL PULSE RESPONSE

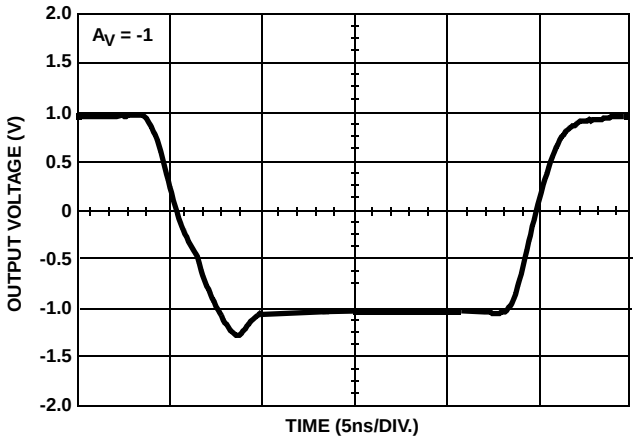


FIGURE 9. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25°C$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

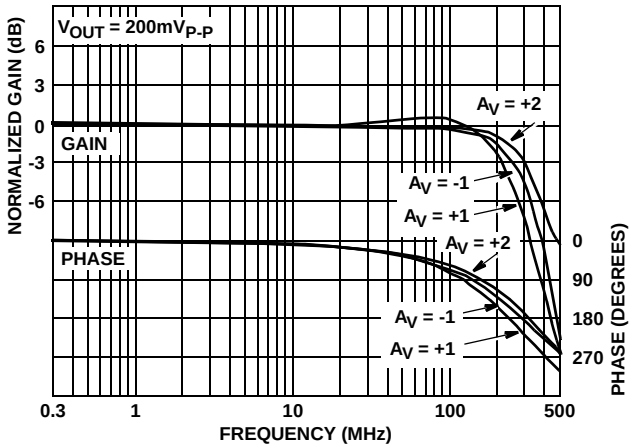


FIGURE 10. FREQUENCY RESPONSE

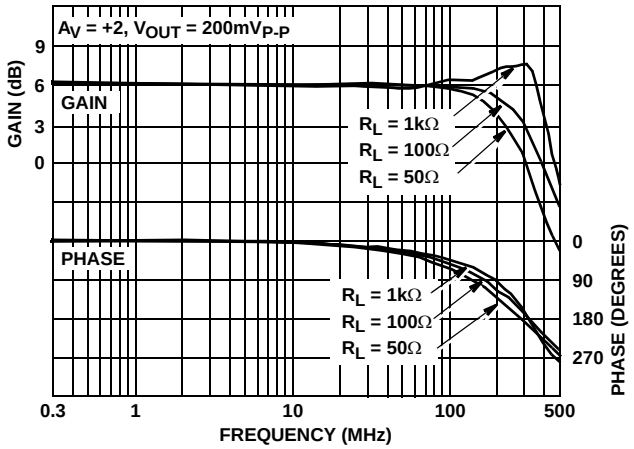


FIGURE 11. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

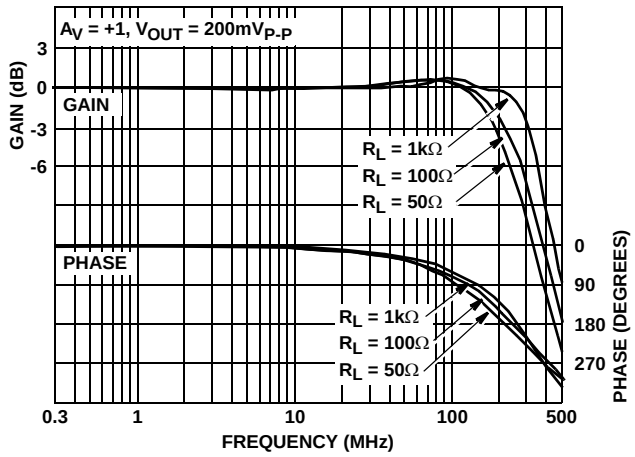


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

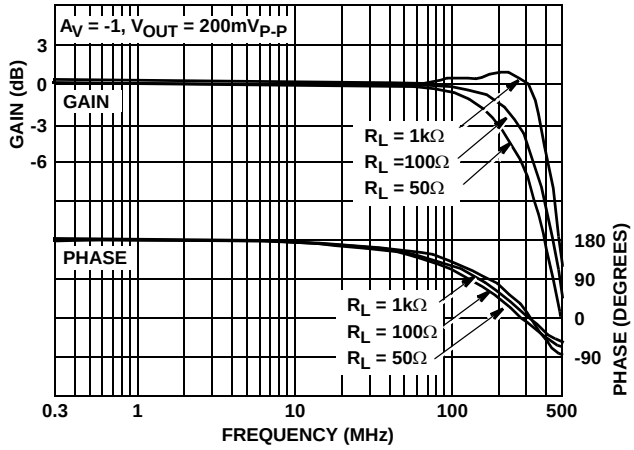


FIGURE 13. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

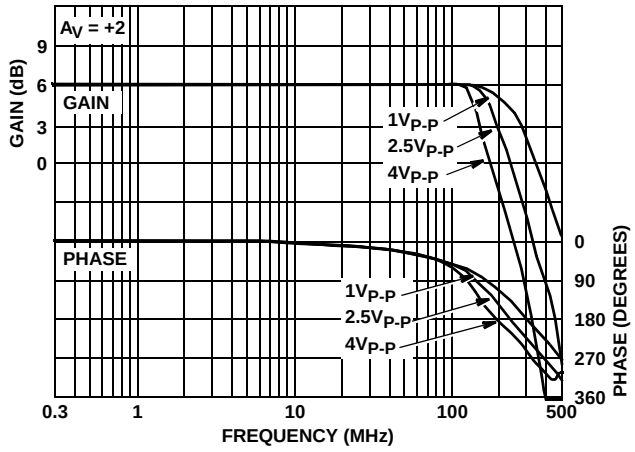


FIGURE 14. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

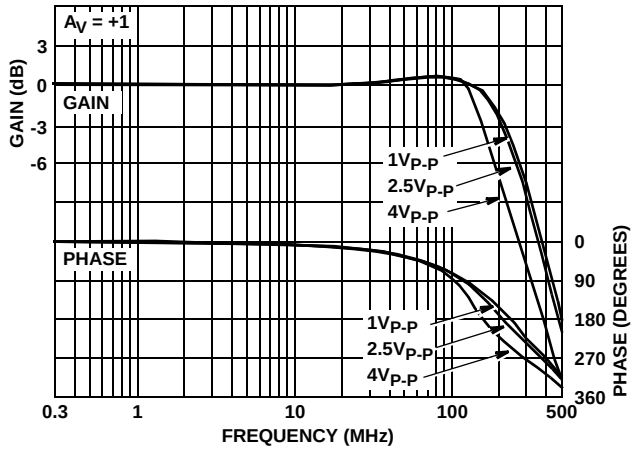


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25°C$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

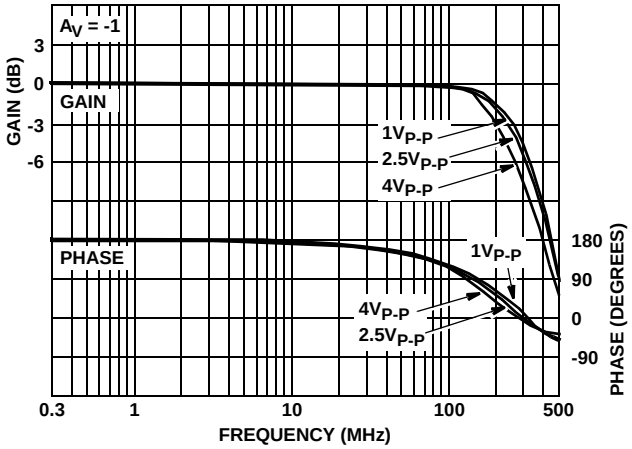


FIGURE 16. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

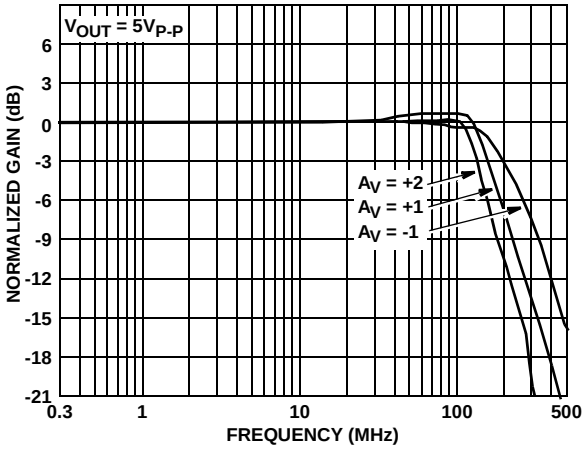


FIGURE 17. FULL POWER BANDWIDTH

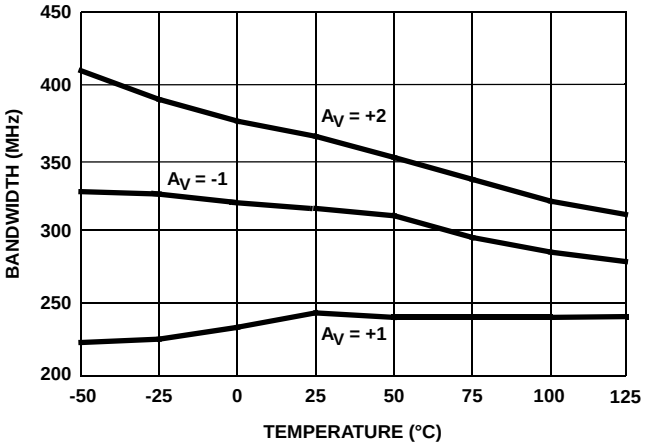


FIGURE 18. -3dB BANDWIDTH vs TEMPERATURE

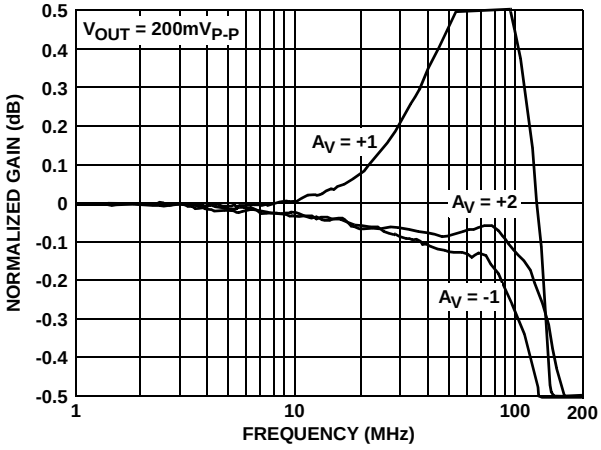


FIGURE 19. GAIN FLATNESS

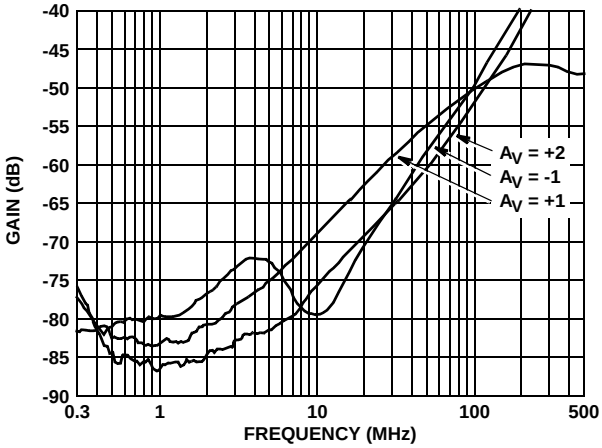


FIGURE 20. REVERSE ISOLATION (S_{12})

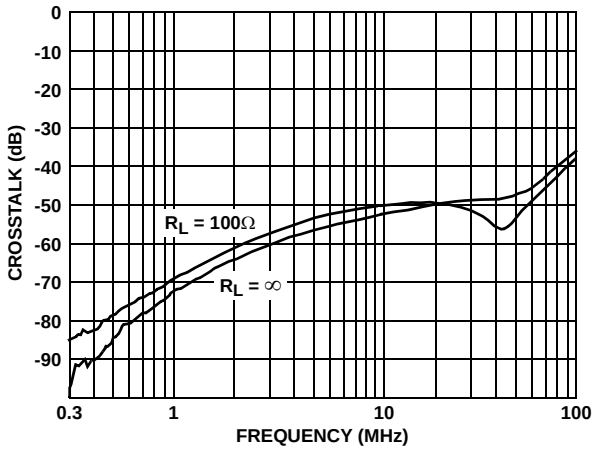


FIGURE 21. ALL HOSTILE CROSSTALK

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

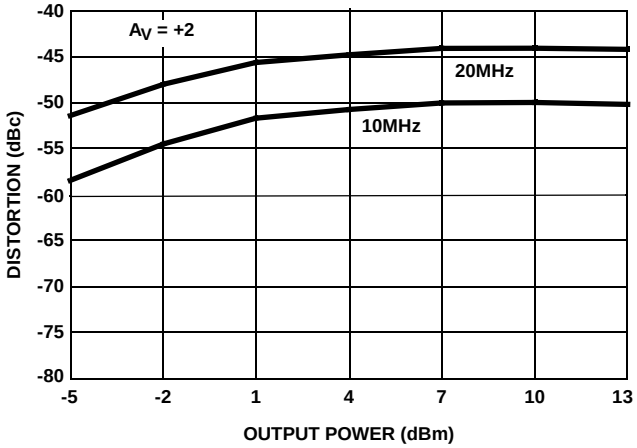


FIGURE 22. 2nd HARMONIC DISTORTION vs P_{OUT}

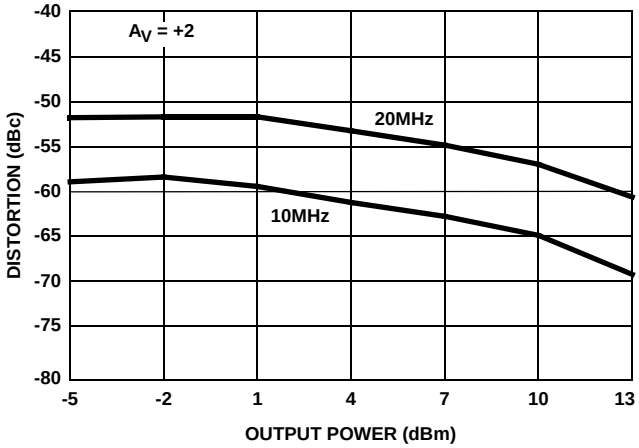


FIGURE 23. 3rd HARMONIC DISTORTION vs P_{OUT}

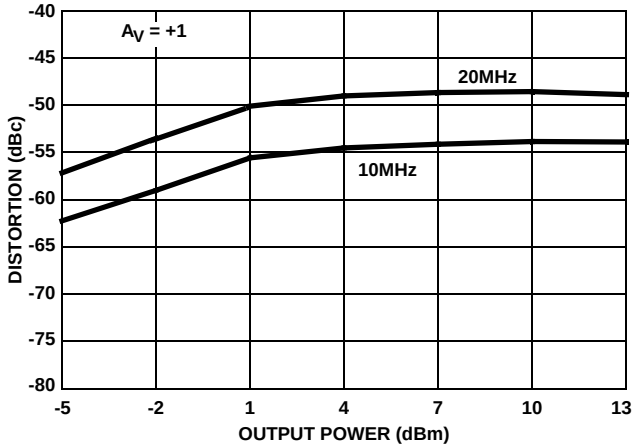


FIGURE 24. 2nd HARMONIC DISTORTION vs P_{OUT}

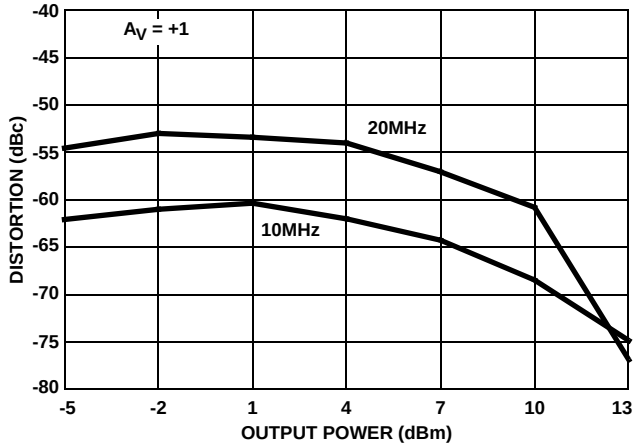


FIGURE 25. 3rd HARMONIC DISTORTION vs P_{OUT}

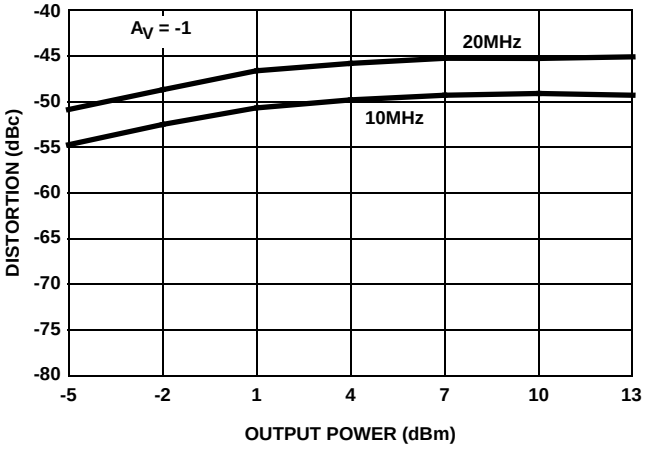


FIGURE 26. 2nd HARMONIC DISTORTION vs P_{OUT}

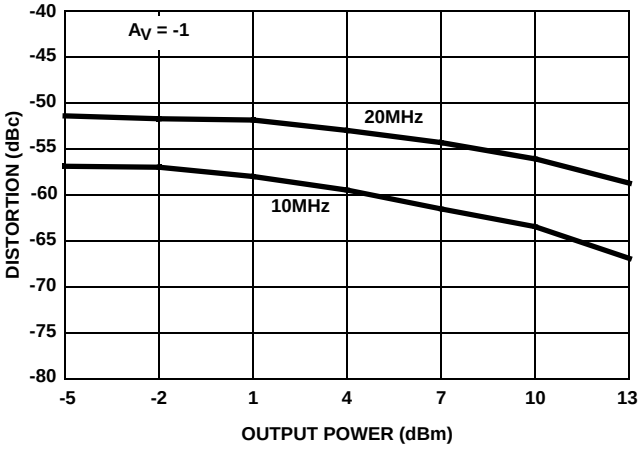


FIGURE 27. 3rd HARMONIC DISTORTION vs P_{OUT}

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25°C$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

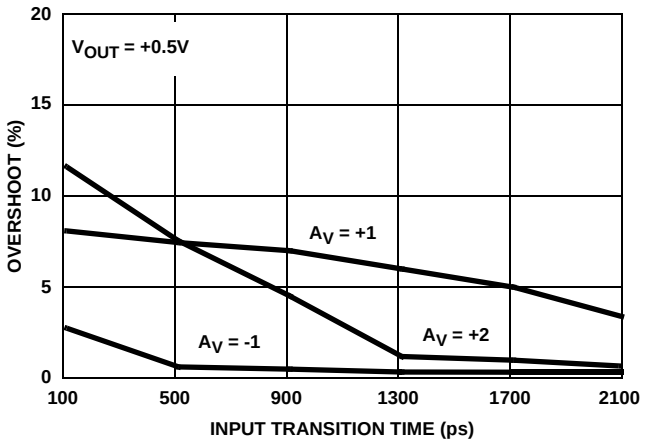


FIGURE 28. OVERSHOOT vs TRANSITION TIME

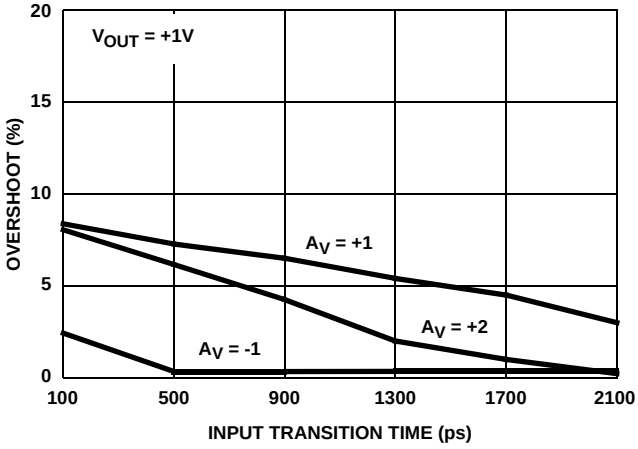


FIGURE 29. OVERSHOOT vs TRANSITION TIME

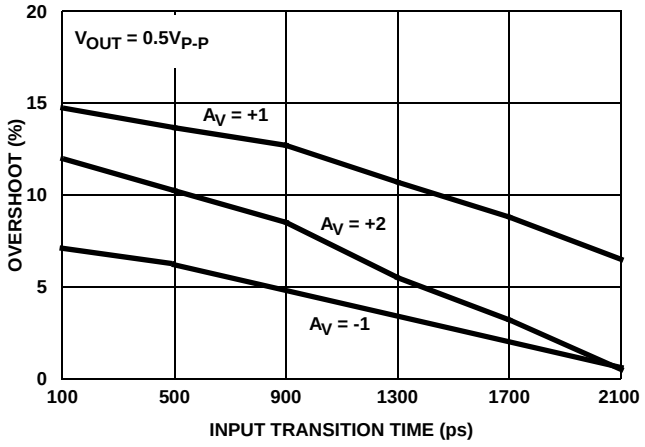


FIGURE 30. OVERSHOOT vs TRANSITION TIME

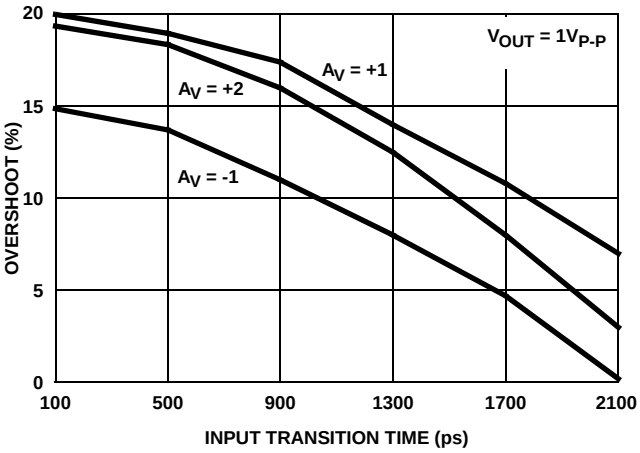


FIGURE 31. OVERSHOOT vs TRANSITION TIME

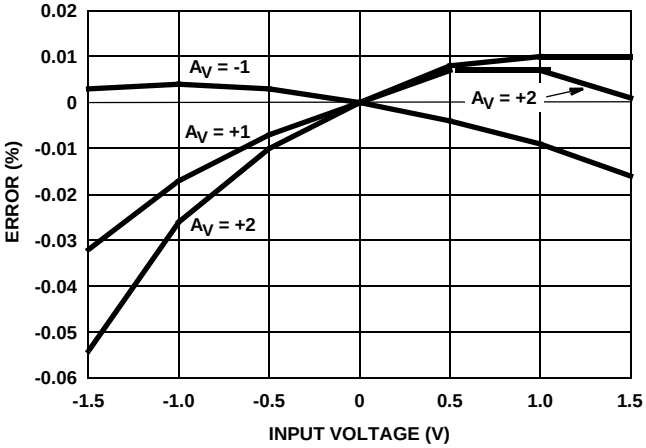


FIGURE 32. INTEGRAL LINEARITY ERROR

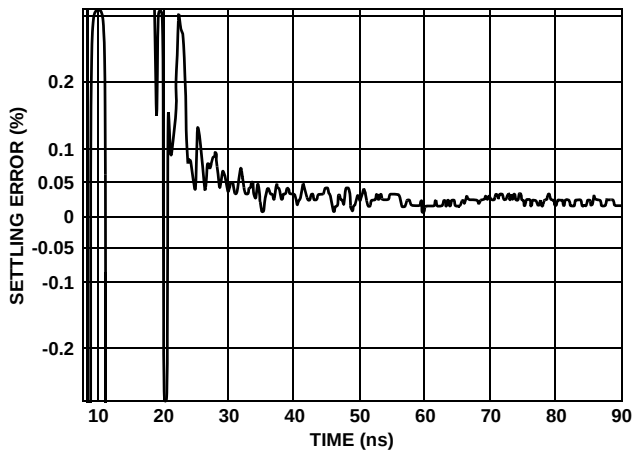


FIGURE 33. SETTLING RESPONSE

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

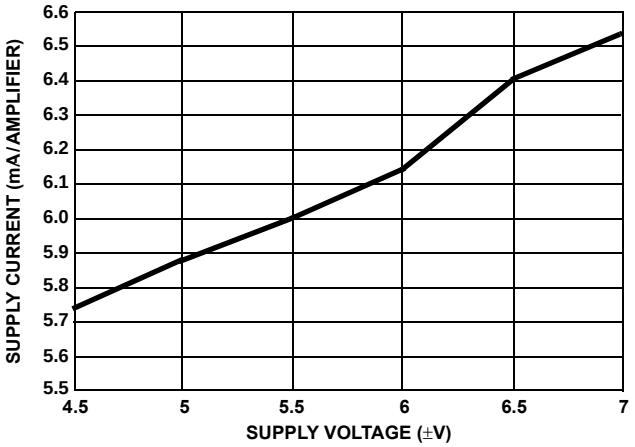


FIGURE 34. SUPPLY CURRENT vs SUPPLY VOLTAGE

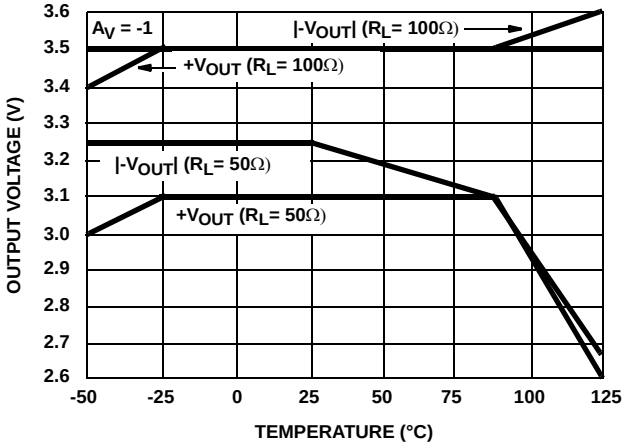


FIGURE 35. OUTPUT VOLTAGE vs TEMPERATURE

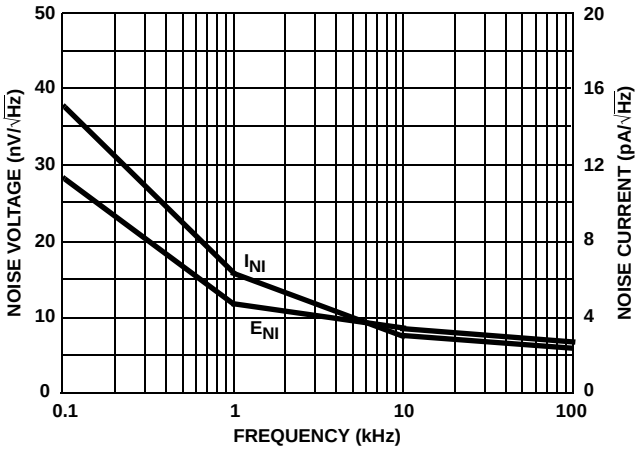


FIGURE 36. INPUT NOISE CHARACTERISTICS

Die Characteristics

DIE DIMENSIONS:

79 mils x 118 mils x 19 mils
2000μm x 3000μm x 483μm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

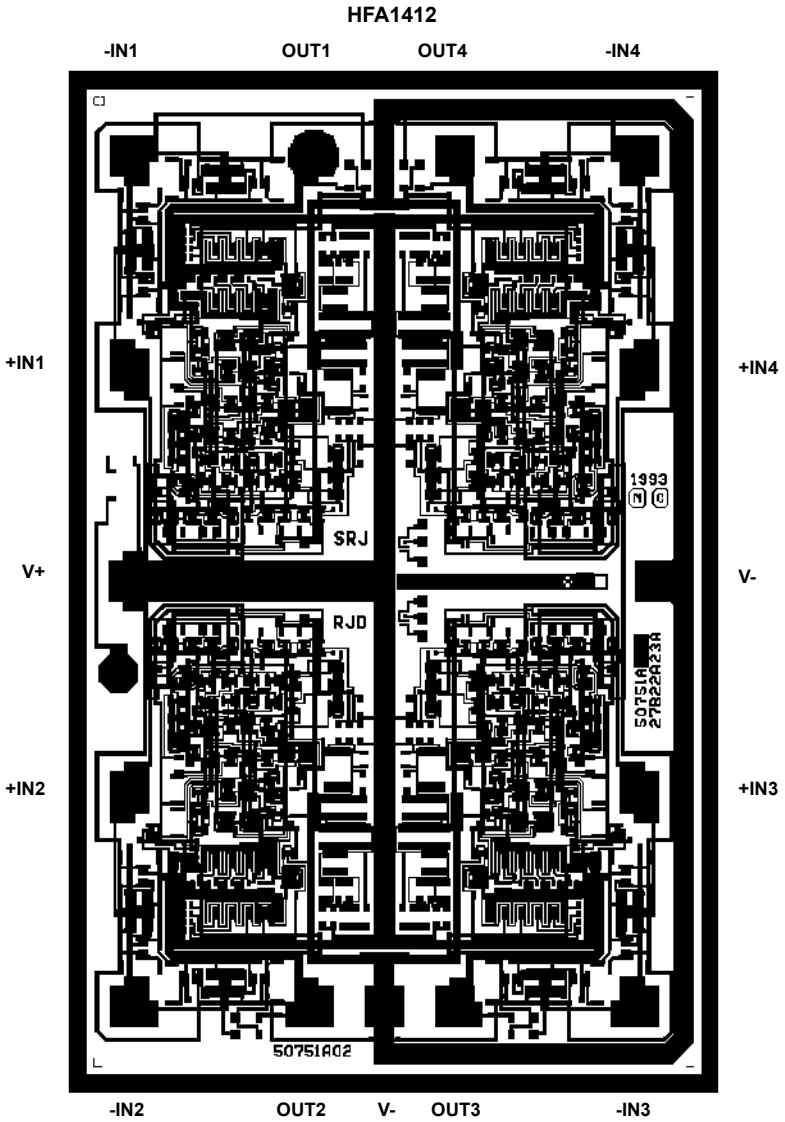
PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

320

Metallization Mask Layout



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Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality