National Semiconductor

November 12, 2008

LME49724
High Performance, High Fidelity, Fully-Differential Audio Operational Amplifier

General Description

The LME49724 is an ultra-low distortion, low noise, high slew rate fully-differential operational amplifier optimized and fully specified for high performance, high fidelity applications. Combining advanced leading-edge process technology with state of the art circuit design, the LME49724 fully-differential audio operational amplifier delivers superior audio signal amplification for outstanding audio performance. The LME49724 combines extremely low voltage noise density (2.1nV/$\sqrt{\text{Hz}}$) with vanishingly low THD+N (0.00003%) to easily satisfy the most demanding audio applications. To ensure that the most challenging loads are driven without compromise, the LME49724 has a high slew rate of ±18V/µs and an output current capability of ±80mA. Further, dynamic range is maximized by an output stage that drives 600Ω loads to $52V_{P-P}$ while operating on a ±15V supply voltage.

The LME49724's outstanding CMRR (102dB), PSRR (125dB), and V_{OS} (0.2mV) results in excellent operational amplifier DC performance.

The LME49724 has a wide supply range of ±2.5V to ±18V. Over this supply range the LME49724's input circuitry maintains excellent common-mode and power supply rejection, as well as maintaining its low input bias current. The LME49724 is unity gain stable. This Fully-Differential Audio Operational Amplifier achieves outstanding AC performance while driving complex loads with capacitive values as high as 100pF.

Key Specifications

- Power Supply Voltage Range ±2.5V to ±18V
- THD+N (A_V = 1, V_{OUT} = $3V_{RMS}$, f_{IN} = 1kHz)
  - R_L = 2kΩ 0.00003% (typ)
  - R_L = 600Ω 0.00003% (typ)
- Input Noise Density 2.1nV/$\sqrt{\text{Hz}}$ (typ)
- Slew Rate ±18V/µs (typ)
- Gain Bandwidth Product 50MHz (typ)
- Open Loop Gain (R_L = 600Ω) 125dB (typ)
- Input Bias Current 60nA (typ)
- Input Offset Voltage 0.2mV (typ)
- DC Gain Linearity Error 0.000009%

Features

- Drives 600Ω loads with full output signal swing
- Optimized for superior audio signal fidelity
- Output short circuit protection
- PSRR and CMRR exceed 100dB (typ)
- Available in PSOP package

Applications

- Ultra high quality audio amplification
- High fidelity preamplifiers and active filters
- Simple single-ended to differential conversion
- State of the art D-to-A converters
- State of the art A-to-D input amplifiers
- Professional Audio
- High fidelity equalization and crossover networks
- High performance line drivers and receivers

Typical Application

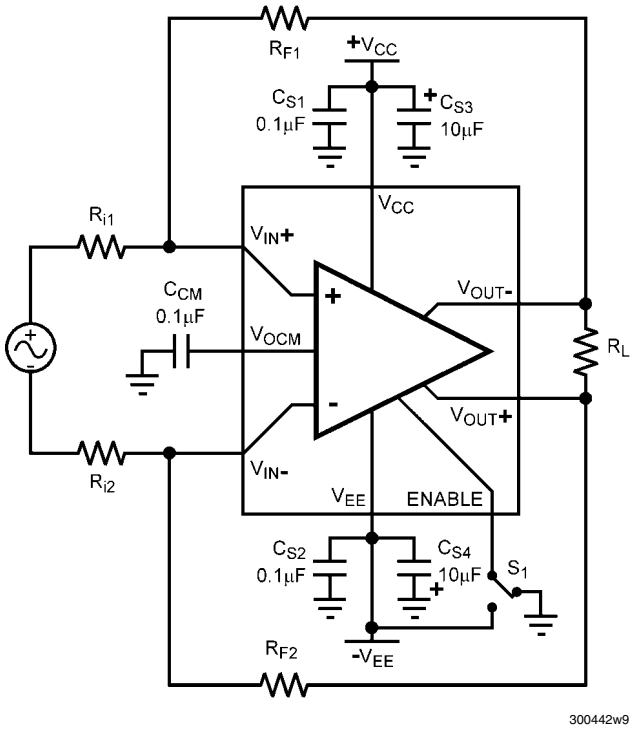
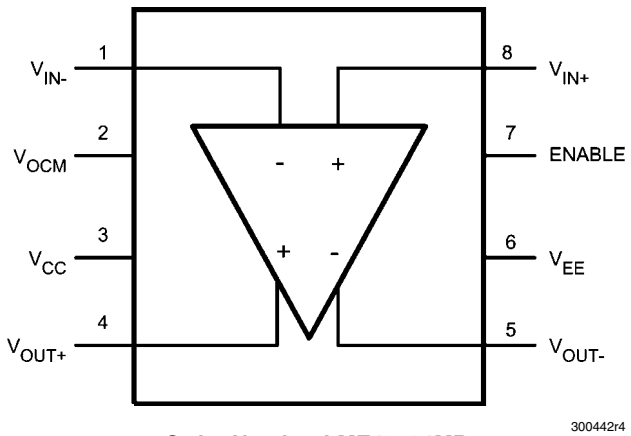


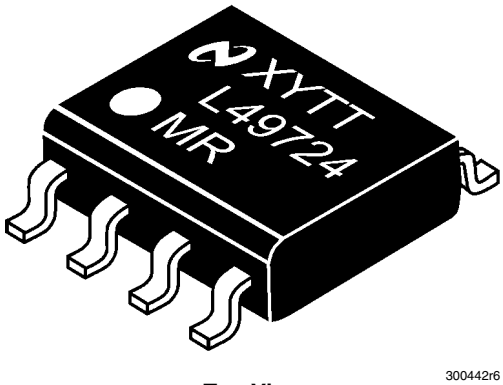
FIGURE 1. Typical Application Circuit

Connection Diagrams



Order Number LME49724MR
See NS Package Number MRA08B

PSOP Marking



Top View
XY — Date Code
TT — Die Traceability
L49724 — LME49724
MR — Package Code

Ordering Information

Order Number	Package	Package DWG #	Transport Media	MSL Level	Green Status	Features
LME49724MR	8 lead PSOP	MRA08B				

Pin Descriptions

Pin	Name	Pin Function	Type
1	V_{IN-}	Input pin	Analog Input
2	V_{OCM}	Sets the output DC voltage. Internally set by a resistor divider to the midpoint of the voltages on the V_{CC} and V_{EE} pins. Can be forced externally to a different voltage (50kΩ input impedance).	Analog Input
3	V_{CC}	Positive power supply pin.	Power Supply
4	V_{OUT+}	Output pin. Signal is inverted relative to V_{IN-} where the feedback loop is connected.	Analog Output
5	V_{OUT-}	Output pin. Signal is inverted relative to V_{IN+} where the feedback loop is connected.	Analog Output
6	V_{EE}	Negative power supply pin or ground for a single supply configuration.	Power Supply
7	ENABLE	Enables the LME49724 when the voltage is greater than 2.35V above the voltage on the V_{EE} pin. Disable the LME49724 by connecting to the same voltage as on the V_{EE} pin which will reduce current consumption to less than 0.3mA (typ).	Analog Input
8	V_{IN+}	Input pin	Analog Input
Exposed Pad		Exposed pad for improved thermal performance. Connect to the same potential as the V_{EE} pin or electrically isolate.	

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage ($V_S = V_{CC} + \|V_{EE}\|$)	38V
Storage Temperature	−65°C to 150°C
Input Voltage	$(V_{EE}) - 0.7V$ to $(V_{CC}) + 0.7V$
Output Short Circuit	Continuous
Power Dissipation (Note 3)	Internally Limited
ESD Rating (Note 4)	2000V
ESD Rating (Note 5)	200V
Junction Temperature (T_{JMAX})	150°C
Soldering Information	
Vapor Phase (60sec.)	215°C
Infrared (60sec.)	220°C
Thermal Resistance	
θ_{JA} (MR)	49.6°C/W

Operating Ratings (Notes 1, 2)

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage Range	$\pm 2.5V \le V_S \le \pm 18V$

Electrical Characteristics (Notes 1, 2)

The following specifications apply for $V_S = \pm 15V$, $R_L = 2k\Omega$, $f_{IN} = 1kHz$, and $T_A = 25°C$, unless otherwise specified.

Symbol	Parameter	Conditions	LME49724 Typical (Note 6)	LME49724 Limit (Note 7)	Units (Limits)
POWER SUPPLY					
V_S	Operating Power Supply			±2.5V ±18V	V (min) V (max)
I_{CCQ}	Total Quiescent Current	$V_O = 0V$, $I_O = 0mA$ Enable = GND Enable = V_{EE}	 10 0.3	 15 0.5	 mA (max) mA (max)
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 15V$ (Note 8)	125	95	dB (min)
V_{ENIH}	Enable High Input Voltage	Device active, $T_A = 25°C$ (Note 9)	$V_{EE} + 2.35$		V
V_{ENIL}	Enable Low Input Voltage	Device disabled, $T_A = 25°C$ (Note 9)	$V_{EE} + 1.75$		V
DYNAMIC PERFORMANCE					
THD+N	Total Harmonic Distortion + Noise	$A_V = 1$, $V_{OUT} = 3V_{RMS}$ $R_L = 2k\Omega$ $R_L = 600\Omega$	 0.00003 0.00003	 0.00009	 % % (max)
IMD	Intermodulation Distortion	$A_V = 1$, $V_{OUT} = 3V_{RMS}$ Two-tone, 60Hz & 7kHz 4:1	0.0005		%
GBWP	Gain Bandwidth Product		50	35	MHz (min)
FPBW	Full Power Bandwidth	$V_{OUT} = 1V_{P-P}$, −3dB referenced to output magnitude at f = 1kHz	13		MHz
SR	Sew Rate	$R_L = 2k\Omega$	±18	±13	V/µs (min)
t_S	Settling time	$A_V = -1$, 10V step, $C_L = 100pF$ settling time to 0.1%	0.2		µs
A_{VOL}	Open-Loop Voltage Gain	$-10V < V_{OUT} < 10V$, $R_L = 600\Omega$	125	100	dB (min)
		$-10V < V_{OUT} < 10V$, $R_L = 2k\Omega$	125		dB
		$-10V < V_{OUT} < 10V$, $R_L = 10k\Omega$	125		dB
NOISE					
e_N	Equivalent Input Noise Voltage	$f_{BW} = 20Hz$ to $20kHz$	0.30	0.64	μV_{RMS} (max)
	Equivalent Input Noise Density	f = 1kHz f = 10Hz	2.1 3.7		$nV/\sqrt{Hz}$ (max)
INPUT CHARACTERISTICS					
V_{OS}	Offset Voltage		±0.2	±1	mV (max)
$\Delta V_{OS}/\Delta Temp$	Average Input Offset Voltage Drift vs Temperature	$-40°C \le T_A \le 85°C$	0.5		µV/°C

Symbol	Parameter	Conditions	LME49724		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
I_B	Input Bias Current	V_{CM} = 0V	60	200	nA (max)
I_{OS}	Input Offset Current	V_{CM} = 0V	10	65	nA (max)
$\Delta I_{OS}/\Delta Temp$	Input Bias Current Drift vs Temperature	–40°C ≤ T_A ≤ 85°C	0.1		nA/°C
V_{IN-CM}	Common-Mode Input Voltage Range		±14	V_{CC} – 1.5 V_{EE} + 1.5	V (min) V (min)
CMRR	Common-Mode Rejection	–10V < V_{CM} < 10V	102	95	dB (min)
Z_{IN}	Differential Input Impedance		16		kΩ
	Common-Mode Input Impedance	–10V < V_{CM} < 10V	500		MΩ
OUTPUT CHARACTERISTICS					
V_{OUTMAX}	Maximum Output Voltage Swing	R_L = 600Ω	52	50	V_{P-P} (min)
		R_L = 2kΩ	52		V_{P-P}
		R_L = 10kΩ	53		V_{P-P}
I_{OUT-CC}	Instantaneous Short Circuit Current		80		mA
R_{OUT}	Output Impedance	f_{IN} = 10kHz Closed-Loop Open-Loop	 0.01 23		 Ω Ω
C_{LOAD}	Capacitive Load Drive Overshoot	C_L = 100pF	5		%

Note 1: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

Note 4: Human body model, applicable std. JESD22-A114C.

Note 5: Machine model, applicable std. JESD22-A115-A.

Note 6: Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.

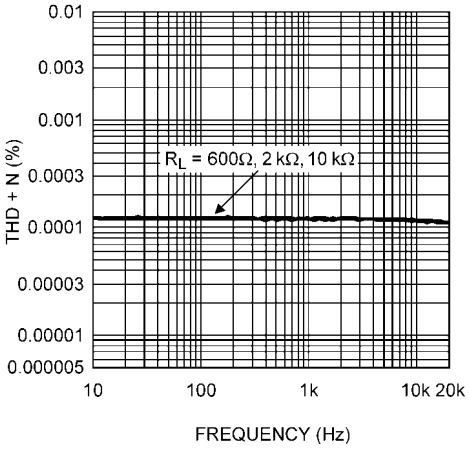
Note 7: Datasheet min/max specification limits are guaranteed by test or statistical analysis.

Note 8: PSRR is measured as follows: V_{OS} is measured at two supply voltages, ±5V and ±15V. PSRR = | $20\log(\Delta V_{OS}/\Delta V_S)$ |.

Note 9: The ENABLE threshold voltage is determined by V_{BE} voltages and will therefore vary with temperature. The typical values represent the most likely parametric norms at T_A = +25°C.

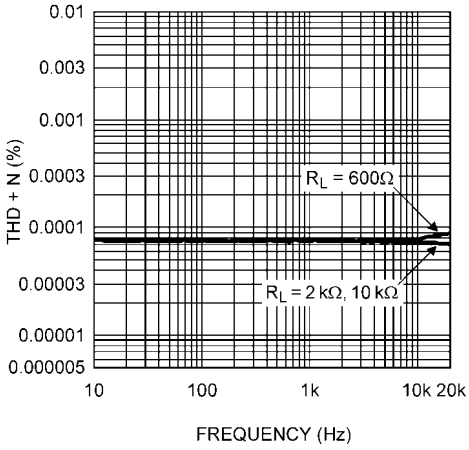
Typical Performance Characteristics

THD+N vs Frequency
V_S = ±2.5V, V_O = 0.5V_{RMS}, Differential Input
R_L = 600Ω, 2kΩ, 10kΩ, 80kHz BW



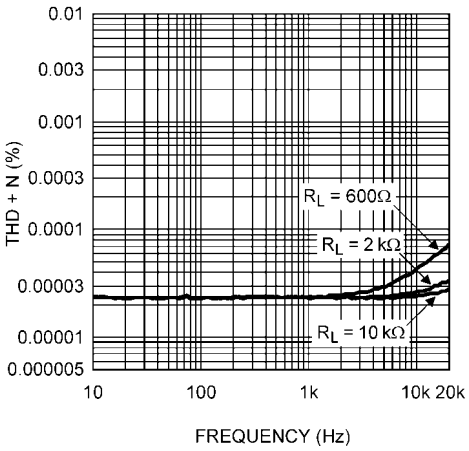
300442s3

THD+N vs Frequency
V_S = ±2.5V, V_O = 0.8V_{RMS}, Differential Input
R_L = 600Ω, 2kΩ, 10kΩ, 80kHz BW



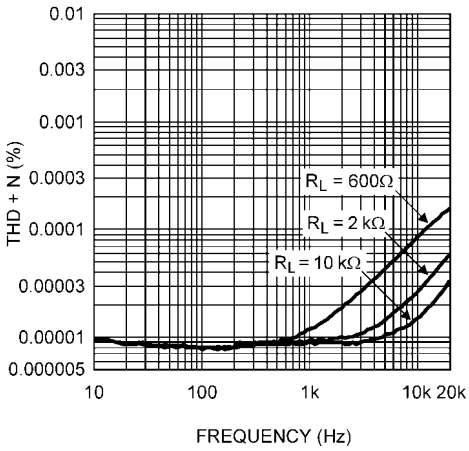
300442s4

THD+N vs Frequency
V_S = ±15V, V_O = 3V_{RMS}, Differential Input
R_L = 600Ω, 2kΩ, 10kΩ, 80kHz BW



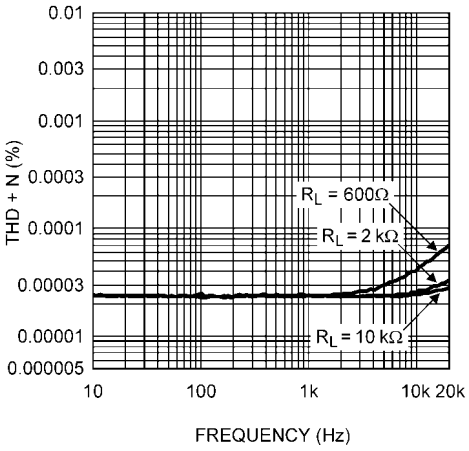
300442s5

THD+N vs Frequency
V_S = ±15V, V_O = 10V_{RMS}, Differential Input
R_L = 600Ω, 2kΩ, 10kΩ, 80kHz BW



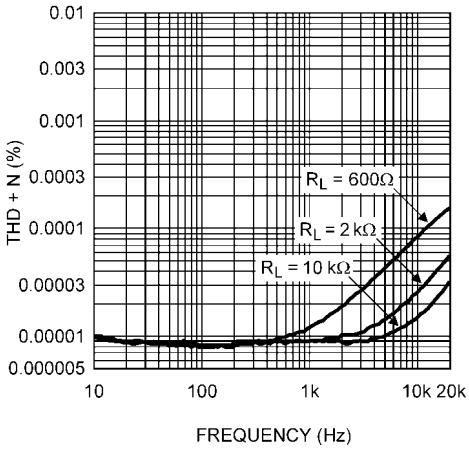
300442s6

THD+N vs Frequency
V_S = ±18V, V_O = 3V_{RMS}, Differential Input
R_L = 600Ω, 2kΩ, 10kΩ, 80kHz BW



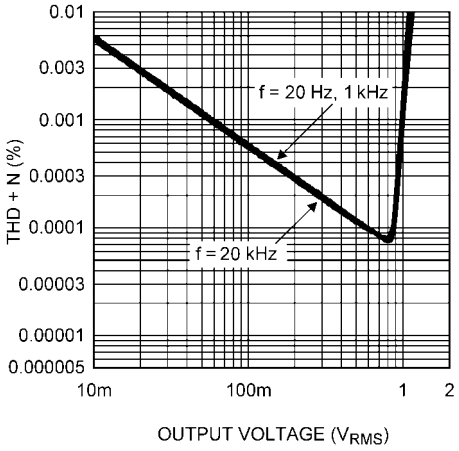
300442s7

THD+N vs Frequency
V_S = ±18V, V_O = 10V_{RMS}, Differential Input
R_L = 600Ω, 2kΩ, 10kΩ, 80kHz BW



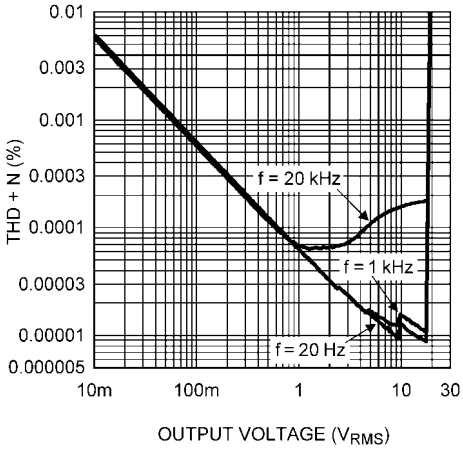
300442s8

THD+N vs Output Voltage
V_S = ±2.5V, R_L = 600Ω, Differential Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



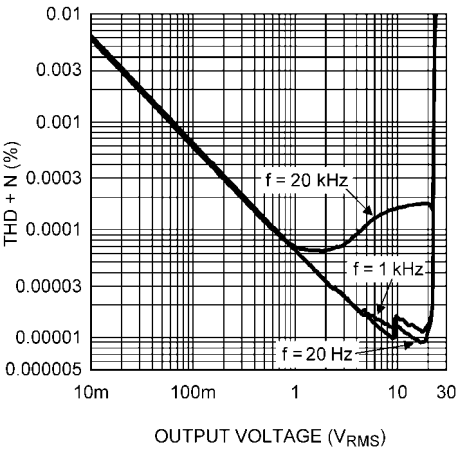
300442t1

THD+N vs Output Voltage
V_S = ±15V, R_L = 600Ω, Differential Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



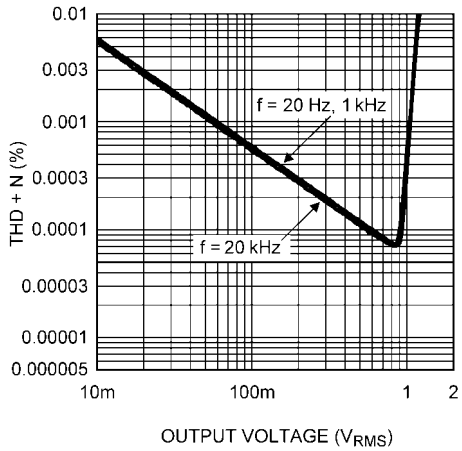
300442t4

THD+N vs Output Voltage
V_S = ±18V, R_L = 600Ω, Differential Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



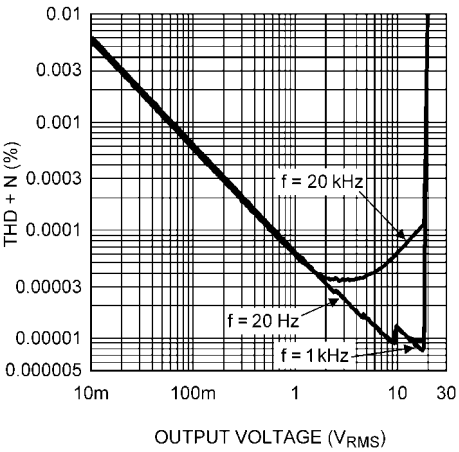
300442t7

THD+N vs Output Voltage
V_S = ±2.5V, R_L = 2kΩ, Differential Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



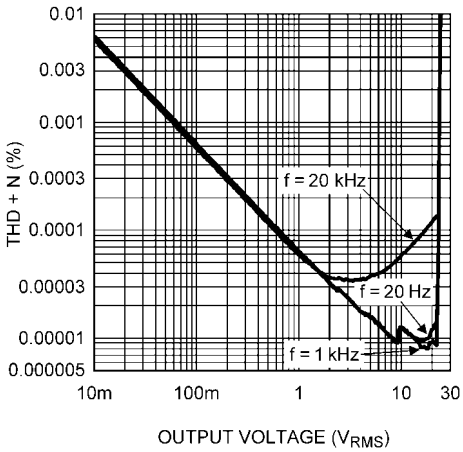
300442s9

THD+N vs Output Voltage
V_S = ±15V, R_L = 2kΩ, Differential Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



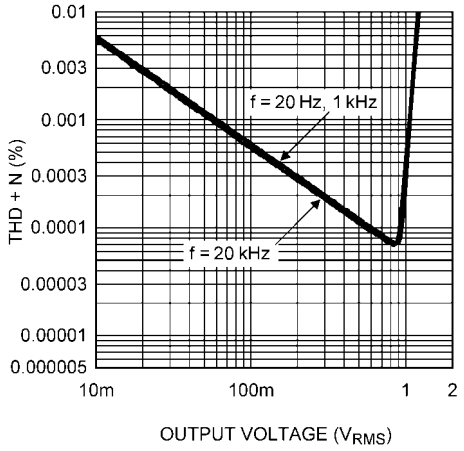
300442t2

THD+N vs Output Voltage
V_S = ±18V, R_L = 2kΩ, Differential Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



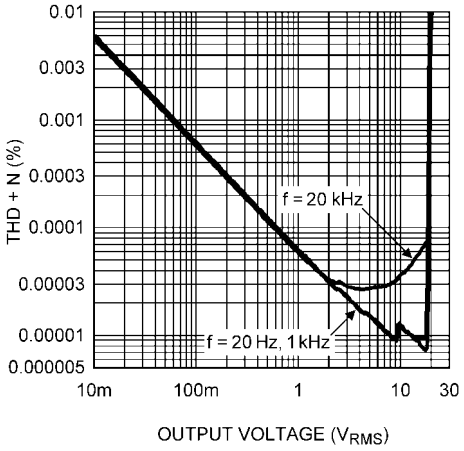
300442t5

THD+N vs Output Voltage
V_S = ±2.5V, R_L = 10kΩ, Differential Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



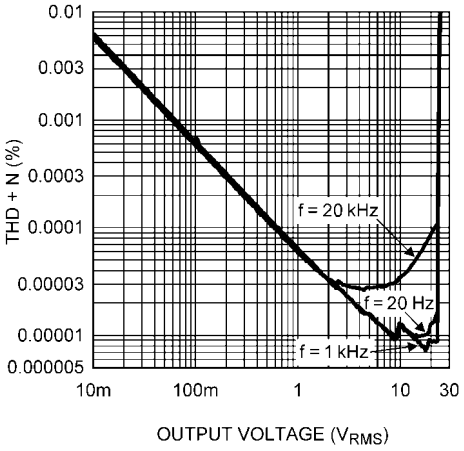
300442t0

THD+N vs Output Voltage
V_S = ±15V, R_L = 10kΩ, Differential Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



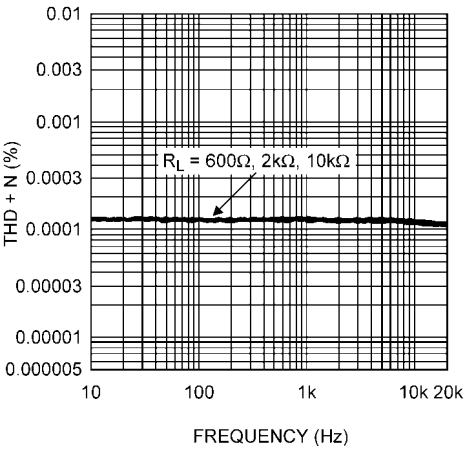
300442t3

THD+N vs Output Voltage
V_S = ±18V, R_L = 10kΩ, Differential Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



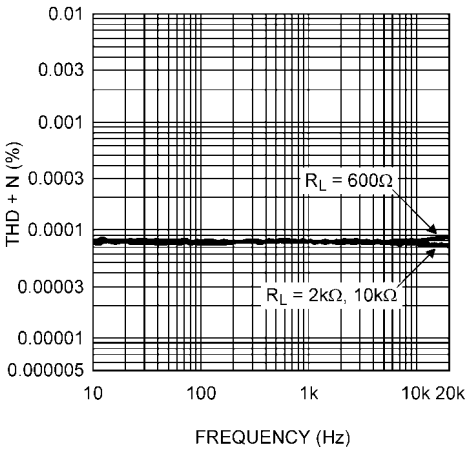
300442t6

THD+N vs Frequency
V_S = ±2.5V, V_O = 0.5V_{RMS}, Single-ended Input
R_L = 600Ω, 2kΩ, 10kΩ, 80kHz BW



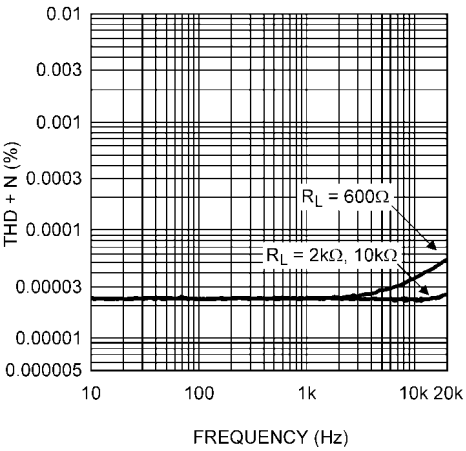
300442u8

THD+N vs Frequency
V_S = ±2.5V, V_O = 0.8V_{RMS}, Single-ended Input
R_L = 600Ω, 2kΩ, 10kΩ, 80kHz BW



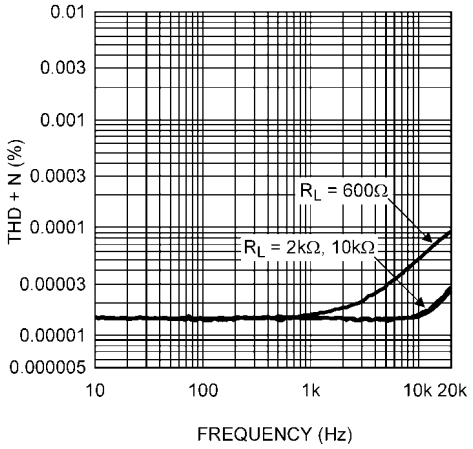
300442u9

THD+N vs Frequency
V_S = ±15V, V_O = 3V_{RMS}, Single-ended Input
R_L = 600Ω, 2kΩ, 10kΩ, 80kHz BW



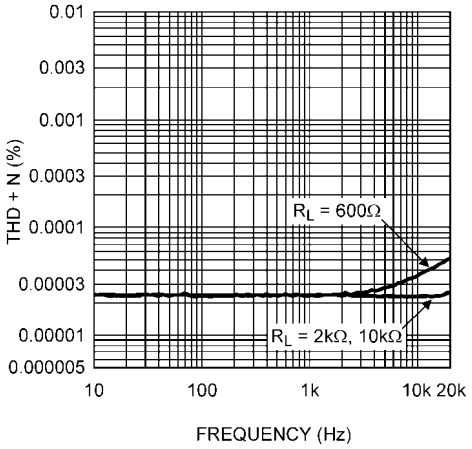
300442v0

THD+N vs Frequency
V_S = ±15V, V_O = 5V_{RMS}, Single-ended Input
R_L = 600Ω, 2kΩ, 10kΩ, 80kHz BW



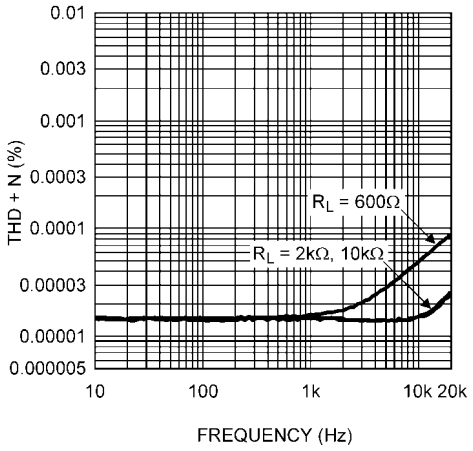
300442v1

THD+N vs Frequency
V_S = ±18V, V_O = 3V_{RMS}, Single-ended Input
R_L = 600Ω, 2kΩ, 10kΩ, 80kHz BW



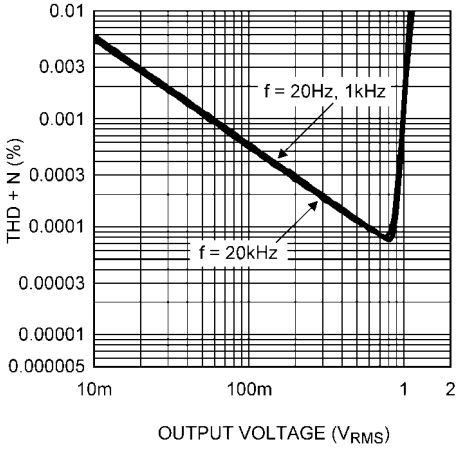
300442v2

THD+N vs Frequency
V_S = ±18V, V_O = 5V_{RMS}, Single-ended Input
R_L = 600Ω, 2kΩ, 10kΩ, 80kHz BW



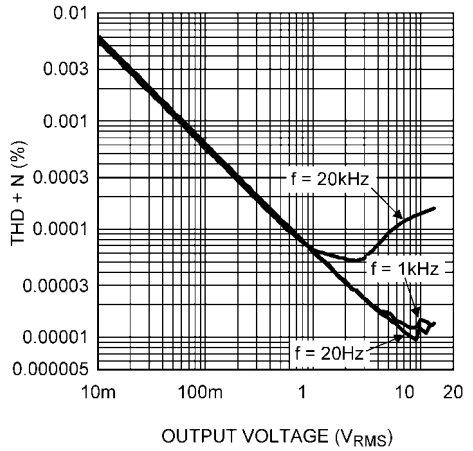
300442v3

THD+N vs Output Voltage
V_S = ±2.5V, R_L = 600Ω, Single-ended Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



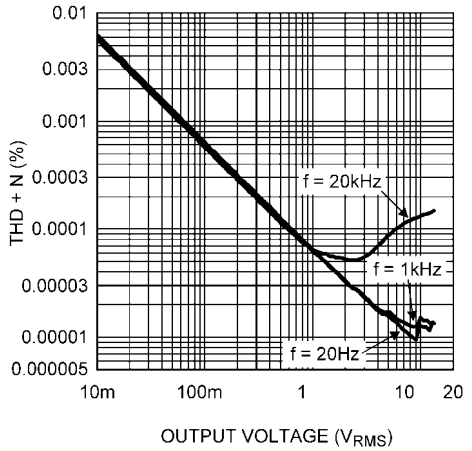
300442v6

THD+N vs Output Voltage
V_S = ±15V, R_L = 600Ω, Single-ended Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



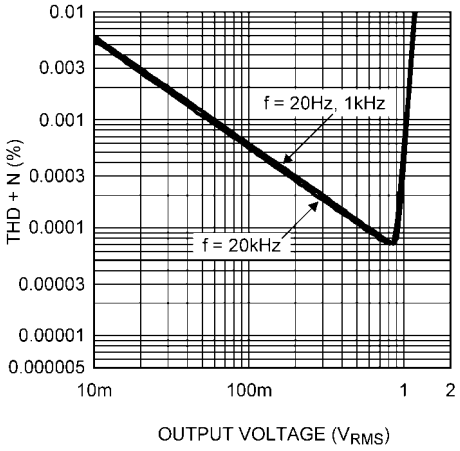
300442v9

THD+N vs Output Voltage
V_S = ±18V, R_L = 600Ω, Single-ended Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



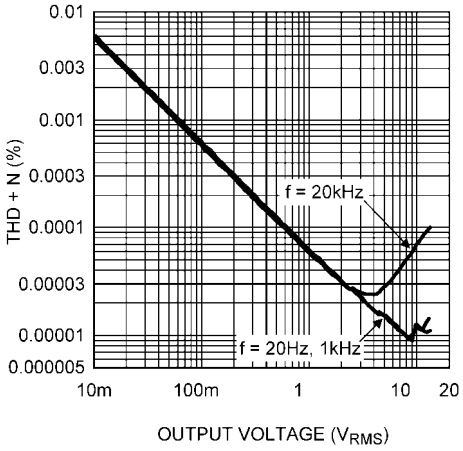
300442w2

THD+N vs Output Voltage
V_S = ±2.5V, R_L = 2kΩ, Single-ended Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



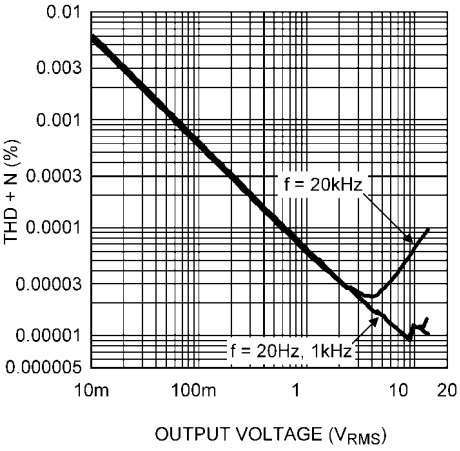
300442v4

THD+N vs Output Voltage
V_S = ±15V, R_L = 2kΩ, Single-ended Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



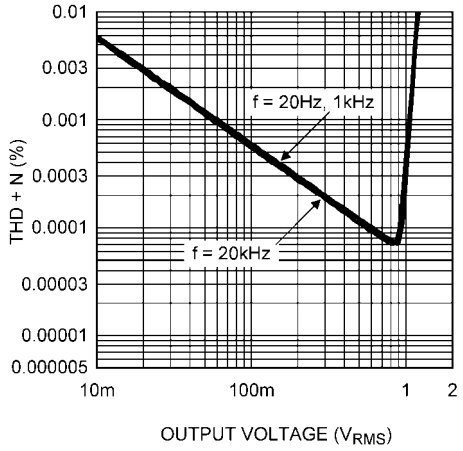
300442v7

THD+N vs Output Voltage
V_S = ±18V, R_L = 2kΩ, Single-ended Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



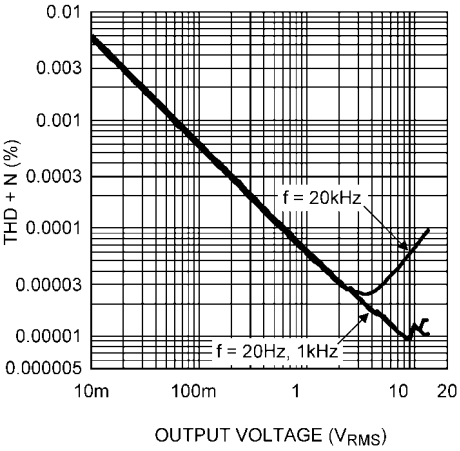
300442w0

THD+N vs Output Voltage
V_S = ±2.5V, R_L = 10kΩ, Single-ended Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



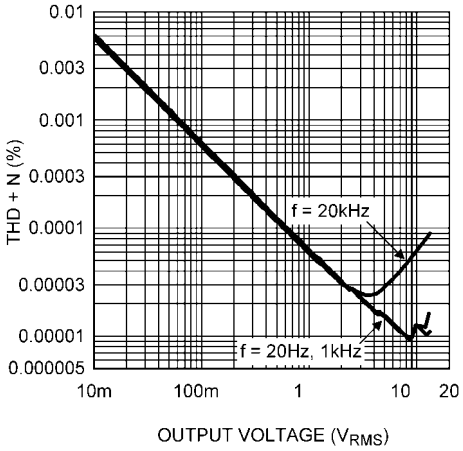
300442v5

THD+N vs Output Voltage
V_S = ±15V, R_L = 10kΩ, Single-ended Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



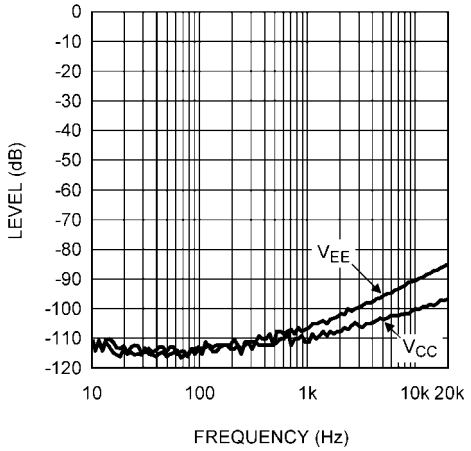
300442v8

THD+N vs Output Voltage
V_S = ±18V, R_L = 10kΩ, Single-ended Input
f = 20Hz, 1kHz, 20kHz, 80kHz BW



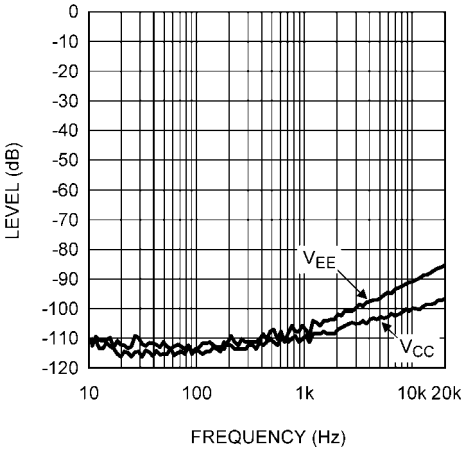
300442w1

PSRR vs Frequency
V_S = ±2.5V, R_L = 600Ω, Inputs to GND
V_{RIPPLE} = 200mV_{P-P}, 80kHz BW



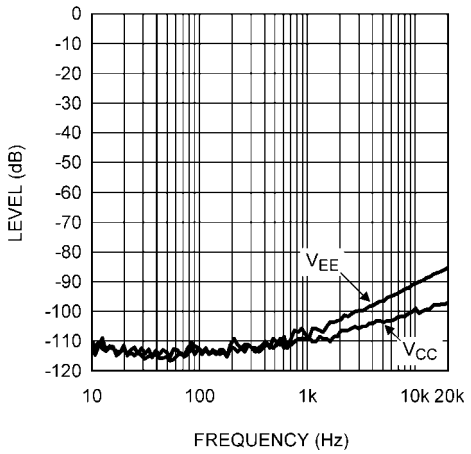
300442u0

PSRR vs Frequency
V_S = ±15V, R_L = 600Ω, Inputs to GND
V_{RIPPLE} = 200mV_{P-P}, 80kHz BW



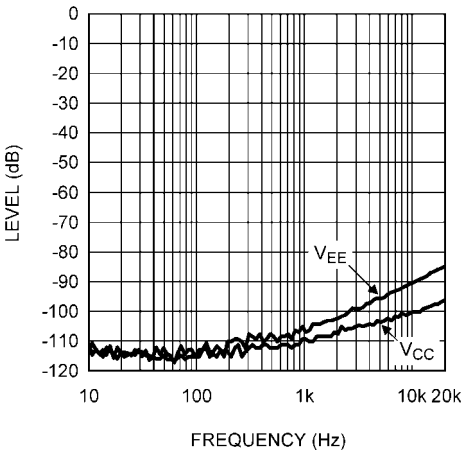
300442u3

PSRR vs Frequency
V_S = ±18V, R_L = 600Ω, Inputs to GND
V_{RIPPLE} = 200mV_{P-P}, 80kHz BW



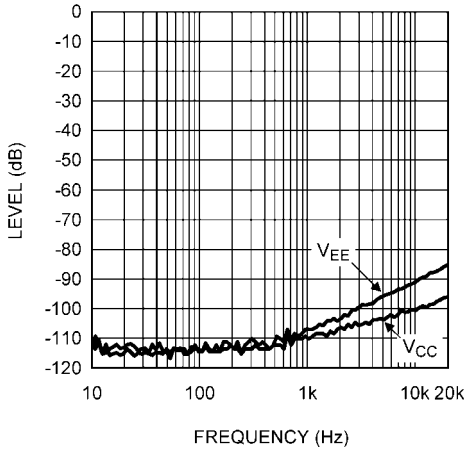
300442u6

PSRR vs Frequency
V_S = ±2.5V, R_L = 2kΩ, Inputs to GND
V_{RIPPLE} = 200mV_{P-P}, 80kHz BW



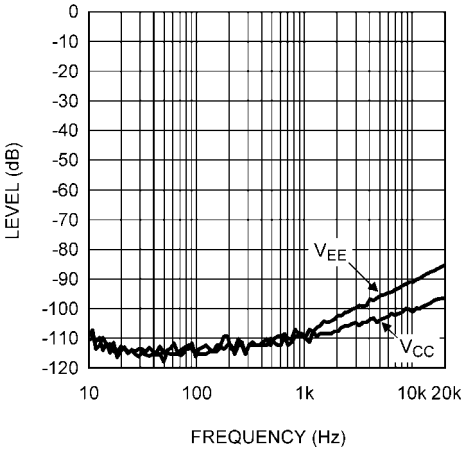
300442t8

PSRR vs Frequency
V_S = ±15V, R_L = 2kΩ, Inputs to GND
V_{RIPPLE} = 200mV_{P-P}, 80kHz BW



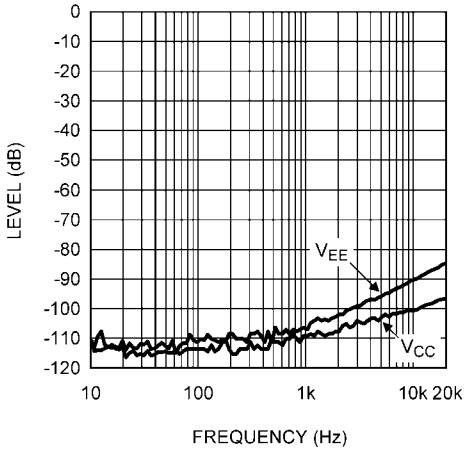
300442u1

PSRR vs Frequency
V_S = ±18V, R_L = 2kΩ, Inputs to GND
V_{RIPPLE} = 200mV_{P-P}, 80kHz BW



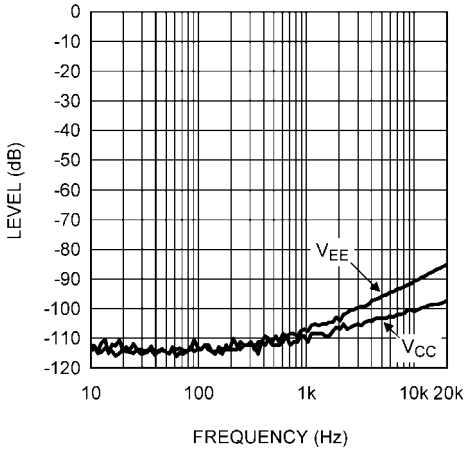
300442u4

PSRR vs Frequency
V_S = ±2.5V, R_L = 10kΩ, Inputs to GND
V_{RIPPLE} = 200mV_{P-P}, 80kHz BW



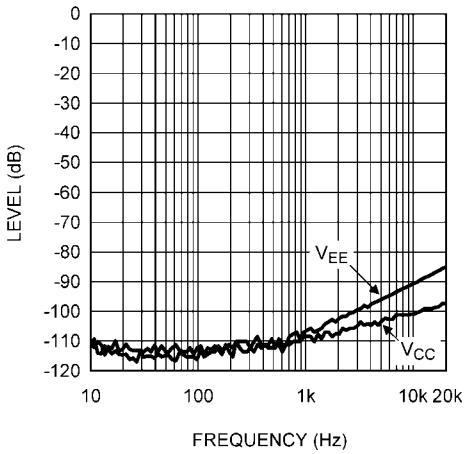
300442t9

PSRR vs Frequency
V_S = ±15V, R_L = 10kΩ, Inputs to GND
V_{RIPPLE} = 200mV_{P-P}, 80kHz BW



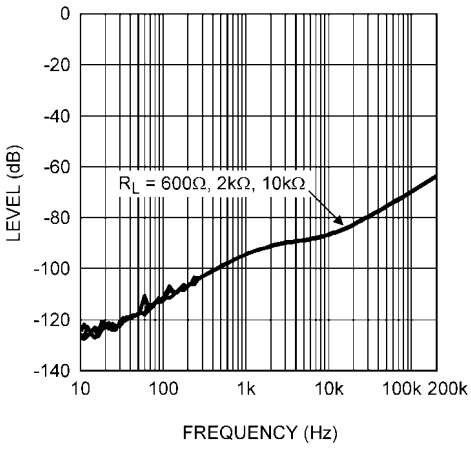
300442u2

PSRR vs Frequency
V_S = ±18V, R_L = 10kΩ, Inputs to GND
V_{RIPPLE} = 200mV_{P-P}, 80kHz BW



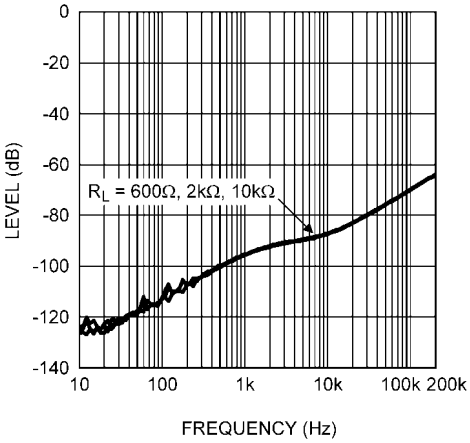
300442u5

CMRR vs Frequency
V_S = ±2.5V, V_{CMRR} = 1V_{P-P}
R_L = 600Ω, 2kΩ, 10kΩ



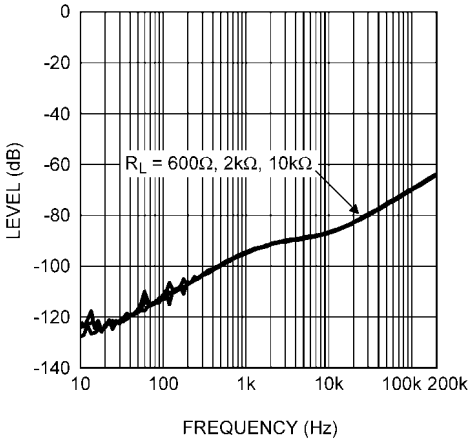
300442y0

CMRR vs Frequency
V_S = ±15V, V_{CMRR} = 1V_{P-P}
R_L = 600Ω, 2kΩ, 10kΩ



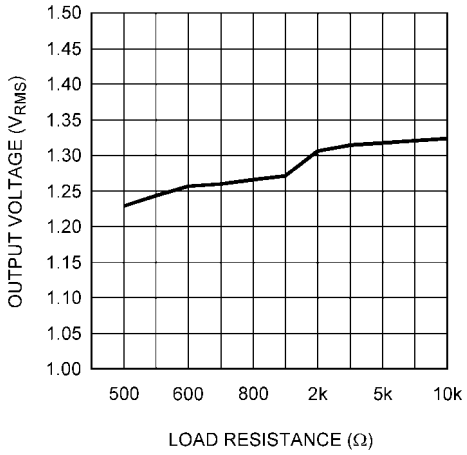
300442x8

CMRR vs Frequency
V_S = ±18V, V_{CMRR} = 1V_{P-P}
R_L = 600Ω, 2kΩ, 10kΩ



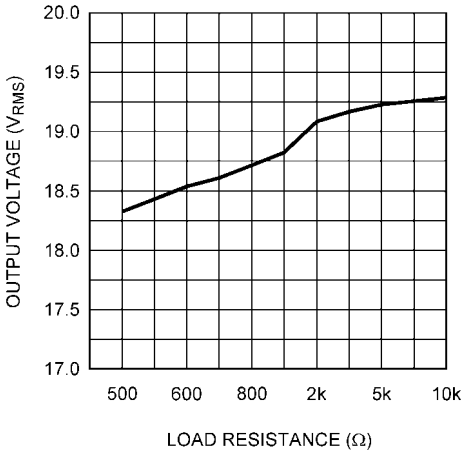
300442x9

Output Voltage vs Load Resistance
V_S = ±2.5V, R_L = 500Ω – 10kΩ
THD+N ≤ 1%, 80kHz BW



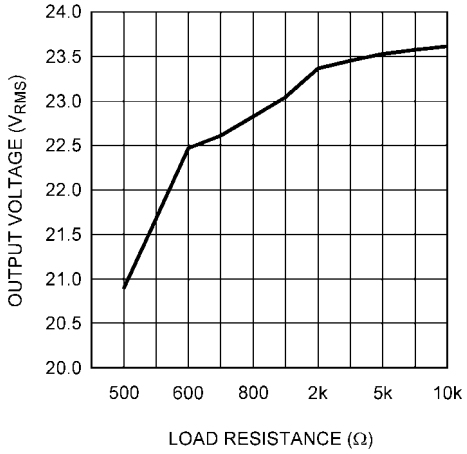
300442w3

Output Voltage vs Load Resistance
V_S = ±15V, R_L = 500Ω – 10kΩ
THD+N ≤ 1%, 80kHz BW



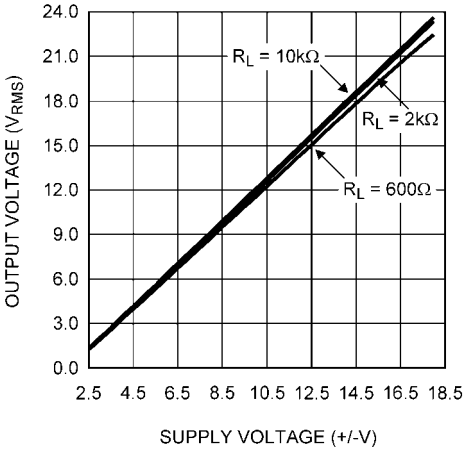
300442w4

Output Voltage vs Load Resistance
V_S = ±18V, R_L = 500Ω – 10kΩ
THD+N ≤ 1%, 80kHz BW



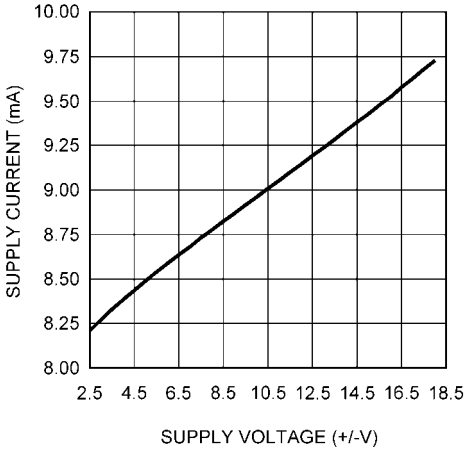
300442w5

Output Voltage vs Supply Voltage
R_L = 600Ω, 2kΩ, 10kΩ, THD+N ≤ 1%
80kHz BW



300442w6

Supply Current vs Supply Voltage
V_{IN} = 0V, R_L = No Load



300442u7

Application Information

GENERAL OPERATION

The LME49724 is a fully differential amplifier with an integrated common-mode reference input (V_{OCM}). Fully differential amplification provides increased noise immunity, high dynamic range, and reduced harmonic distortion products.

Differential amplifiers typically have high CMRR providing improved immunity from noise. When input, output, and supply line trace pairs are routed together, noise pick up is common and easily rejected by the LME49724. CMRR performance is directly proportional to the tolerance and matching of the gain configuring resistors. With 0.1% tolerance resistors the worst case CMRR performance will be about 60dB (20LOG (0.001)).

A differential output has a higher dynamic range than a single-ended output because of the doubling of output voltage. The dynamic range is increased by 6dB as a result of the outputs being equal in magnitude but opposite in phase. As an example, a single-ended output with a $1V_{PP}$ signal will be two $1V_{PP}$ signals with a differential output. The increase is 20LOG (2) = 6dB. Differential amplifiers are ideal for low voltage applications because of the increase in signal amplitude relative to a single-ended amplifier and the resulting improvement in SNR.

Differential amplifiers can also have reduced even order harmonics, all conditions equal, when compared to a single-ended amplifier. The differential output causes even harmonics to cancel between the two inverted outputs leaving only the odd harmonics. In practice even harmonics do not cancel completely, however there still is a reduction in total harmonic distortion.

OUTPUT COMMON-MODE VOLTAGE (V_{OCM} pin)

The output common-mode voltage is the DC voltage on each output. The output common-mode voltage is set by the V_{OCM} pin. The V_{OCM} pin can be driven by a low impedance source. If no voltage is applied to the V_{OCM} pin, the DC common-mode output voltage will be set by the internal resistor divider to the midpoint of the voltages on the V_{CC} and V_{EE} pins. The input impedance of the V_{OCM} pin is 50kΩ. The V_{OCM} pin can be driven up to V_{CC} - 1.5V and V_{EE} + 1.5V. The V_{OCM} pin should be bypassed to ground with a 0.1µF to 1µF capacitor. The V_{OCM} pin should be connected to ground when the desired output common-mode voltage is ground reference. The value of the external capacitor has an effect on the PSRR performance of the LME49724. With the V_{OCM} pin only bypassed with a low value capacitor, the PSRR performance of the LME49724 will be reduced, especially at low audio frequencies. For best PSRR performance, the V_{OCM} pin should be connected to stable, clean reference. Increasing the value of the bypass capacitor on the V_{OCM} pin will also improve PSRR performance.

ENABLE FUNCTION

The LME49724 can be placed into standby mode to reduce system current consumption by driving the ENABLE pin below V_{EE} + 1.75V. The LME49724 is active when the voltage on the ENABLE pin is above V_{EE} + 2.35V. The ENABLE pin should not be left floating. For best performance under all conditions, drive the ENABLE pin to the V_{EE} pin voltage to enter standby mode and to ground for active operation when operating from split supplies. When operating from a single supply, drive the ENABLE pin to ground for standby mode and to V_{CC} for active mode.

FULLY DIFFERENTIAL OPERATION

The LME49724 performs best in a fully differential configuration. The circuit shown in Figure 2 is the typical fully differential configuration.

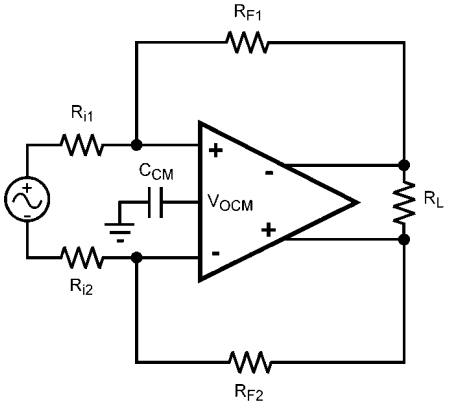


FIGURE 2. Fully Differential Configuration

The closed-loop gain is shown in Equation 1 below.

$$A_V = R_F / R_i \quad (V/V) \qquad (1)$$

Where $R_{F1} = R_{F2}$, $R_{i1} = R_{i2}$. Using low value resistors will give the lowest noise performance.

SINGLE-ENDED TO DIFFERENTIAL CONVERSION

For many applications, it is required to convert a single-ended signal to a differential signal. The LME49724 can be used for a high performance, simple single-to-differential converter. Figure 3 shows the typical single-to-differential converter circuit configuration.

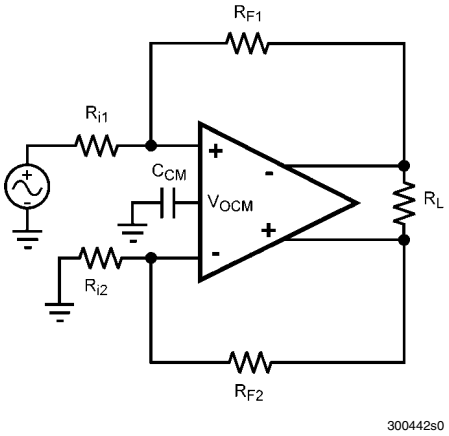


FIGURE 3. Single-Ended Input to Differential Output

SINGLE SUPPLY OPERATION

The LME49724 can be operated from a single power supply, as shown in Figure 4. The supply voltage range is limited to a minimum of 5V and a maximum of 36V. The common-mode output DC voltage will be set to the midpoint of the supply voltage. The V_{OCM} pin can be used to adjust the common-mode output DC voltage on the outputs, as described previously, if the supply voltage midpoint is not the desired DC voltage.

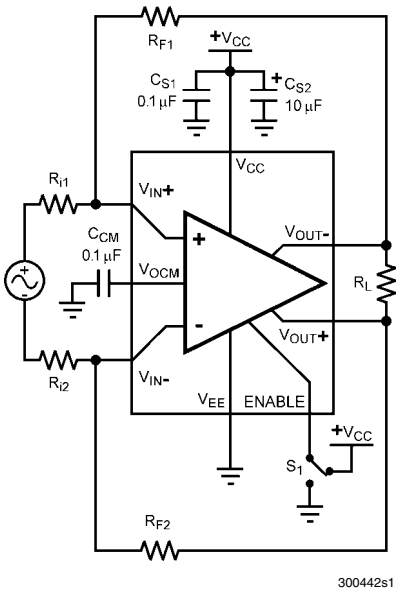


FIGURE 4. Single Supply Configuration

DRIVING A CAPACITIVE LOAD

The LME49724 is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 100pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 100pF must be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

THERMAL PCB DESIGN

The LME49724's high operating supply voltage along with its high output current capability can result in significant power dissipation. For this reason the LME49724 is provided in the exposed DAP MSOP (PSOP) package for improved thermal dissipation performance compared to other surface mount packages. The exposed pad is designed to be soldered to a copper plane on the PCB which then acts as a heat sink. The thermal plane can be on any layer by using multiple thermal vias under and outside the IC package. The vias under the IC should have solder mask openings for the entire pad under the IC on the top layer but cover the vias on the bottom layer. This method prevents solder from being pulled away from the thermal vias during the reflow process resulting in optimum thermal conductivity.

Heat radiation from the PCB plane area is best accomplished when the thermal plane is on the top or bottom copper layers. The LME49724 should always be soldered down to a copper pad on the PCB for both optimum thermal performance as well as mechanical stability.

The exposed pad is for heat transfer and the thermal plane should either be electrically isolated or connected to the same potential as the V_{EE} pin. For high frequency applications (f > 1MHz) or lower impedance loads, the pad should be connected to a plane that is connected to the V_{EE} potential.

SUPPLY BYPASSING

The LME49724 should have its supply leads bypassed with low-inductance capacitors such as leadless surface mount (SMT) capacitors located as close as possible to the supply pins. It is recommended that a 10µF tantalum or electrolytic capacitor be placed in parallel with a 0.1µF ceramic or film type capacitor on each supply pin. These capacitors should be star routed with a dedicated ground return plane or large trace for best THD performance. Placing capacitors too far from the power supply pins, especially with thin connecting traces, can lead to excessive inductance, resulting in degraded high-frequency bypassing. Poor high-frequency bypassing can result in circuit instabilities. When using high bandwidth power supplies, the value and number of supply bypass capacitors should be reduced for optimal power supply performance.

BALANCE CABLE DRIVER

With high peak-to-peak differential output voltage and plenty of low distortion drive current, the LME49724 makes an excellent balanced cable driver. Combining the single-to-differential configuration with a balanced cable driver results in a high performance single-ended input to balanced line driver solution.

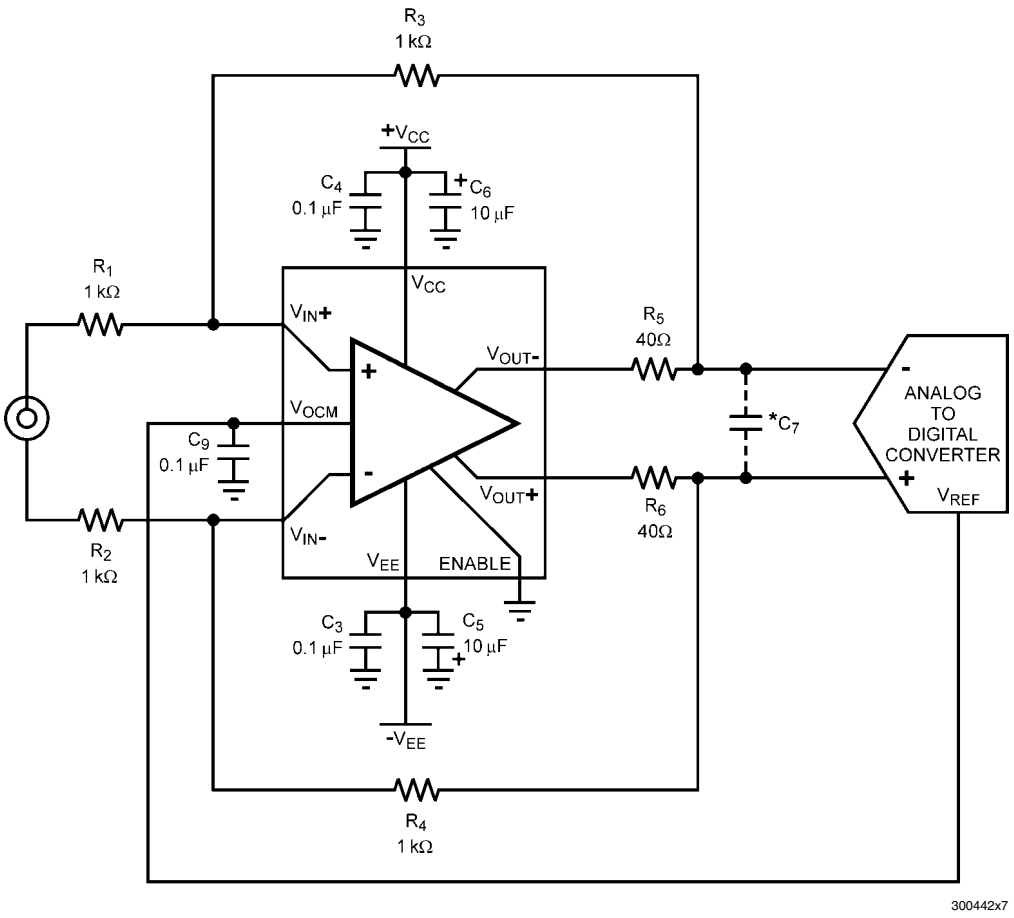
Although the LME49724 can drive capacitive loads up to 100pF, cable loads exceeding 100pF can cause instability. For such applications, series resistors are needed on the outputs before the capacitive load.

ANALOG-TO-DIGITAL CONVERTER (ADC) APPLICATION

Figure 5 is a typical fully differential application circuit for driving an analog-to-digital converter (ADC). The additional components of R_5, R_6, and C_7 are optional components and are for stability and proper ADC sampling. ADC's commonly use switched capacitor circuitry at the input. When the ADC samples the signal the current momentarily increases and may disturb the signal integrity at the sample point causing a signal glitch. Component C_7 is significantly larger than the input capacitance of a typical ADC and acts as a charge reservoir greatly reducing the effect of the signal sample by the ADC. Resistors R_5 and R_6 decouple the capacitive load, C_7, for stability. The values shown are general values. Specific values should be optimized for the particular ADC loading requirements.

The output reference voltage from the ADC can be used to drive the V_{OCM} pin to set the common-mode DC voltage on the outputs of the LME49724. A buffer may be needed to drive the LME49724's V_{OCM} pin if the ADC cannot drive the 50kΩ input impedance of the V_{OCM} pin.

In order to minimize circuit distortion when using capacitors in the signal path, the capacitors should be comprised of either NPO ceramic, polystyrene, polypropylene or mica composition. Other types of capacitors may provide a reduced distortion performance but for a cost improvement, so capacitor selection is dependent upon design requirements. The performance/cost tradeoff for a specific application is left up to the user.



***** Value is application and converted dependent.

FIGURE 5. Typical Analog-to-Digital Converter Circuit

DISTORTION MEASUREMENTS

The vanishing low residual distortion produced by the LME49724 is below the capabilities of commercially available equipment. This makes distortion measurements more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49724's low residual distortion is an input referred internal error. As shown in Figure 6, adding a resistor connected between the amplifier's inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is increased. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced, which means that measurement resolution increases. To ensure minimum effects on distortion measurements, keep the value of R_5 low. The distortion reading on the audio analyzer must be divided by a factor of $(R_3 + R_4)/R_5$, where $R_1 = R_2$ and $R_3 = R_4$, to get the actual measured distortion of the device under test. The values used for the LME49724 measurements were R_1, R_2, R_3, R_4 = 1kΩ and R_5 = 20Ω.

This technique is verified by duplicating the measurements with high closed-loop gain and/or making the measurements at high frequencies. Doing so produces distortion components that are within the measurement equipment's capabilities.

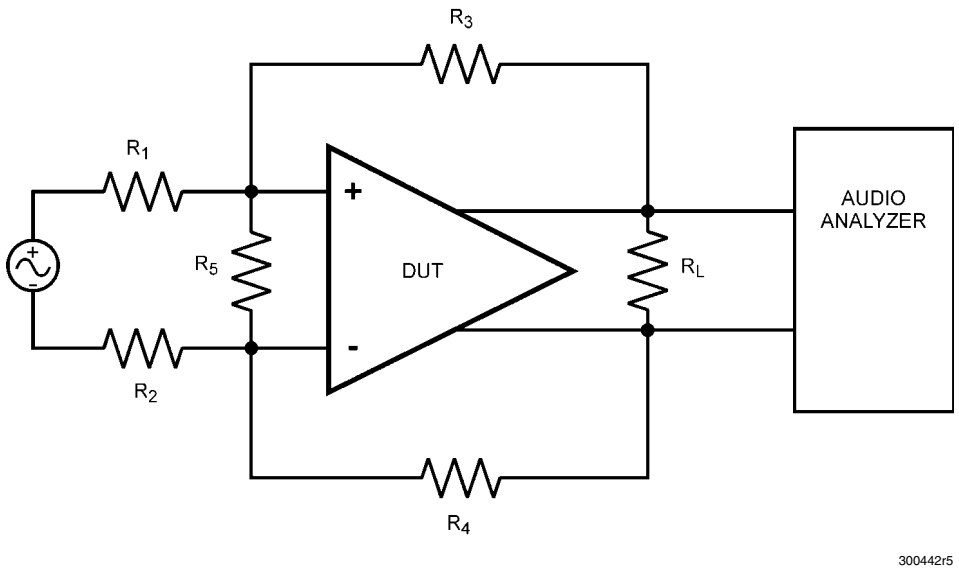


FIGURE 6. THD+N and IMD Distortion Test Circuit

PERFORMANCE VARIATIONS

The LME49724 has excellent performance with little variation across different supply voltages, load impedances, and input configuration (single-ended or differential). Inspection of the THD+N vs Frequency and THD+N vs Output Voltage performance graphs reveals only minimal differences with different load values. Figures 7 and 8 below show the performance across different supply voltages with the same output signal level and load. Figure 7 has plots at ±5V, ±12V, ±15V, and ±18V with a $3V_{RMS}$ output while Figure 8 has plots at ±12V, ±15V, and ±18V with a $10V_{RMS}$ output. Both figures use a 600Ω load. The performance for each different supply voltage under the same conditions is so similar it is nearly impossible to discern the different plots lines.

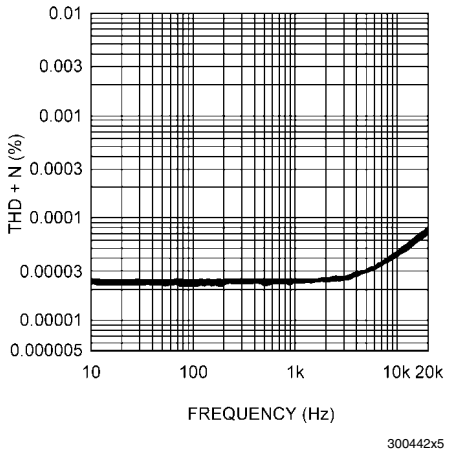


FIGURE 7. THD+N vs FREQUENCY with R_L = 600Ω V_{OUT} = $3V_{RMS}$, Differential Input, 80kHz BW V_S = ±5V, ±12V, ±15V, and ±18V

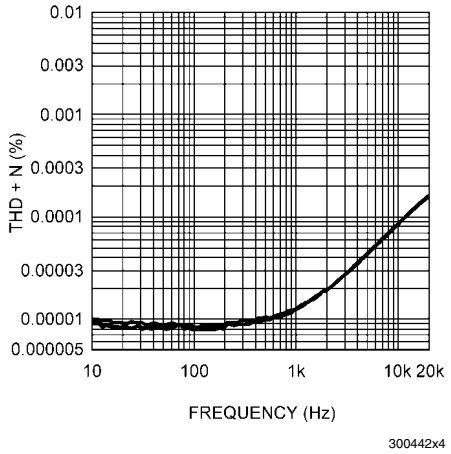


FIGURE 8. THD+N vs FREQUENCY with R_L = 600Ω V_{OUT} = $10V_{RMS}$, Differential Input, 80kHz BW V_S = ±12V, ±15V, and ±18V

Whether the input configuration is single-ended or differential has only a minimal affect on THD+N performance at higher audio frequencies or higher signal levels. For easy comparison, Figures 9 and 10 are a combination of the performance graphs found in the *Typical Performance Characteristics* section above.

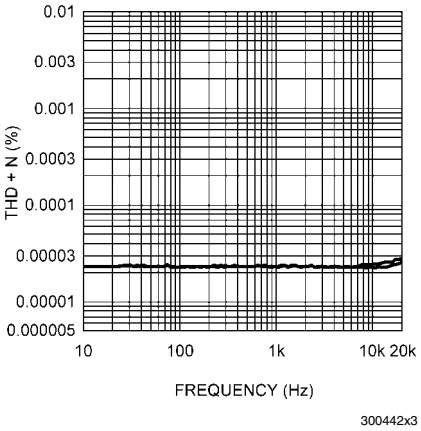


FIGURE 9. THD+N vs FREQUENCY with R_L = 10kΩ V_{OUT} = 3V_{RMS}, V_S = ±15V, 80kHz BW Single-ended and Differential Input

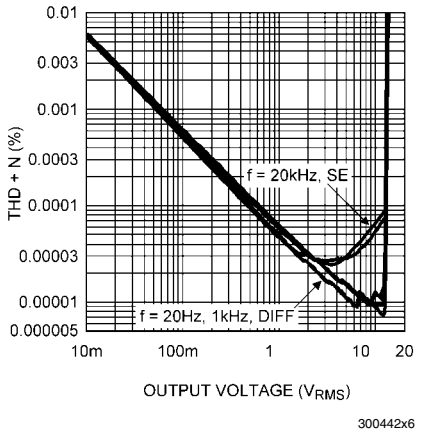


FIGURE 10. THD+N vs OUTPUT VOLTAGE with R_L = 10kΩ f = 20Hz, 1kHz, 20kHz, V_S = ±15V, 80kHz BW Single-ended and Differential Input

Power Supply Rejection Ratio does not vary with load value nor supply voltage. For easy comparison, Figures 11 and 12 below are created by combining performance graphs found in the *Typical Performance Characteristics* section above.

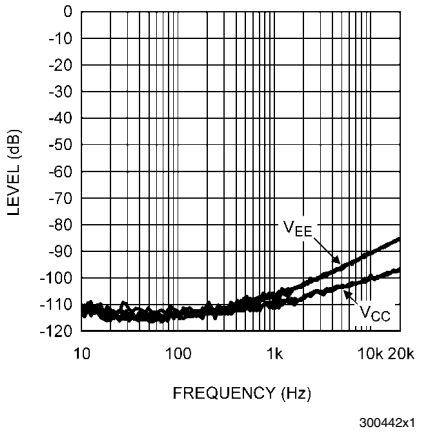


FIGURE 11. PSRR vs FREQUENCY with R_L = 600Ω

V_S = ±2.5V, ±15V, and ±18V, 80kHz BW

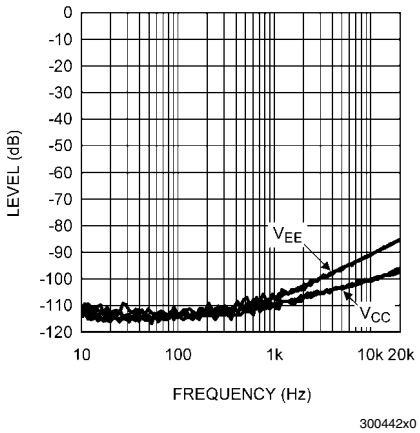


FIGURE 12. PSRR vs FREQUENCY with V_S = ±15V R_L = 600Ω, 2kΩ, and 10kΩ, 80kHz BW

Although supply current may not be a critical specification for many applications, there is also no real variation in supply current with no load or with a 600Ω load. This is a result of the extremely low offset voltage, typically less than 1mV. Figure 13 shows the supply current under the two conditions with no real difference discernable.

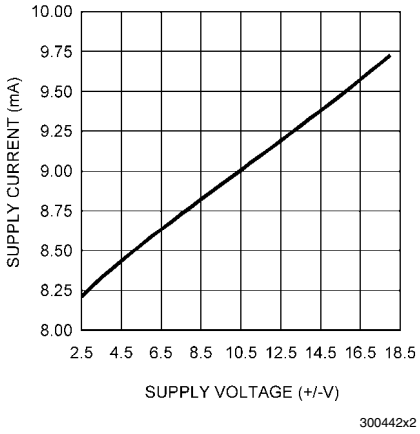


FIGURE 13. Supply Current vs Supply Voltage R_L = No Load and 600Ω

Demo Board Schematic

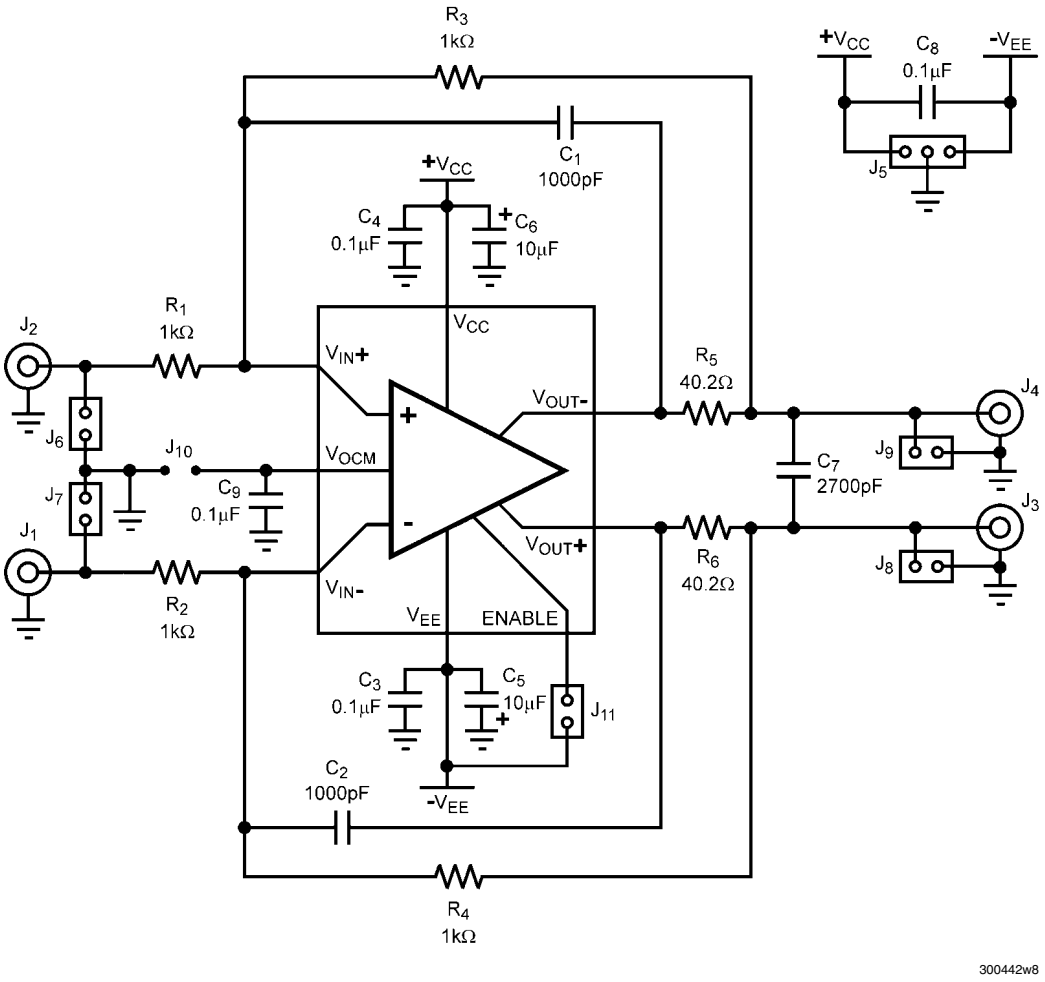


FIGURE 14. Demonstration Board Circuit

Build of Materials

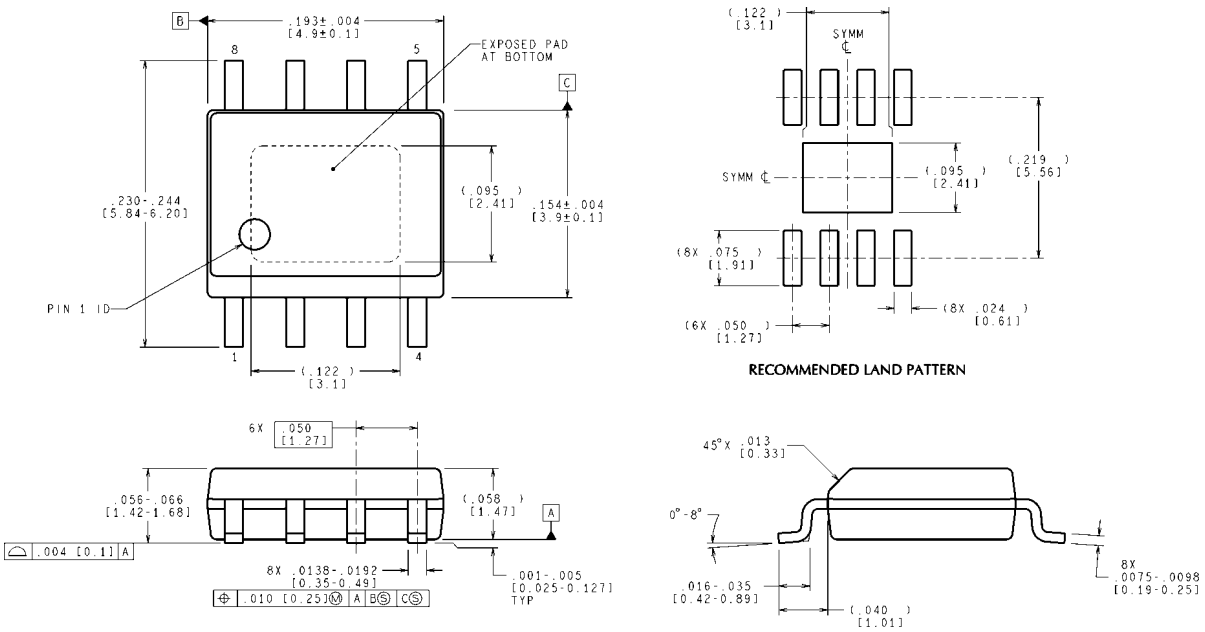
TABLE 1. Reference Demo Board Bill of Materials

Designator	Value	Tolerance	Part Description	Comment
R_1, R_2, R_3, R_4	1kΩ	1%	1/8W, 0603 Resistor	
R_5, R_6	40.2Ω	1%	1/8W, 0603 Resistor	
C_1, C_2	1000pF	10%	0603, NPO Ceramic Capacitor, 50V	
C_3, C_4, C_8, C_9	0.1µF	–20%, +80%	0603, Y5V Ceramic Capacitor, 25V	
C_5, C_6	10µF	20%	Size C (6032), Tantalum Capacitor, 25V	
C_7	2700pF	10%	0805, NPO Ceramic Capacitor, 50V	
U_1			LME49724MR	
J_1, J_2, J_3, J_4			SMA coaxial connector	Inputs & Outputs
J_5			0.100" 1x3 header, vertical mount	V_{DD}, V_{EE}, GND
J_6, J_7, J_8, J_9, J_{10}, J_{11}			0.100" 1x2 header, vertical mount	Inputs, Outputs, V_{OCM}, Enable

Revision History

Rev	Date	Description
1.0	11/12/08	Initial release.

Physical Dimensions inches (millimeters) unless otherwise noted



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Notes

Notes

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