

LMP7732

2.9 nV/sqrt(Hz) Low Noise, RRIO Amplifier

General Description

The LMP7732 is a dual low noise, rail-to-rail input and output, low voltage amplifier. The LMP7732 is part of the LMP® amplifier family and is ideal for precision and low noise applications with low voltage requirements.

This operational amplifier offers low voltage noise of 2.9 nV/√Hz with a 1/f corner of only 3 Hz. The LMP7732 has bipolar junction input stages with a bias current of only 1.5 nA. This low input bias current, complemented by the very low level of voltage noise, makes the LMP7732 an excellent choice for photometry applications.

The LMP7732 provides a wide GBW of 22 MHz while consuming only 4 mA of current. This high gain bandwidth along with the high open loop gain of 130 dB enables accurate signal conditioning in applications with high closed loop gain requirements.

The LMP7732 has a supply voltage range of 1.8V to 5.5V, making it an ideal choice for battery operated portable applications.

The LMP7732 is offered in the 8-Pin SOIC and MSOP packages.

The LMP7731 is the single version of this product and is offered in the 5-Pin SOT-23 and 8-Pin SOIC packages.

Features

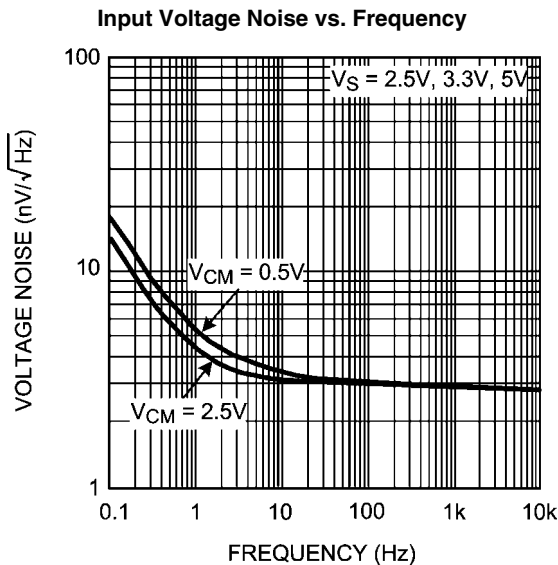
(Typical values, $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$)

| | |
|--|----------------|
| ■ Input voltage noise | |
| — $f = 3\text{ Hz}$ | 3.3 nV/√Hz |
| — $f = 1\text{ kHz}$ | 2.9 nV/√Hz |
| ■ CMRR | 130 dB |
| ■ Open loop gain | 130 dB |
| ■ GBW | 22 MHz |
| ■ Slew rate | 2.4 V/μs |
| ■ THD @ $f = 10\text{ kHz}$, $A_V = 1$, $R_L = 2\text{ k}\Omega$ | 0.001% |
| ■ Supply current | 4.4 mA |
| ■ Supply voltage range | 1.8V to 5.5V |
| ■ Operating temperature range | -40°C to 125°C |
| ■ Input bias current | ±1.5 nA |
| ■ RRIO | |

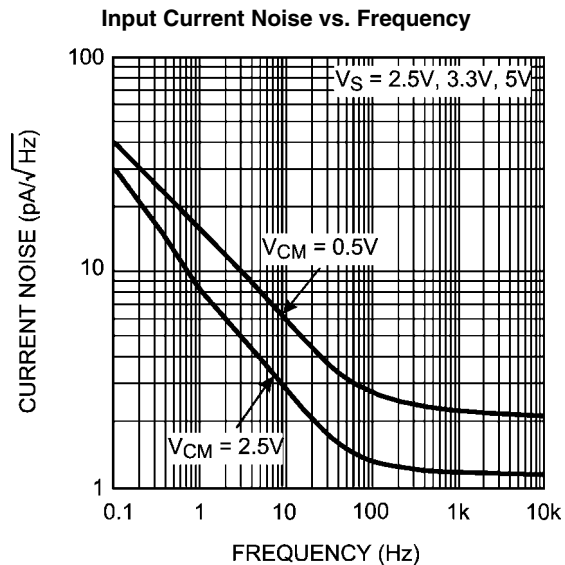
Applications

- Gas analysis instruments
- Photometric instrumentation
- Medical instrumentation

Typical Performance Characteristics



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)

Human Body Model

For inputs pins only

2000V

For all other pins

2000V

Machine Model

200V

Charge Device Model

1000V

V_{IN} Differential

$\pm 2V$

Supply Voltage ($V_S = V^+ - V^-$)

6.0V

Storage Temperature Range

-65°C to 150°C

Junction Temperature (Note 3)

$+150^\circ\text{C}$ max

Soldering Information

Infrared or Convection (20 sec)

235°C

Wave Soldering Lead Temp. (10 sec)

260°C

Operating Ratings (Note 1)

Temperature Range

-40°C to 125°C

Supply Voltage ($V_S = V^+ - V^-$)

1.8V to 5.5V

Package Thermal Resistance (θ_{JA})

8-Pin SOIC

190°C/W

8-Pin MSOP

235°C/W

2.5V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 2.5V$, $V^- = 0V$, $V_{CM} = V^+/2$, $R_L > 10\text{ k}\Omega$ to $V^+/2$. **Bold-face** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min (Note 6) | Typ (Note 5) | Max (Note 6) | Units |
|------------|--|---------------------------------------|-------------------|-----------------|--|------------------------------|
| V_{OS} | Input Offset Voltage (Note 7) | $V_{CM} = 2.0V$ | | ± 9 | ± 500 ± 600 | μV |
| | | $V_{CM} = 0.5V$ | | ± 9 | ± 500 ± 600 | |
| TCV_{OS} | Input Offset Voltage Temperature Drift | $V_{CM} = 2.0V$ | | ± 0.5 | ± 5.5 | $\mu\text{V}/^\circ\text{C}$ |
| | | $V_{CM} = 0.5V$ | | ± 0.2 | ± 5.5 | |
| I_B | Input Bias Current | $V_{CM} = 2.0V$ | | ± 1 | ± 30 ± 45 | nA |
| | | $V_{CM} = 0.5V$ | | ± 12 | ± 50 ± 75 | |
| I_{OS} | Input Offset Current | $V_{CM} = 2.0V$ | | ± 1 | ± 50 ± 75 | nA |
| | | $V_{CM} = 0.5V$ | | ± 11 | ± 60 ± 80 | |
| TCI_{OS} | Input Offset Current Drift | $V_{CM} = 0.5V$ and $V_{CM} = 2.0V$ | | 0.0474 | | $\text{nA}/^\circ\text{C}$ |
| CMRR | Common Mode Rejection Ratio | $0.15V \leq V_{CM} \leq 0.7V$ | 101 | 120 | | dB |
| | | $0.23V \leq V_{CM} \leq 0.7V$ | 89 | | | |
| | | $1.5V \leq V_{CM} \leq 2.35V$ | 105 | 129 | | |
| | | $1.5V \leq V_{CM} \leq 2.27V$ | 99 | | | |
| PSRR | Power Supply Rejection Ratio | $2.5V \leq V^+ \leq 5V$ | 111 105 | 129 | | dB |
| | | $1.8V \leq V^+ \leq 5.5V$ | | 117 | | |
| CMVR | Common Mode Voltage Range | Large Signal CMRR $\geq 80\text{ dB}$ | 0 | | 2.5 | V |
| A_{VOL} | Open Loop Voltage Gain | $R_L = 10\text{ k}\Omega$ to $V^+/2$ | 112 | 130 | | dB |
| | | $V_{OUT} = 0.5V$ to $2.0V$ | 104 | | | |
| | | $R_L = 2\text{ k}\Omega$ to $V^+/2$ | 109 | 119 | | |
| | | $V_{OUT} = 0.5V$ to $2.0V$ | 90 | | | |

| Symbol | Parameter | Conditions | Min (Note 6) | Typ (Note 5) | Max (Note 6) | Units |
|-----------|--------------------------------------|---|-----------------|-----------------|-------------------|------------------------|
| V_{OUT} | Output Voltage Swing High | $R_L = 10\text{ k}\Omega$ to $V+/2$ | | 4 | 50 75 | mV from either rail |
| | | $R_L = 2\text{ k}\Omega$ to $V+/2$ | | 13 | 50 75 | |
| | Output Voltage Swing Low | $R_L = 10\text{ k}\Omega$ to $V+/2$ | | 6 | 50 75 | |
| | | $R_L = 2\text{ k}\Omega$ to $V+/2$ | | 9 | 50 75 | |
| I_{OUT} | Output Current | Sourcing, $V_{OUT} = V+/2$ $V_{IN}(\text{diff}) = 100\text{ mV}$ | 22 12 | 31 | | mA |
| | | Sinking, $V_{OUT} = V+/2$ $V_{IN}(\text{diff}) = -100\text{ mV}$ | 15 10 | 44 | | |
| | | | | | | |
| I_S | Supply Current | $V_{CM} = 2.0\text{V}$ | | 4.0 | 5.4 6.8 | mA |
| | | $V_{CM} = 0.5\text{V}$ | | 4.6 | 6.2 7.8 | |
| SR | Slew Rate | $A_V = +1$, $C_L = 10\text{ pF}$, $R_L = 10\text{ k}\Omega$ to $V+/2$ $V_{OUT} = 2 V_{PP}$ | | 2.4 | | V/ μs |
| GBW | Gain Bandwidth | $C_L = 20\text{ pF}$, $R_L = 10\text{ k}\Omega$ to $V+/2$ | | 21 | | MHz |
| G_M | Gain Margin | $C_L = 20\text{ pF}$, $R_L = 10\text{ k}\Omega$ to $V+/2$ | | 14 | | dB |
| Φ_M | Phase Margin | $C_L = 20\text{ pF}$, $R_L = 10\text{ k}\Omega$ to $V+/2$ | | 60 | | deg |
| R_{IN} | Input Resistance | Differential Mode | | 38 | | k Ω |
| | | Common Mode | | 151 | | M Ω |
| THD+N | Total Harmonic Distortion + Noise | $A_V = 1$, $f_O = 1\text{ kHz}$, Amplitude = 1V | | 0.002 | | % |
| e_n | Input Referred Voltage Noise Density | $f = 1\text{ kHz}$, $V_{CM} = 2.0\text{V}$ | | 3.0 | | nV/ $\sqrt{\text{Hz}}$ |
| | | $f = 1\text{ kHz}$, $V_{CM} = 0.5\text{V}$ | | 3.0 | | |
| | Input Voltage Noise | 0.1 Hz to 10 Hz | | 75 | | nV $_{PP}$ |
| i_n | Input Referred Current Noise Density | $f = 1\text{ kHz}$, $V_{CM} = 2.0\text{V}$ | | 1.1 | | pA/ $\sqrt{\text{Hz}}$ |
| | | $f = 1\text{ kHz}$, $V_{CM} = 0.5\text{V}$ | | 2.3 | | |

3.3V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 3.3\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V+/2$, $R_L > 10\text{ k}\Omega$ to $V+/2$. **Bold-face** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min (Note 6) | Typ (Note 5) | Max (Note 6) | Units |
|------------|--|------------------------|-----------------|-----------------|--|------------------------------|
| V_{OS} | Input Offset Voltage (Note 7) | $V_{CM} = 2.5\text{V}$ | | ± 6 | ± 500 ± 600 | μV |
| | | $V_{CM} = 0.5\text{V}$ | | ± 6 | ± 500 ± 600 | |
| TCV_{OS} | Input Offset Voltage Temperature Drift | $V_{CM} = 2.5\text{V}$ | | ± 0.5 | ± 5.5 | $\mu\text{V}/^\circ\text{C}$ |
| | | $V_{CM} = 0.5\text{V}$ | | ± 0.2 | ± 5.5 | |
| I_B | Input Bias Current | $V_{CM} = 2.5\text{V}$ | | ± 1.5 | ± 30 ± 45 | nA |
| | | $V_{CM} = 0.5\text{V}$ | | ± 13 | ± 50 ± 77 | |
| I_{OS} | Input Offset Current | $V_{CM} = 2.5\text{V}$ | | ± 1 | ± 50 ± 70 | nA |
| | | $V_{CM} = 0.5\text{V}$ | | ± 11 | ± 60 ± 80 | |

| Symbol | Parameter | Conditions | Min (Note 6) | Typ (Note 5) | Max (Note 6) | Units |
|------------------------------|--------------------------------------|--|-----------------|-----------------|-----------------|------------------------|
| TC _{I_{OS}} | Input Offset Current Drift | $V_{CM} = 0.5V$ and $V_{CM} = 2.5V$ | | 0.048 | | nA/°C |
| CMRR | Common Mode Rejection Ratio | $0.15V \leq V_{CM} \leq 0.7V$ $0.23V \leq V_{CM} \leq 0.7V$ | 101 89 | 120 | | dB |
| | | $1.5V \leq V_{CM} \leq 3.15V$ $1.5V \leq V_{CM} \leq 3.07V$ | 105 99 | 130 | | |
| PSRR | Power Supply Rejection Ratio | $2.5V \leq V^+ \leq 5.0V$ | 111 105 | 129 | | dB |
| | | $1.8V \leq V^+ \leq 5.5V$ | | 117 | | |
| CMVR | Common Mode Voltage Range | Large Signal CMRR ≥ 80 dB | 0 | | 3.3 | V |
| A _{VOL} | Open Loop Voltage Gain | $R_L = 10\text{ k}\Omega$ to $V^{+}/2$ $V_{OUT} = 0.5V$ to $2.8V$ | 112 104 | 130 | | dB |
| | | $R_L = 2\text{ k}\Omega$ to $V^{+}/2$ $V_{OUT} = 0.5V$ to $2.8V$ | 110 92 | 119 | | |
| V _{OUT} | Output Voltage Swing High | $R_L = 10\text{ k}\Omega$ to $V^{+}/2$ | | 5 | 50 75 | mV from either rail |
| | | $R_L = 2\text{ k}\Omega$ to $V^{+}/2$ | | 14 | 50 75 | |
| | Output Voltage Swing Low | $R_L = 10\text{ k}\Omega$ to $V^{+}/2$ | | 9 | 50 75 | |
| | | $R_L = 2\text{ k}\Omega$ to $V^{+}/2$ | | 13 | 50 75 | |
| I _{OUT} | Output Current | Sourcing, $V_{OUT} = V^{+}/2$ $V_{IN}(\text{diff}) = 100\text{ mV}$ | 28 22 | 45 | | mA |
| | | Sinking, $V_{OUT} = V^{+}/2$ $V_{IN}(\text{diff}) = -100\text{ mV}$ | 25 20 | 48 | | |
| I _S | Supply Current | $V_{CM} = 2.5V$ | | 4.2 | 5.6 7.0 | mA |
| | | $V_{CM} = 0.5V$ | | 4.8 | 6.4 8.0 | |
| SR | Slew Rate | $A_V = +1$, $C_L = 10\text{ pF}$, $R_L = 10\text{ k}\Omega$ to $V^{+}/2$ $V_{OUT} = 2 V_{PP}$ | | 2.4 | | V/ μ s |
| GBW | Gain Bandwidth | $C_L = 20\text{ pF}$, $R_L = 10\text{ k}\Omega$ to $V^{+}/2$ | | 22 | | MHz |
| G _M | Gain Margin | $C_L = 20\text{ pF}$, $R_L = 10\text{ k}\Omega$ to $V^{+}/2$ | | 14 | | dB |
| Φ_M | Phase Margin | $C_L = 20\text{ pF}$, $R_L = 10\text{ k}\Omega$ to $V^{+}/2$ | | 62 | | deg |
| THD+N | Total Harmonic Distortion + Noise | $A_V = 1$, $f_O = 1\text{ kHz}$, Amplitude = 1V | | 0.002 | | % |
| R _{IN} | Input Resistance | Differential Mode | | 38 | | k Ω |
| | | Common Mode | | 151 | | M Ω |
| e _n | Input Referred Voltage Noise Density | $f = 1\text{ kHz}$, $V_{CM} = 2.5V$ | | 2.9 | | nV/ $\sqrt{\text{Hz}}$ |
| | | $f = 1\text{ kHz}$, $V_{CM} = 0.5V$ | | 2.9 | | |
| | Input Voltage Noise | 0.1 Hz to 10 Hz | | 75 | | nV _{PP} |
| i _n | Input Referred Current Noise Density | $f = 1\text{ kHz}$, $V_{CM} = 2.5V$ | | 1.1 | | pA/ $\sqrt{\text{Hz}}$ |
| | | $f = 1\text{ kHz}$, $V_{CM} = 0.5V$ | | 2.1 | | |

5V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V^+/2$, $R_L > 10\text{ k}\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min (Note 6) | Typ (Note 5) | Max (Note 6) | Units |
|--------------------------|--|--|-------------------|-----------------|--|------------------------------|
| V_{OS} | Input Offset Voltage (Note 7) | $V_{\text{CM}} = 4.5\text{V}$ | | ± 6 | ± 500 ± 600 | μV |
| | | $V_{\text{CM}} = 0.5\text{V}$ | | ± 6 | ± 500 ± 600 | |
| TCV_{OS} | Input Offset Voltage Temperature Drift | $V_{\text{CM}} = 4.5\text{V}$ | | ± 0.5 | ± 5.5 | $\mu\text{V}/^\circ\text{C}$ |
| | | $V_{\text{CM}} = 0.5\text{V}$ | | ± 0.2 | ± 5.5 | |
| I_{B} | Input Bias Current | $V_{\text{CM}} = 4.5\text{V}$ | | ± 1.5 | ± 30 ± 50 | nA |
| | | $V_{\text{CM}} = 0.5\text{V}$ | | ± 14 | ± 50 ± 85 | |
| I_{OS} | Input Offset Current | $V_{\text{CM}} = 4.5\text{V}$ | | ± 1 | ± 50 ± 70 | nA |
| | | $V_{\text{CM}} = 0.5\text{V}$ | | ± 11 | ± 65 ± 80 | |
| TCI_{OS} | Input Offset Current Drift | $V_{\text{CM}} = 0.5\text{V}$ and $V_{\text{CM}} = 4.5\text{V}$ | | 0.0482 | | nA/ $^\circ\text{C}$ |
| CMRR | Common Mode Rejection Ratio | $0.15\text{V} \leq V_{\text{CM}} \leq 0.7\text{V}$ | 101 | 120 | | dB |
| | | $0.23\text{V} \leq V_{\text{CM}} \leq 0.7\text{V}$ | 89 | | | |
| | | $1.5\text{V} \leq V_{\text{CM}} \leq 4.85\text{V}$ | 105 | 130 | | |
| | | $1.5\text{V} \leq V_{\text{CM}} \leq 4.77\text{V}$ | 99 | | | |
| PSRR | Power Supply Rejection Ratio | $2.5\text{V} \leq V^+ \leq 5\text{V}$ | 111 105 | 129 | | dB |
| | | $1.8\text{V} \leq V^+ \leq 5.5\text{V}$ | | 117 | | |
| CMVR | Common Mode Voltage Range | Large Signal CMRR $\geq 80\text{ dB}$ | 0 | | 5 | V |
| A_{VOL} | Open Loop Voltage Gain | $R_L = 10\text{ k}\Omega$ to $V^+/2$ $V_{\text{OUT}} = 0.5\text{V}$ to 4.5V | 112 104 | 130 | | dB |
| | | $R_L = 2\text{ k}\Omega$ to $V^+/2$ $V_{\text{OUT}} = 0.5\text{V}$ to 4.5V | 110 94 | 119 | | |
| V_{OUT} | Output Voltage Swing High | $R_L = 10\text{ k}\Omega$ to $V^+/2$ | | 8 | 50 75 | mV from either rail |
| | | $R_L = 2\text{ k}\Omega$ to $V^+/2$ | | 24 | 50 75 | |
| | Output Voltage Swing Low | $R_L = 10\text{ k}\Omega$ to $V^+/2$ | | 9 | 50 75 | |
| | | $R_L = 2\text{ k}\Omega$ to $V^+/2$ | | 23 | 50 75 | |
| I_{OUT} | Output Current | Sourcing, $V_{\text{OUT}} = V^+/2$ $V_{\text{IN}}(\text{diff}) = 100\text{ mV}$ | 33 27 | 47 | | mA |
| | | Sinking, $V_{\text{OUT}} = V^+/2$ $V_{\text{IN}}(\text{diff}) = -100\text{ mV}$ | 30 25 | 49 | | |
| I_{S} | Supply Current | $V_{\text{CM}} = 4.5\text{V}$ | | 4.4 | 6.0 7.4 | mA |
| | | $V_{\text{CM}} = 0.5\text{V}$ | | 5.0 | 6.8 8.4 | |
| SR | Slew Rate | $A_V = +1$, $C_L = 10\text{ pF}$, $R_L = 10\text{ k}\Omega$ to $V^+/2$ $V_{\text{OUT}} = 2 V_{\text{PP}}$ | | 2.4 | | V/ μs |
| GBW | Gain Bandwidth | $C_L = 20\text{ pF}$, $R_L = 10\text{ k}\Omega$ to $V^+/2$ | | 22 | | MHz |

| Symbol | Parameter | Conditions | Min (Note 6) | Typ (Note 5) | Max (Note 6) | Units |
|----------|--------------------------------------|--|--------------|--------------|--------------|------------------------|
| G_M | Gain Margin | $C_L = 20 \text{ pF}, R_L = 10 \text{ k}\Omega \text{ to } V+/2$ | | 12 | | dB |
| Φ_M | Phase Margin | $C_L = 20 \text{ pF}, R_L = 10 \text{ k}\Omega \text{ to } V+/2$ | | 65 | | deg |
| R_{IN} | Input Resistance | Differential Mode | | 38 | | k Ω |
| | | Common Mode | | 151 | | M Ω |
| THD+ N | Total Harmonic Distortion + Noise | $A_V = 1, f_O = 1 \text{ kHz}, \text{Amplitude} = 1V$ | | 0.001 | | % |
| e_n | Input Referred Voltage Noise Density | $f = 1 \text{ kHz}, V_{CM} = 4.5V$ | | 2.9 | | nV/ $\sqrt{\text{Hz}}$ |
| | | $f = 1 \text{ kHz}, V_{CM} = 0.5V$ | | 2.9 | | |
| | Input Voltage Noise | 0.1 Hz to 10 Hz | | 75 | | nV _{PP} |
| i_n | Input Referred Current Noise Density | $f = 1 \text{ kHz}, V_{CM} = 4.5V$ | | 1.1 | | pA/ $\sqrt{\text{Hz}}$ |
| | | $f = 1 \text{ kHz}, V_{CM} = 0.5V$ | | 2.2 | | |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

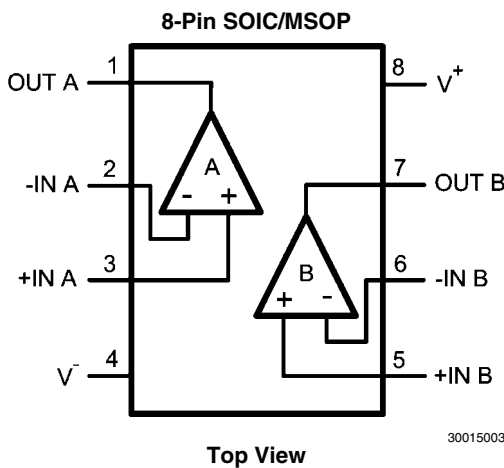
Note 4: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute maximum Ratings indicate junction temperature limits beyond which the device maybe permanently degraded, either mechanically or electrically.

Note 5: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 6: All limits are guaranteed by testing, statistical analysis or design.

Note 7: Ambient production test is performed at 25°C with a variance of $\pm 3^\circ\text{C}$.

Connection Diagram

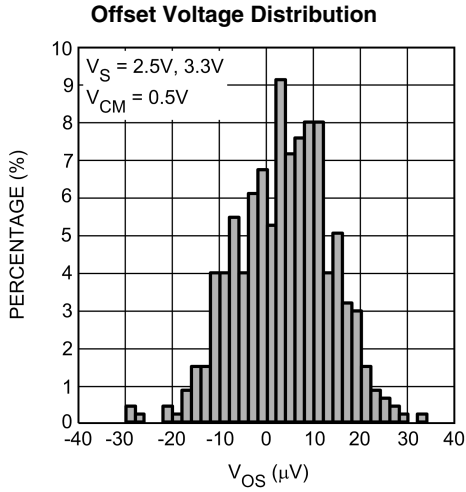


Ordering Information

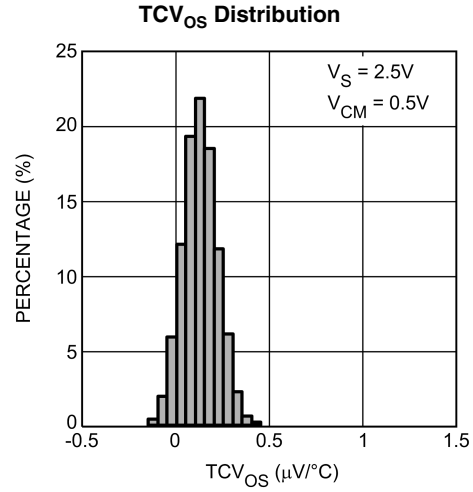
| Package | Part Number | Package Marking | Transport Media | NSC Drawing |
|------------|-------------|-----------------|--------------------------|-------------|
| 8-Pin SOIC | LMP7732MA | LMP7732MA | 95 units/Rails | M08A |
| | LMP7732MAX | | 2.5k Units Tape and Reel | |
| 8-Pin MSOP | LMP7732MM | AZ3A | 1k Units Tape and Reel | MUA08A |
| | LMP7732MME | | 250 Units Tape and Reel | |
| | LMP7732MMX | | 3.5k Units Tape and Reel | |

Typical Performance Characteristics

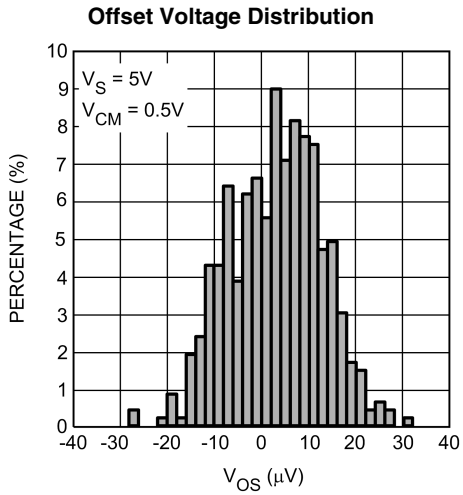
Unless otherwise noted: $T_A = 25^\circ\text{C}$, $R_L > 10\text{ k}\Omega$, $V_{CM} = V_S/2$.



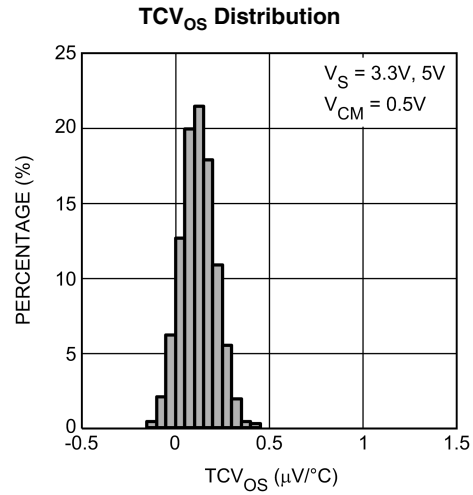
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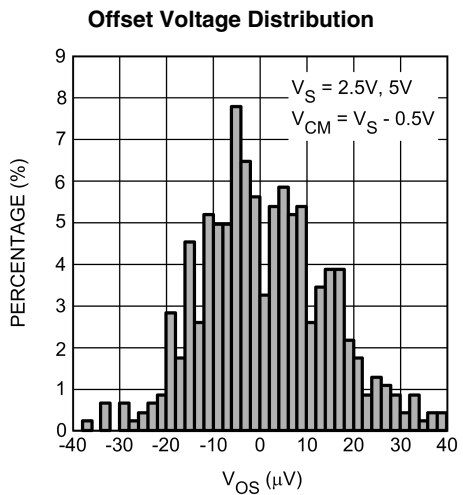
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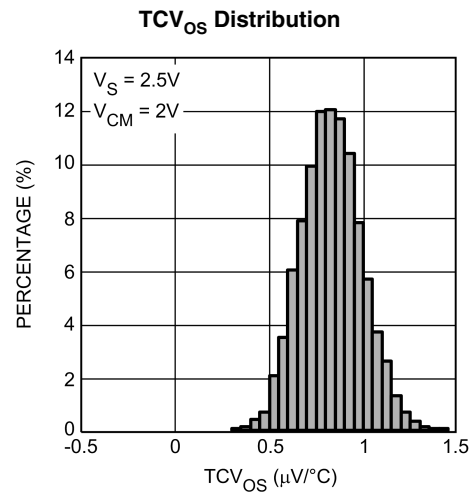
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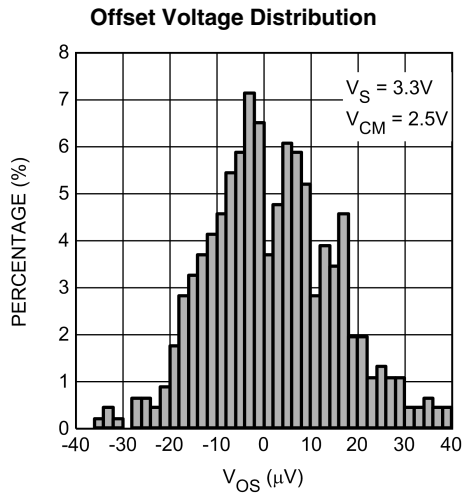
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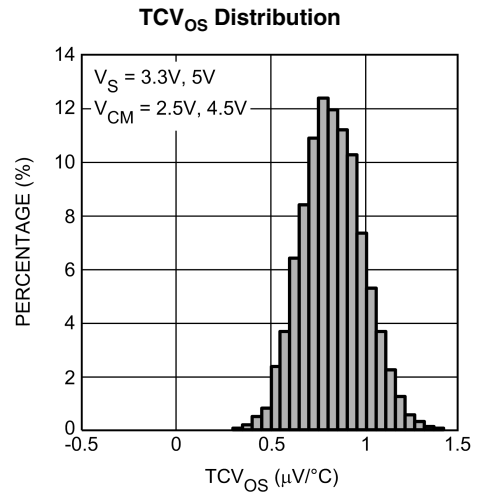
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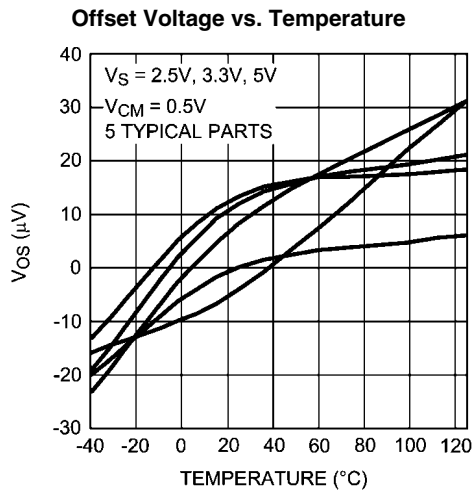
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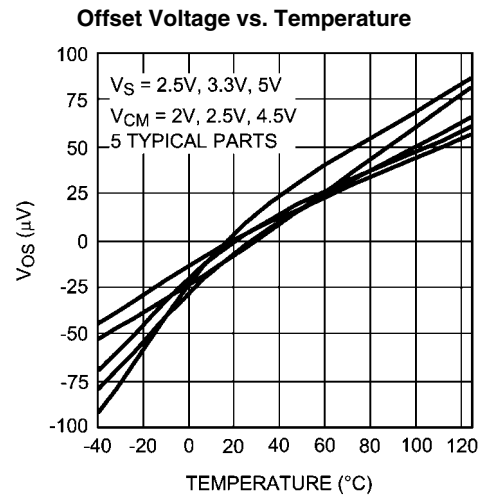
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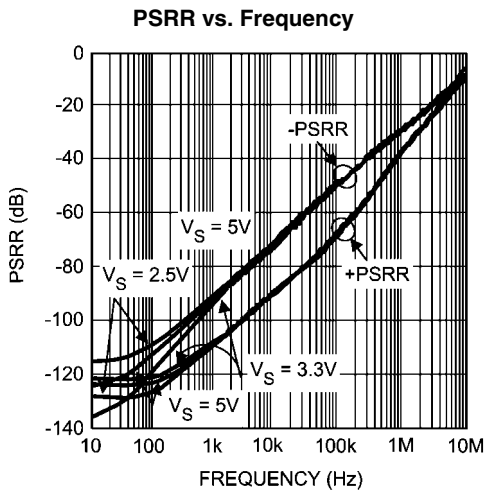
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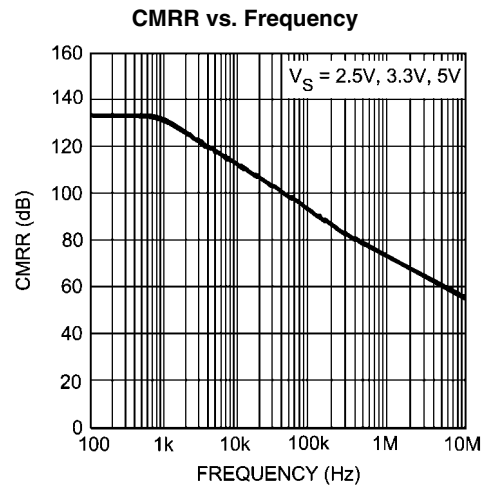
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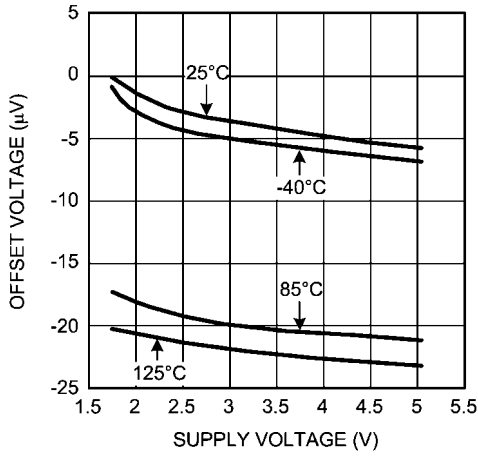


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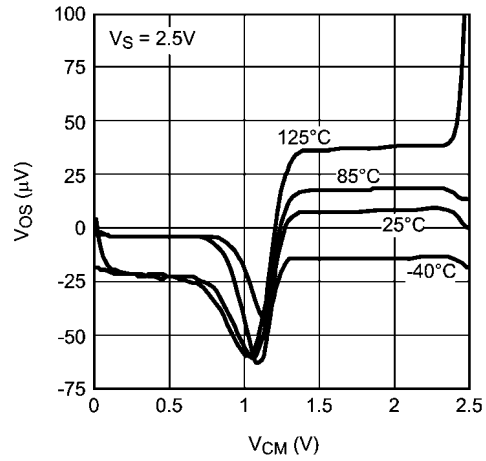
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Offset Voltage vs. Supply Voltage



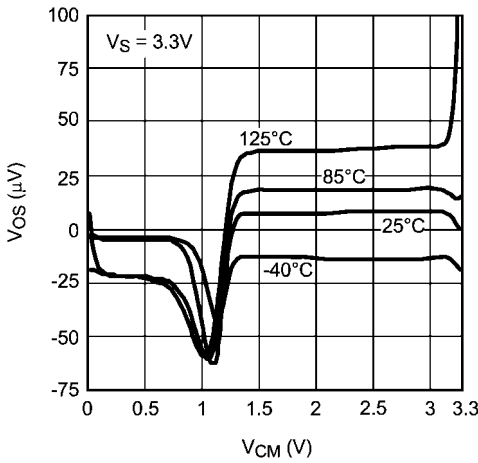
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Offset Voltage vs. V_{CM}



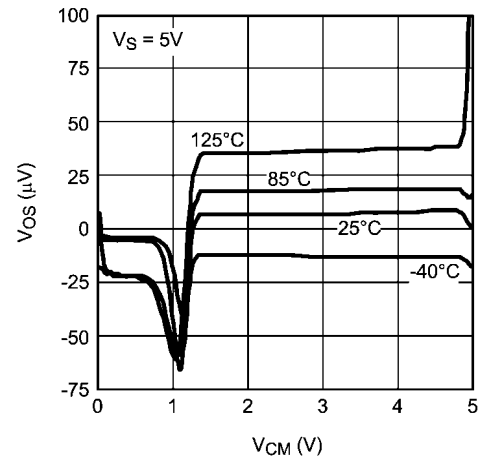
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Offset Voltage vs. V_{CM}



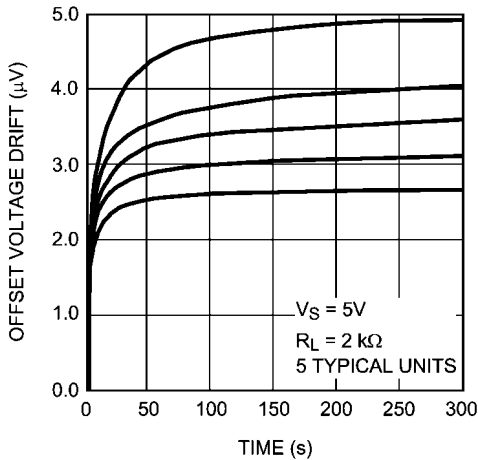
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Offset Voltage vs. V_{CM}



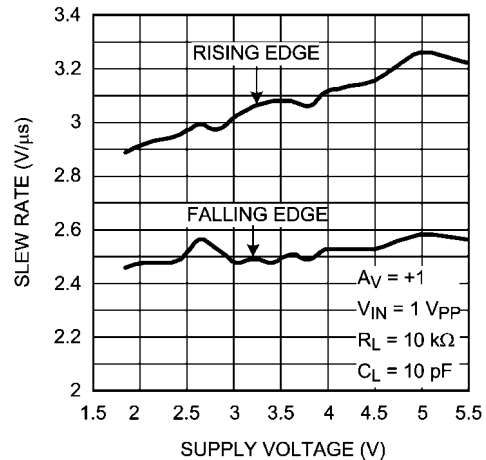
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Input Offset Voltage Time Drift



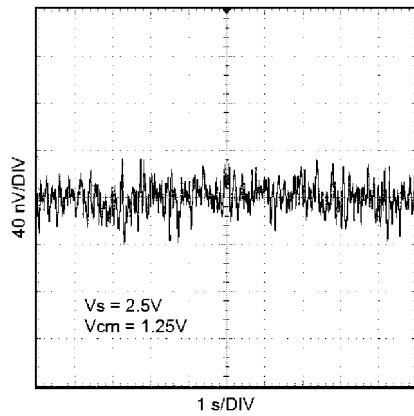
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Slew Rate vs. Supply Voltage



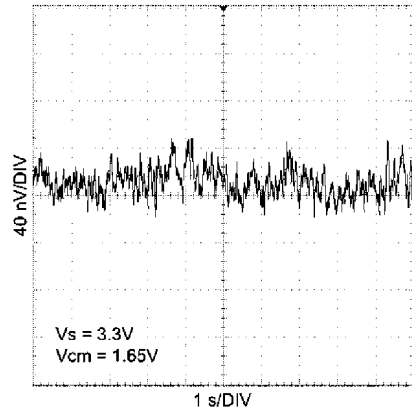
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Time Domain Voltage Noise



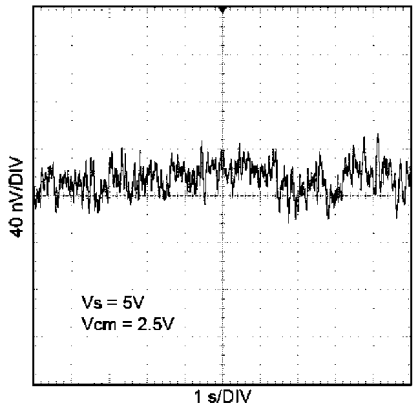
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Time Domain Voltage Noise



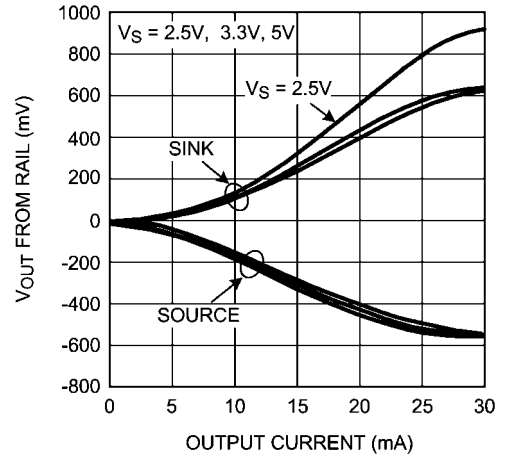
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Time Domain Voltage Noise



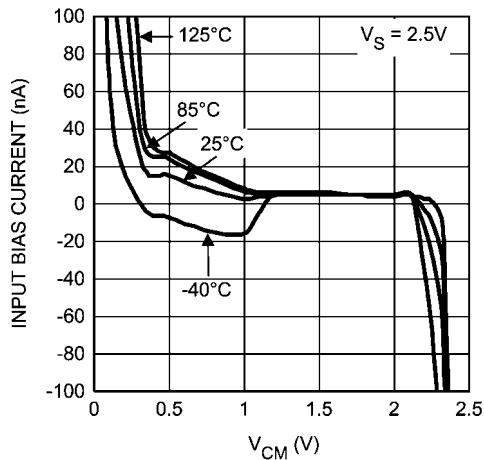
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Output Voltage vs. Output Current



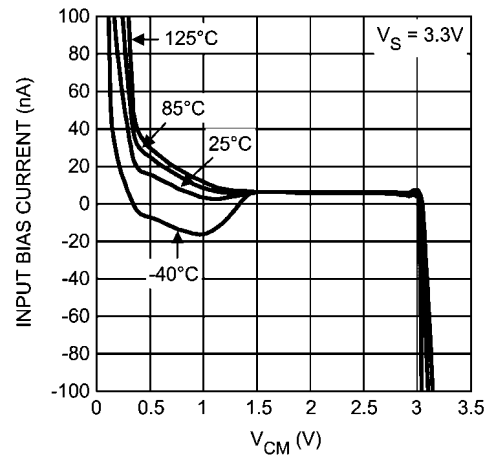
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Input Bias Current vs. V_{CM}

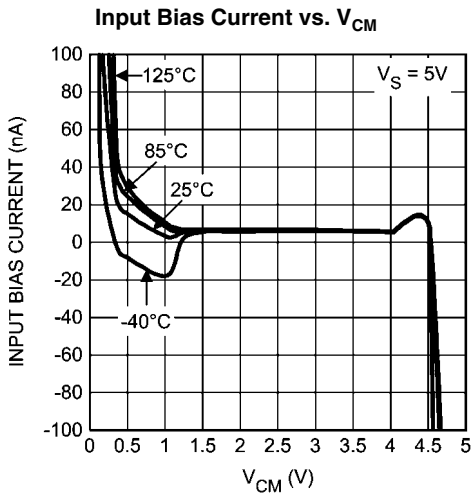


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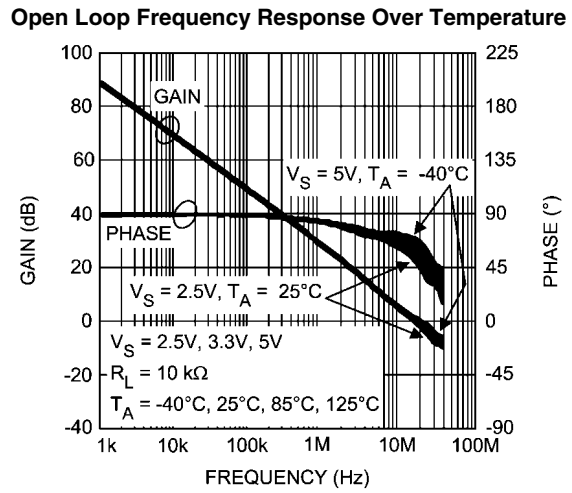
Input Bias Current vs. V_{CM}



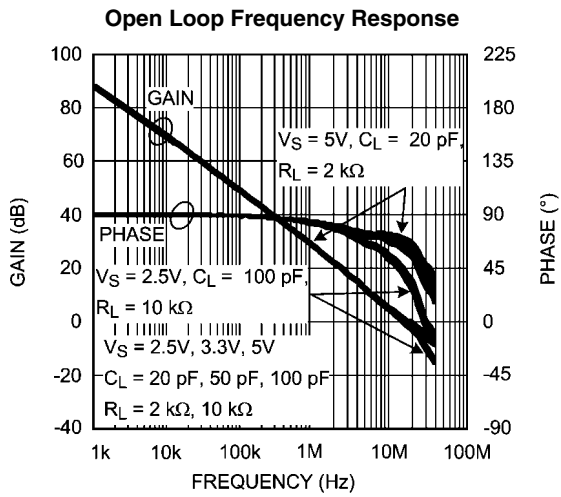
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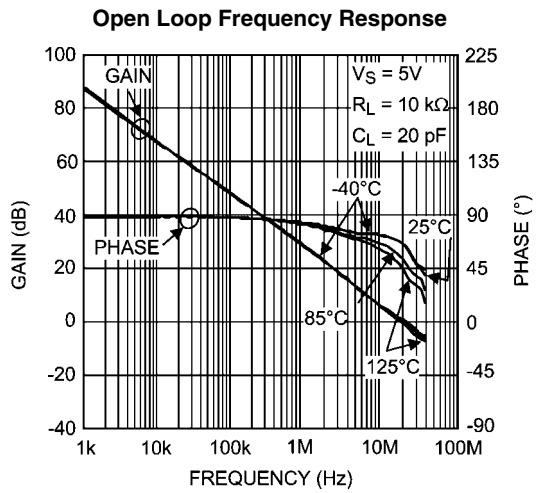
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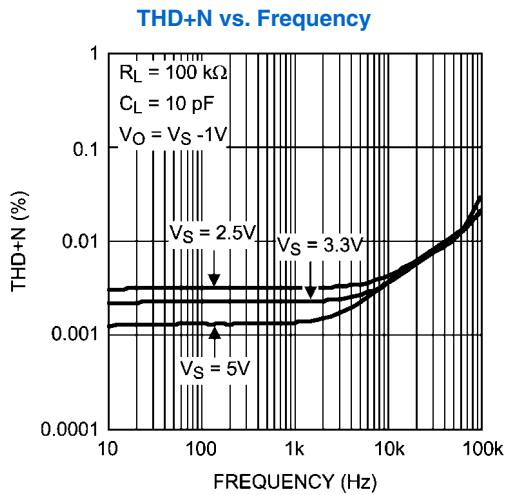
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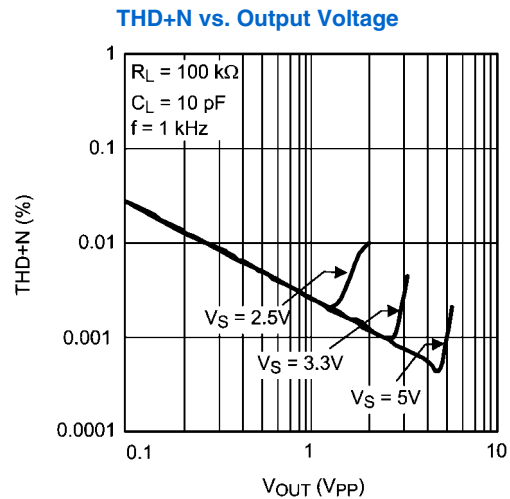
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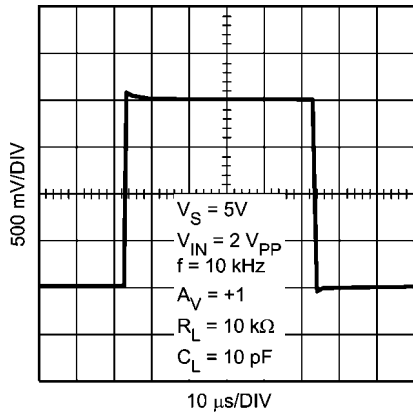


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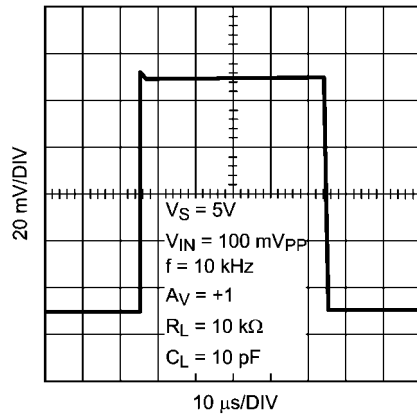
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Large Signal Step Response



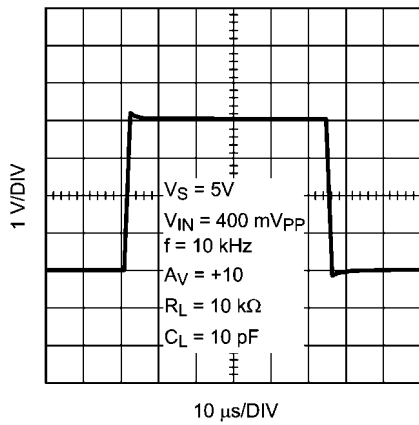
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Small Signal Step Response



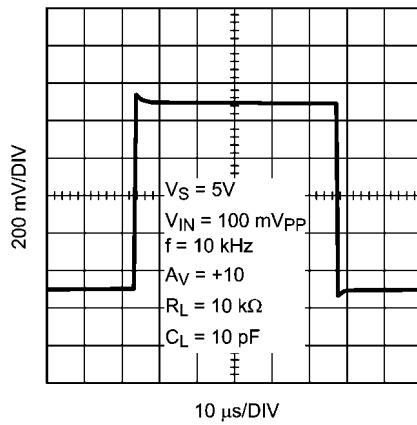
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Large Signal Step Response



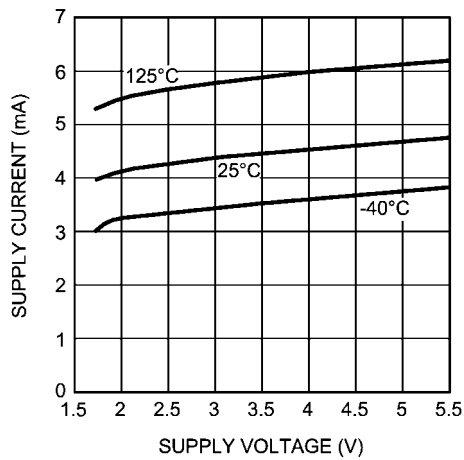
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Small Signal Step Response



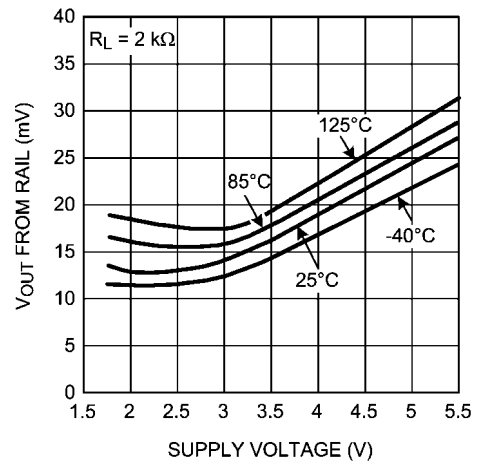
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Supply Current vs. Supply Voltage



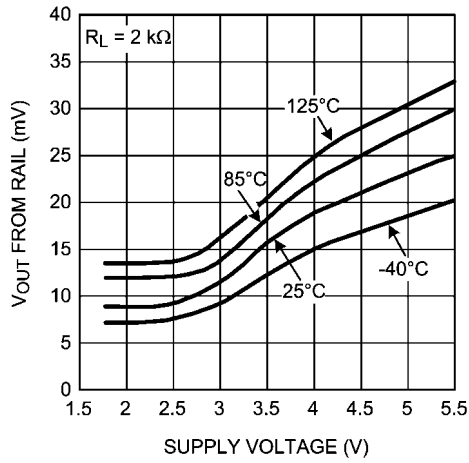
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Output Swing High vs. Supply Voltage



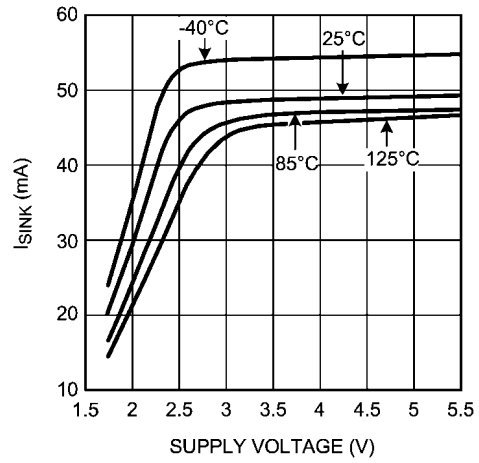
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Output Swing Low vs. Supply Voltage



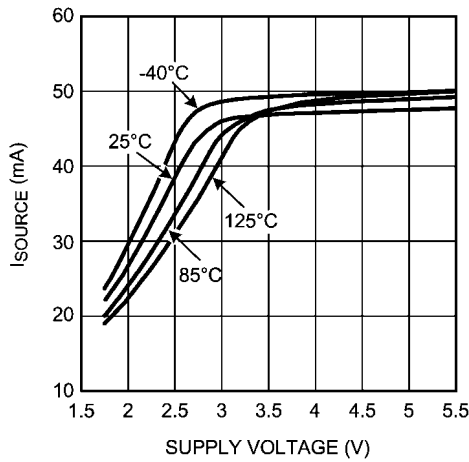
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Sinking Current vs. Supply Voltage



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Sourcing Current vs. Supply Voltage



30015061

Application Notes

LMP7732

The LMP7732 is a dual low noise, rail-to-rail input and output, low voltage amplifier.

The low input voltage noise of only $2.9 \text{ nV}/\sqrt{\text{Hz}}$ with a $1/f$ corner at 3 Hz makes the LMP7732 ideal for sensor applications where DC accuracy is of importance.

The LMP7732 has high gain bandwidth of 22 MHz. This wide bandwidth enables the use of the amplifier at higher gain settings while retaining ample usable bandwidth for the application. This is particularly beneficial when system designers need to use sensors with very limited output voltage range as it allows larger gains in one stage which in turn increases signal to noise ratio.

The LMP7732 has a proprietary input bias cancellation circuitry on the input stages. This allows the LMP7732 to have only about 1.5 nA bias current with a bipolar input stage. This low input bias current, paired with the inherent lower input voltage noise of bipolar input stages makes the LMP7732 an excellent choice for precision applications. The combination of low input bias current, low input offset voltage, and low input voltage noise enables the user to achieve unprecedented accuracy and higher signal integrity.

National Semiconductor is heavily committed to precision amplifiers and the market segment they serve. Technical support and extensive characterization data is available for sensitive applications or applications with a constrained error budget.

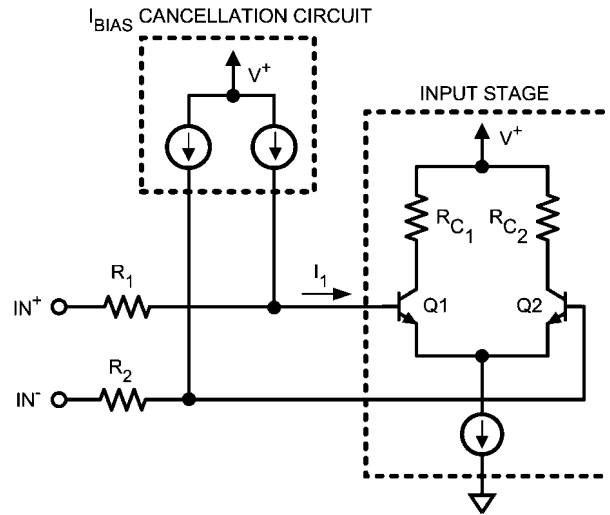
The LMP7732 comes in the 8-Pin SOIC and MSOP packages. These small packages are ideal solutions for area constrained PC boards and portable electronics.

INPUT BIAS CURRENT CANCELLATION

The LMP7732 has proprietary input bias current cancellation circuitry on its input stage.

The LMP7732 has rail-to-rail input. This is achieved by having a p-input and n-input stage in parallel. *Figure 1* only shows one of the input stages as the circuitry is symmetrical for both stages.

Figure 1 shows that as the common mode voltage gets closer to one of the extreme ends, current I_1 significantly increases. This increased current shows as an increase in voltage drop across resistor R_1 equal to $I_1 * R_1$ on IN^+ of the amplifier. This voltage contributes to the offset voltage of the amplifier. When common mode voltage is in the mid-range, the transistors are operating in the linear region and I_1 is significantly small. The voltage drop due to I_1 across R_1 can be ignored as it is orders of magnitude smaller than the amplifier's input offset voltage. As the common mode voltage gets closer to one of the rails, the offset voltage generated due to I_1 increases and becomes comparable to the amplifiers offset voltage.

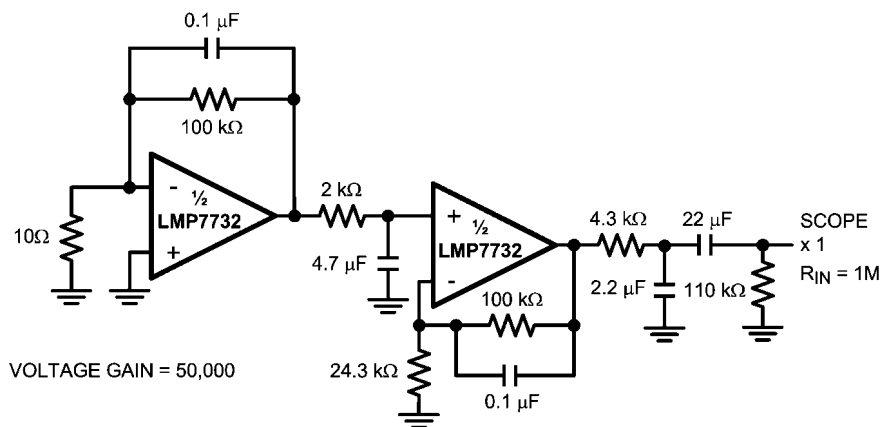


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FIGURE 1. Input Bias Current Cancellation

INPUT VOLTAGE NOISE MEASUREMENT

The LMP7732 has very low input voltage noise. The peak-to-peak input voltage noise of the LMP7732 can be measured using the test circuit shown in *Figure 2*.



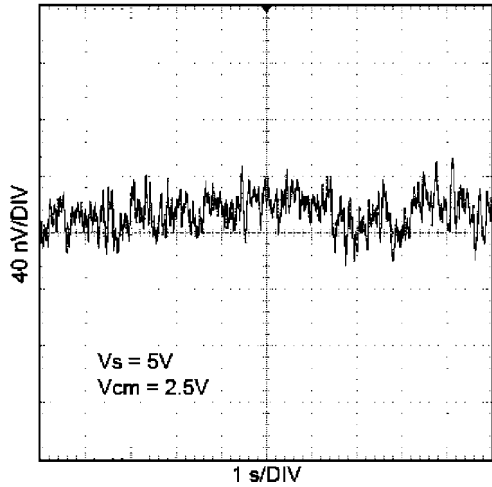
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FIGURE 2. 0.1 Hz to 10 Hz Noise Test Circuit

The frequency response of this noise test circuit at the 0.1 Hz corner is defined by only one zero. The test time for the 0.1 Hz to 10 Hz noise measurement using this configuration should not exceed 10 seconds, as this time limit acts as an

additional zero to reduce or eliminate the contributions of noise from frequencies below 0.1 Hz.

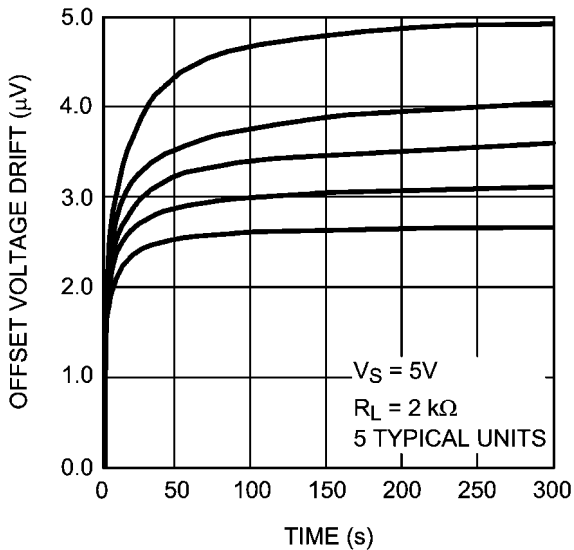
Figure 3 shows typical peak-to-peak noise for the LMP7732 measured with the circuit in *Figure 2*.



30015066

FIGURE 3. 0.1 Hz to 10 Hz Input Voltage Noise

Measuring the very low peak-to-peak noise performance of the LMP7732, requires special testing attention. In order to achieve accurate results, the device should be warmed up for at least five minutes. This is so that the input offset voltage of the op amp settles to a value. During this warm up period, the offset can typically change by a few μV because the chip temperature increases by about 30°C . If the 10 seconds of the measurement is selected to include this warm up time, some of this temperature change might show up as the measured noise. Figure 4 shows the start-up drift of five typical LMP7732 units.



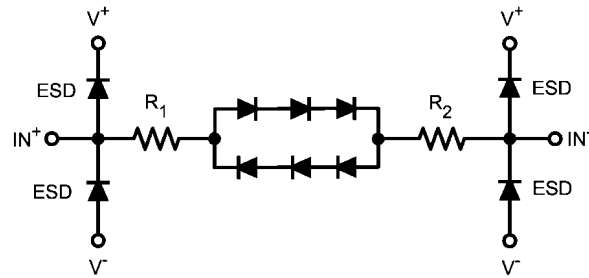
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FIGURE 4. Start-Up Input Offset Voltage Drift

During the peak-to-peak noise measurement, the LMP7732 must be shielded. This prevents offset variations due to airflow. Offset can vary by a few nV due to this airflow and that can invalidate measurements of input voltage noise with a magnitude which is in the same range. For similar reasons, sudden motions must also be restricted in the vicinity of the test area. The feed-through which results from this motion could increase the observed noise value which in turn would invalidate the measurement.

DIODES BETWEEN THE INPUTS

The LMP7732 has a set of anti-parallel diodes between their input pins, as shown in Figure 5. These diodes are present to protect the input stage of the amplifiers. At the same time, they limit the amount of differential input voltage that is allowed on the input pins. A differential signal larger than the voltage needed to turn on the diodes might cause damage to the diodes. The differential voltage between the input pins should be limited to ± 3 diode drops or the input current needs to be limited to ± 20 mA.



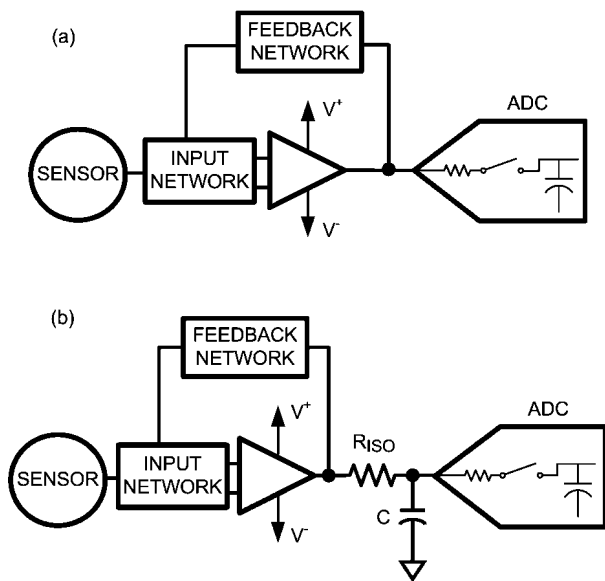
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FIGURE 5. Anti-Parallel Diodes between Inputs

DRIVING AN ADC

Analog to Digital Converters, ADCs, usually have a sampling capacitor on their input. When the ADC's input is directly connected to the output of the amplifier a charging current flows from the amplifier to the ADC. This charging current causes a momentary glitch that can take some time to settle. There are different ways to minimize this effect. One way is to slow down the sampling rate. This method gives the amplifier sufficient time to stabilize its output. Another way to minimize the glitch, caused by the switch capacitor, is to have an external capacitor connected to the input of the ADC. This capacitor is chosen so that its value is much larger than the internal switching capacitor and it will hence provide the charge needed to quickly and smoothly charge the ADC's sampling capacitor. Since this large capacitor will be loading the output of the amplifier as well, an isolation resistor is needed between the output of the amplifier and this capacitor. The isolation resistor, R_{ISO} , separates the additional load capacitance from the output of the amplifier and will also form a low-pass filter and can be designed to provide noise reduction as well as anti-aliasing. The draw back of having R_{ISO} is that it reduces signal swing since there is some voltage drop across it.

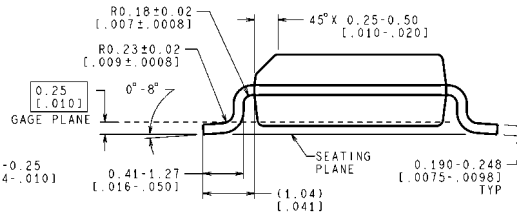
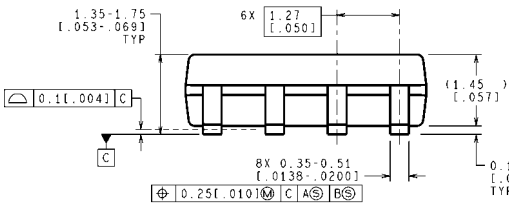
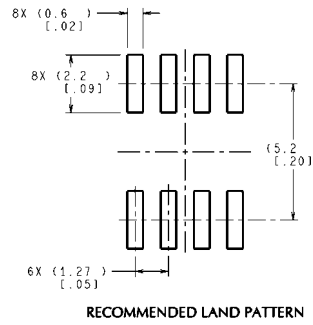
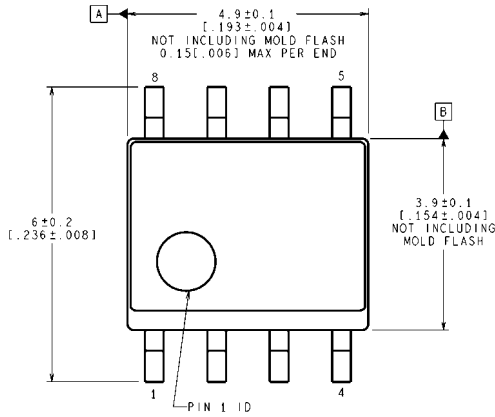
Figure 6 (a) shows the ADC directly connected to the amplifier. To minimize the glitch in this setting, a slower sample rate needs to be used. Figure 6 (b) shows R_{ISO} and an external capacitor used to minimize the glitch.



30015005

FIGURE 6. Driving An ADC

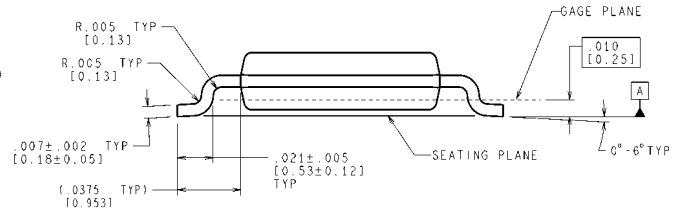
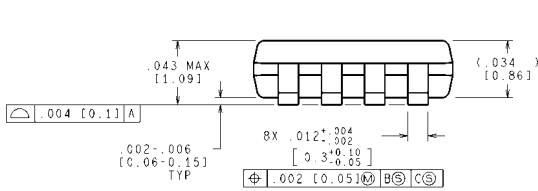
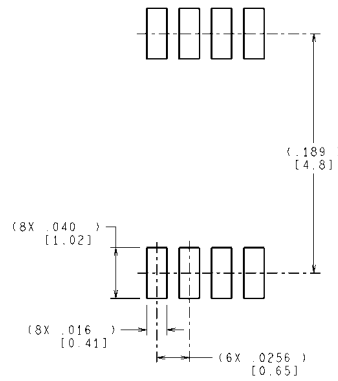
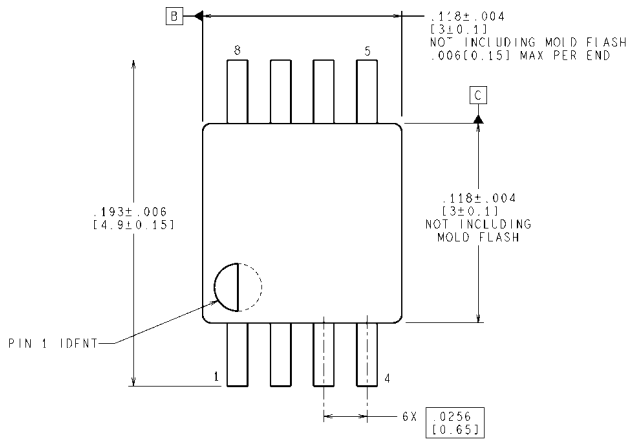
Physical Dimensions inches (millimeters) unless otherwise noted



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VALUES IN [] ARE INCHES
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M08A (Rev L)

**8-Pin SOIC
NS Package Number M08A**



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MUA08A (Rev F)

**8-Pin MSOP
NS Package Number MUA08A**

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