National Semiconductor

May 2005

LMH6703
1.2 GHz, Low Distortion Op Amp with Shutdown

General Description

The LMH™6703 is a very wideband, DC coupled monolithic operational amplifier designed specifically for ultra high resolution video systems as well as wide dynamic range systems requiring exceptional signal fidelity. Benefiting from National's current feedback architecture, the LMH6703 offers a practical gain range of ±1 to ±10 while providing stable operation without external compensation, even at unity gain. At a gain of +2 the LMH6703 supports ultra high resolution video systems with a 750 MHz 2 V_{PP} –3 dB Bandwidth. With 12-bit distortion levels through 10 MHz (R_L = 100Ω), and a 2.3nV/$\sqrt{Hz}$ input referred noise, the LMH6703 is the ideal driver or buffer for high speed flash A/D and D/A converters. Wide dynamic range systems such as radar and communication receivers requiring a wideband amplifier offering exceptional signal purity will find the LMH6703's low input referred noise and low harmonic distortion an attractive solution.

Features

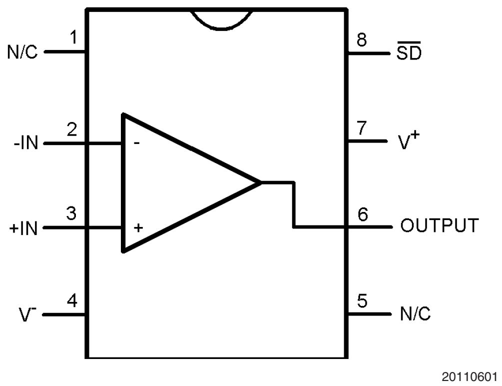
■ –3 dB bandwidth (V_{OUT} = 0.5 V_{PP}, A_V = +2)	1.2 GHz
■ $2^{nd}/3^{rd}$ harmonics (20 MHz, SOT23-6)	–69/–90 dBc
■ Low noise	2.3nV/$\sqrt{Hz}$
■ Fast slew rate	4500 V/μs
■ Supply current	11 mA
■ Output current	90 mA
■ Low differential gain and phase	0.01%/0.02°

Applications

- RGB video driver
- High resolution projectors
- Flash A/D driver
- D/A transimpedance buffer
- Wide dynamic range IF amp
- Radar/communication receivers
- DDS post-amps
- Line driver

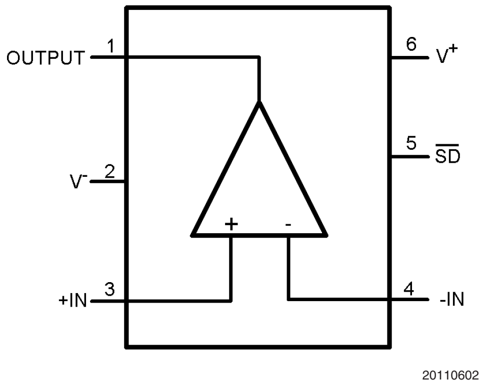
Connection Diagrams

8-pin SOIC



Top View

6-pin SOT23



Top View

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LMH6703MA	LMH6703MA	95 Units/Rail	M08A
	LMH6703MAX		2.5k Units Tape and Reel	
6-Pin SOT23	LMH6703MF	AR1A	1k Units Tape and Reel	MF06A
	LMH6703MFX		3k Units Tape and Reel	

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 5)	
Human Body Model	2000V
Machine Model	200V
V_S	±6.75V
I_{OUT}	(Note 3)
Common Mode Input Voltage	V^- to V^+
Maximum Junction Temperature	+150˚C
Storage Temperature Range	−65˚C to +150˚C
Soldering Information	
Infrared or Convection (20 sec.)	235˚C
Wave Soldering (10 sec.)	260˚C

Operating Ratings (Note 1)

Operating Temperature Range	−40˚C to +85˚C
Supply Voltage Range	±4V to ±6V
Package Thermal Resistance (θ_{JA}) (Note 4)	
6-Pin SOT23	208˚C/W
8-Pin SOIC	160˚C/W

Electrical Characteristics (Note 2)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, A_V = +2, V_S = ±5V, R_L = 100Ω, R_F = 560Ω, $\overline{SD}$ = Floating. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
Frequency Domain Performance						
SSBW	-3 dB Bandwidth	V_{OUT} = 0.5 V_{PP}, A_V = +1		1800		MHz
		V_{OUT} = 0.5 V_{PP}, A_V = +2		1200		
LSBW		V_{OUT} = 2 V_{PP}		750		
		V_{OUT} = 4 V_{PP}		500		
GF	0.1 dB Gain Flatness	V_{OUT} = 0.5 V_{PP}		150		MHz
		V_{OUT} = 2 V_{PP}		150		
DG	Differential Gain	R_L = 150Ω, 4.43 MHz		0.01		%
DP	Differential Phase	R_L = 150Ω, 4.43 MHz		0.02		deg
Time Domain Response						
t_r	Rise Time	2V Step, 10% to 90%		0.5		ns
		6V Step, 10% to 90%		1.05		ns
t_f	Fall Time	2V Step, 10% to 90%		0.5		ns
		6V Step, 10% to 90%		1.05		ns
SR	Slew Rate	4V Step, 10% to 90% (Note 6)		4200		V/μs
		6V Step, 10% to 90% (Note 6)		4500		V/μs
t_s	Settling Time	2V Step, V_{OUT} within 0.1%		10		ns
Distortion And Noise Response						
HD2	2nd Harmonic Distortion	2 V_{PP}, 5 MHz, SOT23-6		−87		dBc
		2 V_{PP}, 20 MHz, SOT23-6		−69		
		2 V_{PP}, 50 MHz, SOT23-6		−60		
HD3	3rd Harmonic Distortion	2 V_{PP}, 5 MHz, SOT23-6		−100		dBc
		2 V_{PP}, 20 MHz, SOT23-6		−90		
		2 V_{PP}, 50 MHz, SOT23-6		−70		
IMD	3rd Order Intermodulation Products	50 MHz, P_O = 5 dBm/ tone		−80		dBc
e_n	Input Referred Voltage Noise	>1 MHz		2.3		nV/ $\sqrt{Hz}$
i_n	Input Referred Noise Current	Inverting Pin >1 MHz		18.5		pA/ $\sqrt{Hz}$
	Input Referred Noise Current	Non-Inverting Pin >1 MHz		3		pA/ $\sqrt{Hz}$
Static, DC Performance						
V_{OS}	Input Offset Voltage			±1.5	±7 **±9**	mV

Electrical Characteristics (Note 2) (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ C$, $A_V = +2$, $V_S = \pm 5V$, $R_L = 100\Omega$, $R_F = 560\Omega$, $\overline{SD}$ = Floating. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
TCV_{OS}	Input Offset Voltage Average Drift	(Note 10)		22		μV/°C
I_B	Input Bias Current	Non-Inverting (Note 9)		−7	±20 **±23**	μA
		Inverting (Note 9)		−2	±35 **±44**	
TCI_B	Input Bias Current Average Drift	Non-Inverting (Note 10)		+30		nA/°C
		Inverting (Note 10)		−70		
V_O	Output Voltage Range	$R_L = \infty$	**±3.3**	±3.45		V
		$R_L = 100\Omega$	±3.2 **±3.14**	±3.4		
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.0V$ to $\pm 6.0V$	48 **46**	52		dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = -1.0V$ to $+1.0V$	45 **44**	47		dB
I_S	Supply Current (Enabled)	$\overline{SD} = 2V$, $R_L = \infty$		11	12.5 **15.0**	mA
	Supply Current (Disabled)	$\overline{SD} = 0.8V$, $R_L = \infty$		0.2	0.900 **0.935**	mA
Miscellaneous Performance						
R_{IN+}	Non-Inverting Input Resistance			1		MΩ
R_{IN-}	Inverting Input Resistance	Output Impedance of Input Buffer		30		Ω
C_{IN}	Non-Inverting Input Capacitance			0.8		pF
R_O	Output Resistance	Closed Loop		0.05		Ω
CMVR	Input Common Mode Voltage Range	CMRR ≥ 40 dB	±1.9			V
I_O	Linear Output Current	$V_{IN} = 0V$, $V_{OUT} \leq \pm 80$ mV	±55	±90		mA
Enable/Disable Performance (Disabled Low)						
T_{ON}	Enable Time			10		ns
T_{OFF}	Disable Time			10		ns
	Output Glitch			50		mV_{PP}
V_{IH}	Enable Voltage	$\overline{SD} \geq V_{IH}$	2.0			V
V_{IL}	Disable Voltage	$\overline{SD} \leq V_{IL}$			0.8	V
I_{IH}	Disable Pin Bias Current, High	$\overline{SD} = V^+$ (Note 9)		−7	±70	μA
I_{IL}	Disable Pin Bias Current, Low	$\overline{SD} = 0V$ (Note 9)	−50	−240	−400	μA
I_{OZ}	Disabled Output Leakage Current	$V_{OUT} = \pm 1.8V$		0.07	±25 **±40**	μA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

Note 3: The maximum output current (I_{OUT}) is determined by device power dissipation limitations.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for package soldered directly into a 2 layer PC board with zero air flow.

Note 5: Human body model: 1.5 kΩ in series with 100 pF. Machine model: 0Ω in series with 200 pF.

Note 6: Slew Rate is the average of the rising and falling edges.

Note 7: Typical numbers are the most likely parametric norm.

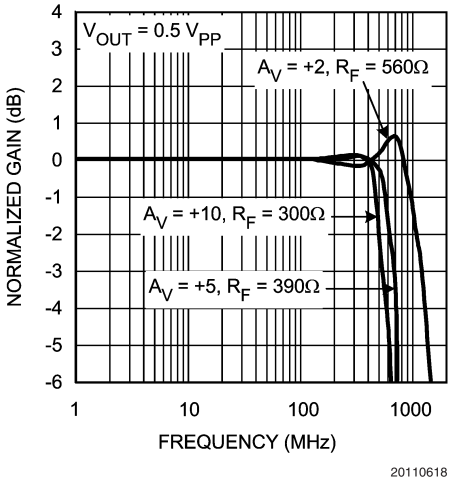
Note 8: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

Note 9: Negative input current implies current flowing out of the device.

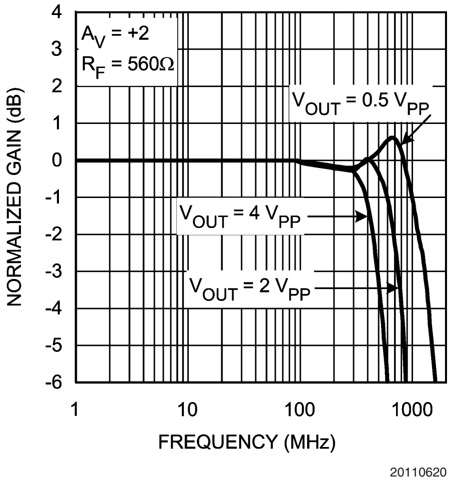
Note 10: Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

Typical Performance Characteristics (A_V = +2, R_L = 100Ω, V_S = ±5V, R_F = 560Ω, T_A = +25˚C, SOT23-6; unless otherwise specified).

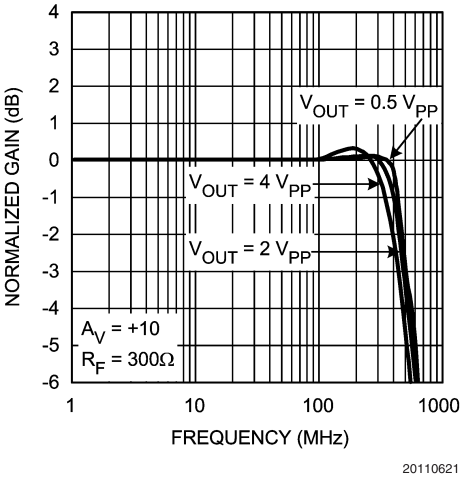
Small Signal Non-Inverting Frequency Response (SOT23)



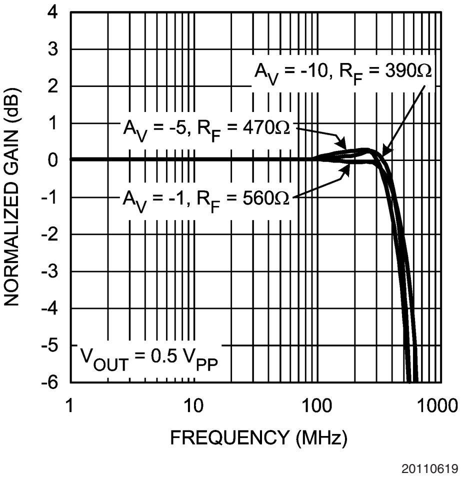
Large Signal Frequency Response (SOT23)



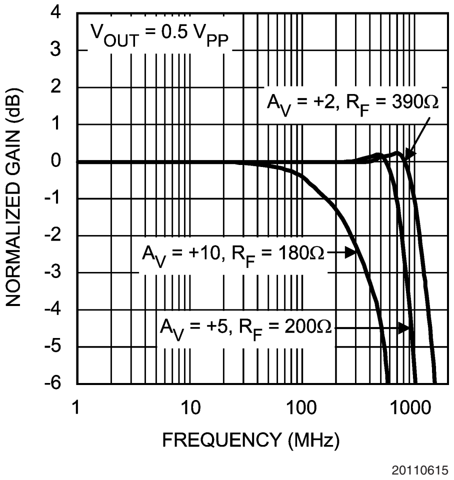
Large Signal Frequency Response (SOT23)



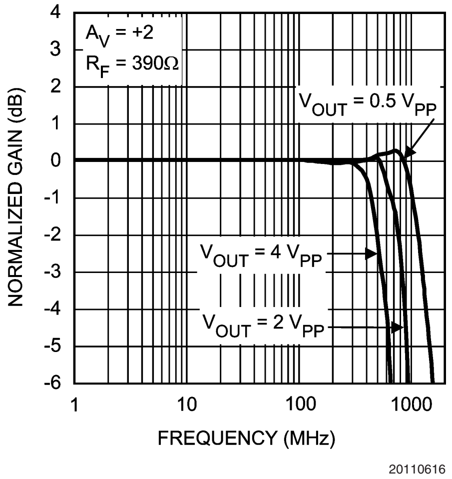
Small Signal Inverting Frequency Response (SOT23)



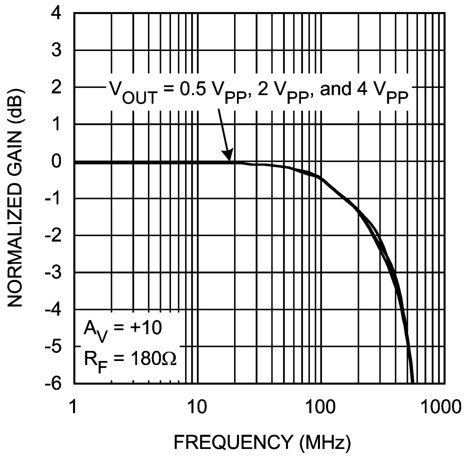
Small Signal Non-Inverting Frequency Response (SOIC)



Large Signal Frequency Response (SOIC)



Typical Performance Characteristics (A_V = +2, R_L = 100Ω, V_S = ±5V, R_F = 560Ω, T_A = +25˚C, SOT23-6; unless otherwise specified). (Continued)



Large Signal Frequency Response (SOIC)

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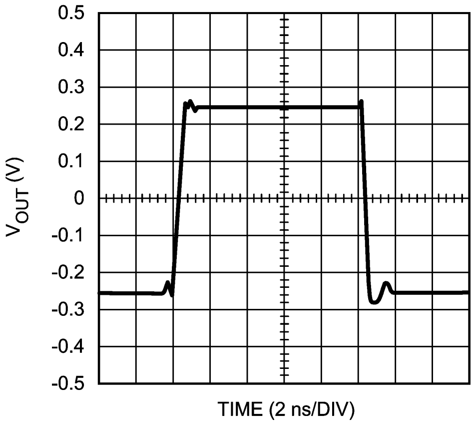

Small Signal Pulse Response

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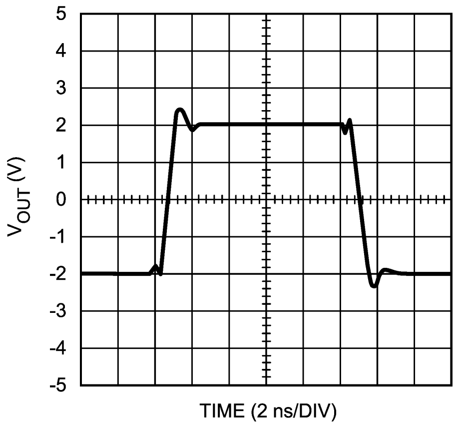

Large Signal Pulse Response

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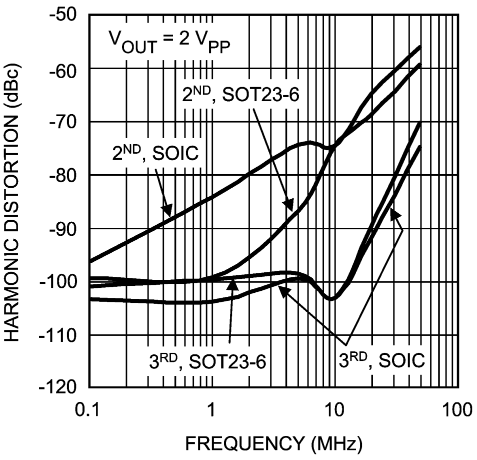

Harmonic Distortion vs. Frequency

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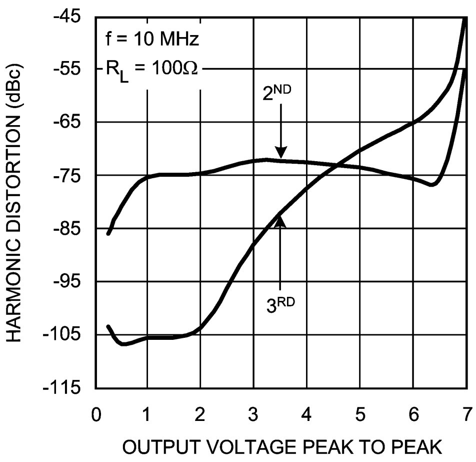

Harmonic Distortion vs. Output Voltage

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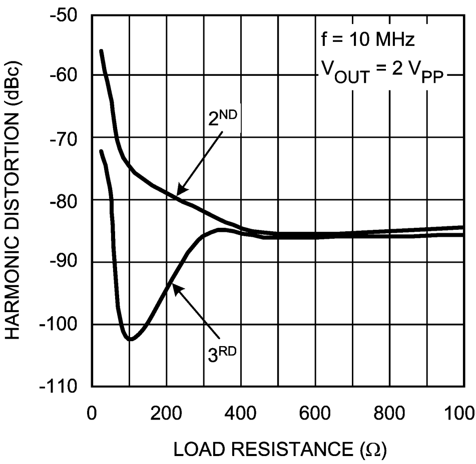
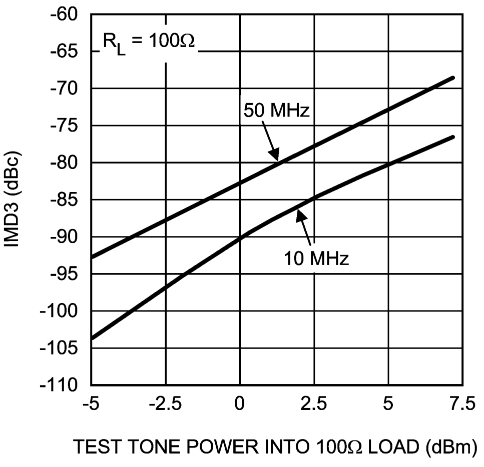


Harmonic Distortion vs. Load

20110625

Typical Performance Characteristics (A_V = +2, R_L = 100Ω, V_S = ±5V, R_F = 560Ω, T_A = +25˚C, SOT23-6; unless otherwise specified). (Continued)

2-Tone 3rd Order Intermodulation



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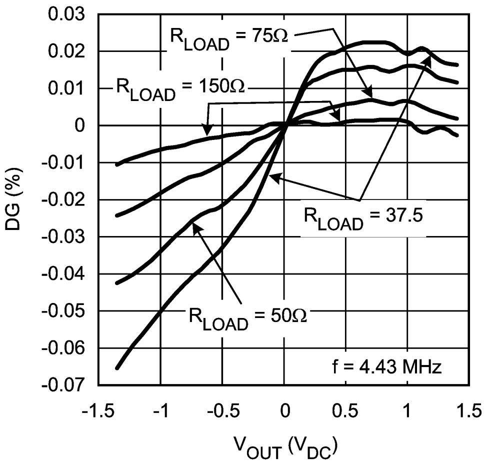
Differential Gain



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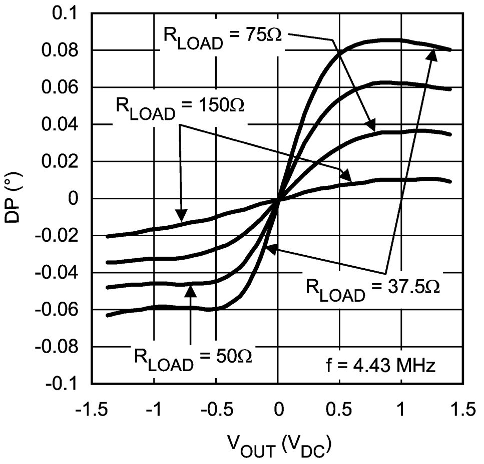
Differential Phase



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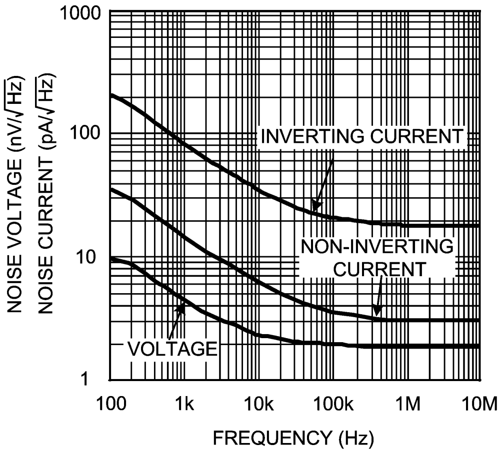
Noise



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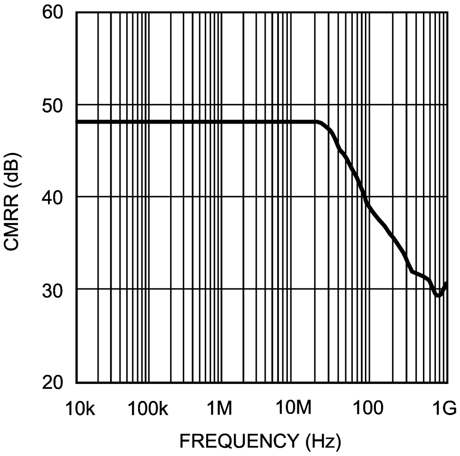
CMRR vs. Frequency



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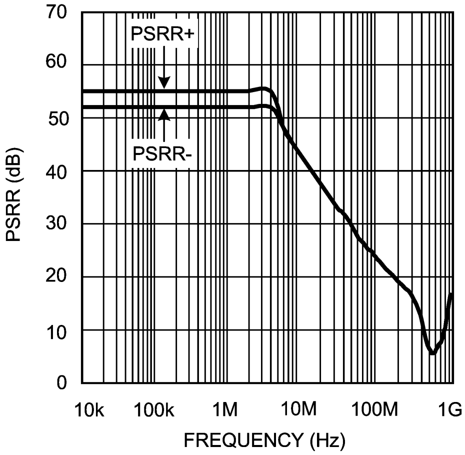
PSRR vs. Frequency



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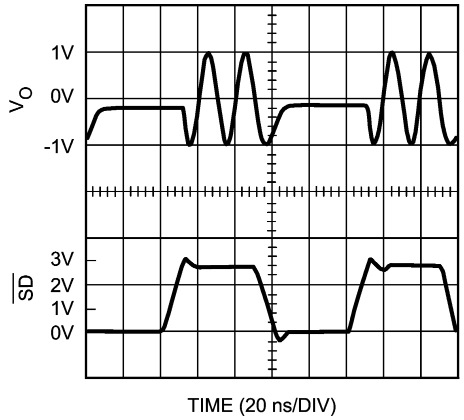
Typical Performance Characteristics (A_V = +2, R_L = 100Ω, V_S = ±5V, R_F = 560Ω, T_A = +25˚C, SOT23-6; unless otherwise specified). (Continued)

Disable Timing



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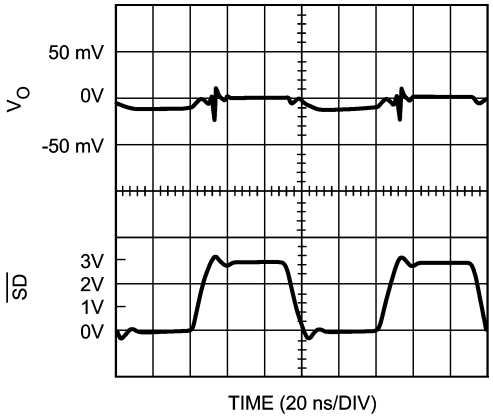
Disable Output Glitch



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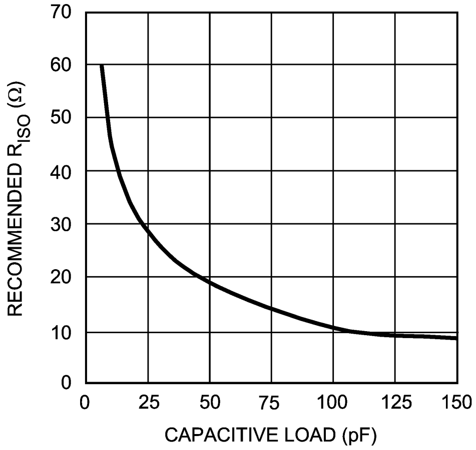
R_{ISO} vs. C_{LOAD} (See Applications Section)



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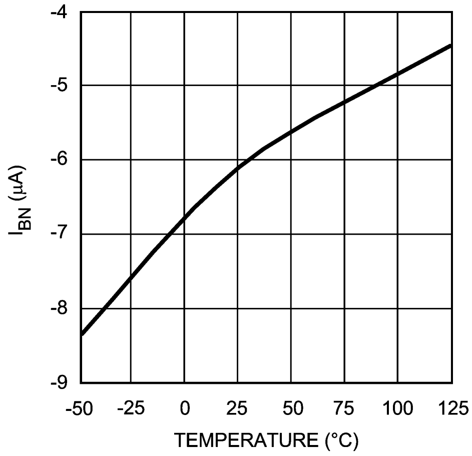
Non-Inverting Input Bias vs. Temperature



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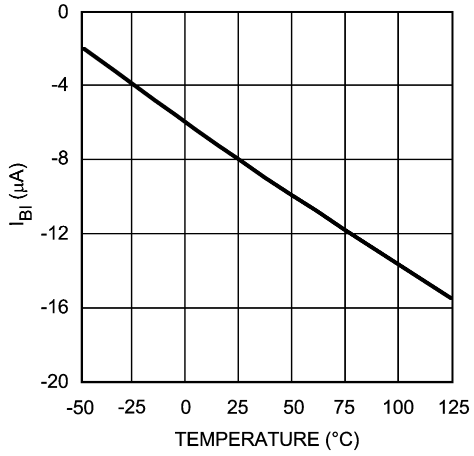
Inverting Input Bias vs. Temperature



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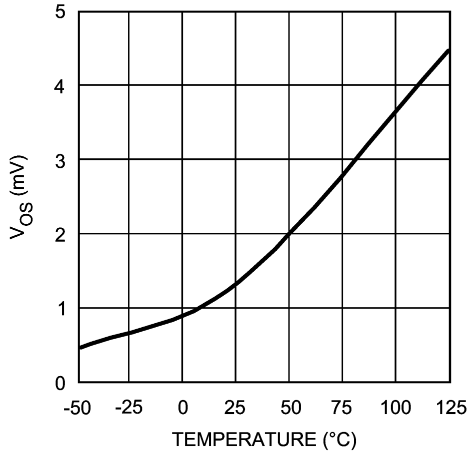
Input Offset vs. Temperature



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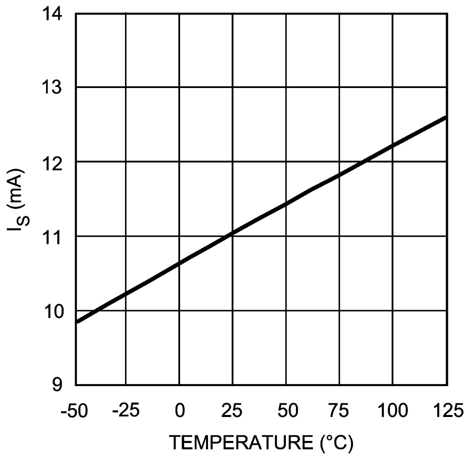
Typical Performance Characteristics (A_V = +2, R_L = 100Ω, V_S = ±5V, R_F = 560Ω, T_A = +25˚C, SOT23-6; unless otherwise specified). (Continued)

Supply Current vs. Temperature



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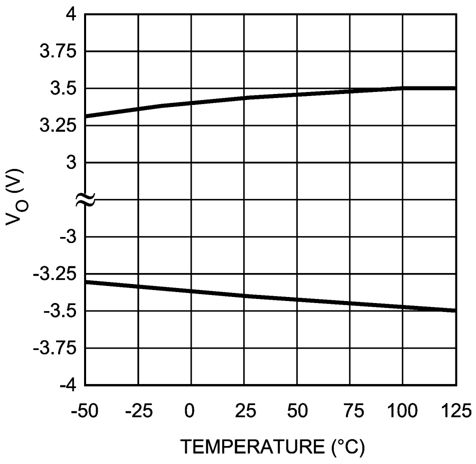
Voltage Swing vs. Temperature



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Application Section

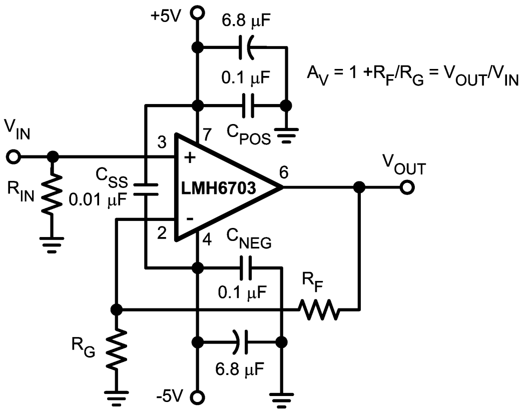


FIGURE 1. Recommended Non-Inverting Gain Circuit (SOIC Pinout Shown)

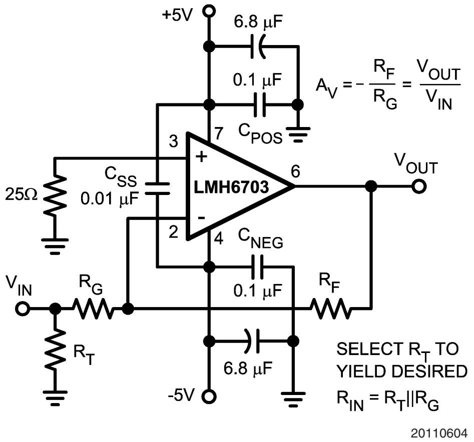


FIGURE 2. Recommended Inverting Gain Circuit (SOIC Pinout Shown)

GENERAL DESCRIPTION

The LMH6703 is a high speed current feedback amplifier, optimized for excellent bandwidth, gain flatness, and low distortion. The loop gain for a current feedback op amp, and hence the frequency response, is predominantly set by the feedback resistor value. The LMH6703 in the SOT23-6 package is optimized for use with a 560Ω feedback resistor. The LMH6703 in the SOIC package is optimized for use with a 390Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 discusses this in detail along with the occasions where a different R_F might be advantageous.

EVALUATION BOARDS

Device	Package	Evaluation Board Part Number
LMH6703MF	SOT23-6	CLC730216
LMH6703MA	SOIC	CLC730227

An Evaluation Board is shipped upon request when a sample order is placed with National Semiconductor.

FEEDBACK RESISTOR SELECTION

One of the key benefits of a current feedback operational amplifier is the ability to maintain optimum frequency response independent of gain by using appropriate values for the feedback resistor (R_F). The Electrical Characteristics and Typical Performance plots specify an R_F of 560Ω (390Ω for the SOIC package), a gain of +2 V/V and ±5V power supplies (unless otherwise specified). Generally, lowering R_F from it's recommended value will peak the frequency response and extend the bandwidth while increasing the value of R_F will cause the frequency response to roll off faster. Reducing the value of R_F too far below it's recommended value will cause overshoot, ringing and, eventually, oscillation.

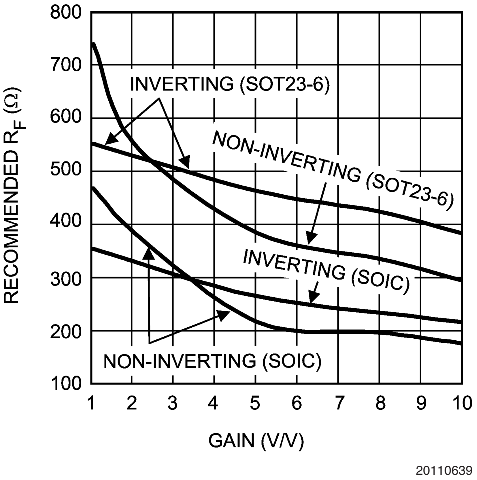


FIGURE 3. Recommended R_F vs. Gain

Since a current feedback amplifier is dependant on the value of R_F to provide frequency compensation and since the value of R_F can be used to optimize the frequency response, different packages use different R_F values. As shown in *Figure 3*, Recommended R_F vs. Gain, the SOT23-6 and the SOIC package use different values for the feedback resistor, R_F. Since each application is slightly different, it is worth some experimentation to find the optimal R_F for a given circuit. In general, a value of R_F that produces ≈0.1 dB of peaking is the best compromise between stability and maximum bandwidth. Note that it is not possible to use a current feedback amplifier with the output shorted directly to the inverting input. The buffer configuration of the LMH6703 requires a 560Ω (390Ω for SOIC package) feedback resistor for stable operation.

The LMH6703 was optimized for high speed operation. As shown in *Figure 3*, the suggested value for R_F decreases for higher gains. Due to the output impedance of the input buffer, there is a practical limit for how small R_F can go, based on the lowest practical value of R_G. This limitation applies to both inverting and non inverting configurations. For the LMH6703 the input resistance of the inverting input is approximately 30Ω and 20Ω is a practical (but not hard and fast) lower limit for R_G. The LMH6703 begins to operate in a gain bandwidth limited fashion in the region when R_G is nearly equal to the input buffer impedance. Note that the

Application Section (Continued)

amplifier will operate with R_G values well below 20Ω, however results may be substantially different than predicted from ideal models. In particular the voltage potential between the Inverting and Non-Inverting inputs cannot be expected to remain small.

Inverting gain applications that require impedance matched inputs may limit gain flexibility somewhat (especially if maximum bandwidth is required). The impedance seen by the source is $R_G \parallel R_T$ (R_T is optional). The value of R_G is R_F /Gain. Thus for a SOT23 in a gain of —5V/V, an R_F of 460Ω is optimum and R_G is 92Ω. Without a termination resistor, R_T, the input impedance would equal R_G, 92Ω. Using an R_T of 109Ω will set the input resistance to match a 50Ω source. Note that source impedances greater then R_G cannot be matched in the inverting configuration.

For more information see Application Note OA-13 which describes the relationship between R_F and closed-loop frequency response for current feedback operational amplifiers. The value for the inverting input impedance for the LMH6703 is approximately 30Ω. The LMH6703 is designed for optimum performance at gains of +1 to +10 V/V and −1 to −9 V/V. Higher gain configurations are still useful, however, the bandwidth will fall as gain is increased, much like a typical voltage feedback amplifier.

The LMH6703 data sheet shows both SOT23-6 and SOIC data in the Electrical Characteristic section to aid in selecting the right package. The Typical Performance Characteristics section shows SOT23-6 package plots only.

CAPACITIVE LOAD DRIVE

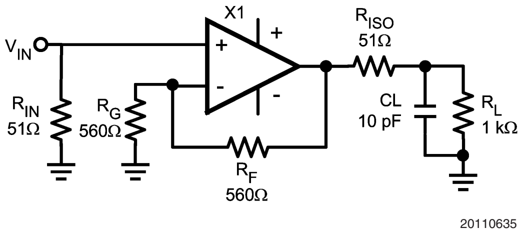


FIGURE 4. Decoupling Capacitive Loads

Capacitive output loading applications will benefit from the use of a series output resistor R_{ISO}. *Figure 4* shows the use of a series output resistor, R_{ISO}, to stabilize the amplifier output under capacitive loading. Capacitive loads from 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. The chart “Suggested R_{ISO} vs. Cap Load” gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for 0.5 dB or less of peaking in the frequency response. This produces a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{ISO} can be reduced slightly from the recommended values.

DC ACCURACY AND NOISE

Example below shows the output offset computation equation for the non-inverting configuration (see *Figure 1*) using the typical bias current and offset specifications for $A_V = +2$:

Output Offset : $V_O = (I_{BN} \cdot R_{IN} \pm V_{OS})\ (1 + R_F/R_G) \pm I_{BI} \cdot R_F$

Where R_{IN} is the equivalent input impedance on the non-inverting input.

Example computation for $A_V = +2$, $R_F = 560\Omega$, $R_{IN} = 25\Omega$:

$V_O = (7\ \mu A \cdot 25\Omega \pm 1.5\ mV)\ (1 + 560/560) \pm 2\mu A \cdot 560 \approx -3.7\ mV$ to $4.5\ mV$

A good design, however, should include a worst case calculation using Min/Max numbers in the data sheet tables, in order to ensure "worst case" operation.

Further improvement in the output offset voltage and drift is possible using the composite amplifiers described in Application Note OA-7. The two input bias currents are physically unrelated in both magnitude and polarity for the current feedback topology. It is not possible, therefore, to cancel their effects by matching the source impedance for the two inputs (as is commonly done for matched input bias current devices).

The total output noise is computed in a similar fashion to the output offset voltage. Using the input noise voltage and the two input noise currents, the output noise is developed through the same gain equations for each term but combined as the square root of the sum of squared contributing elements. See Application Note OA-12 for a full discussion of noise calculations for current feedback amplifiers.

PRINTED CIRCUIT LAYOUT

Whenever questions about layout arise, use the evaluation board as a guide. The CLC730216 is the evaluation board supplied with SOT23-6 samples of the LMH6703 and the CLC730227 is the evaluation board supplied with SOIC samples of the LMH6703.

To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. Components in the feedback path should be placed as close to the device as possible to minimize parasitic capacitance. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends.

Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each voltage rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located further from the device, the smaller ceramic bypass capacitors should be placed as close to the device as possible. In *Figure 1* and *Figure 2* C_{SS} is optional, but is recommended for best second order harmonic distortion.

Application Section (Continued)

VIDEO PERFORMANCE

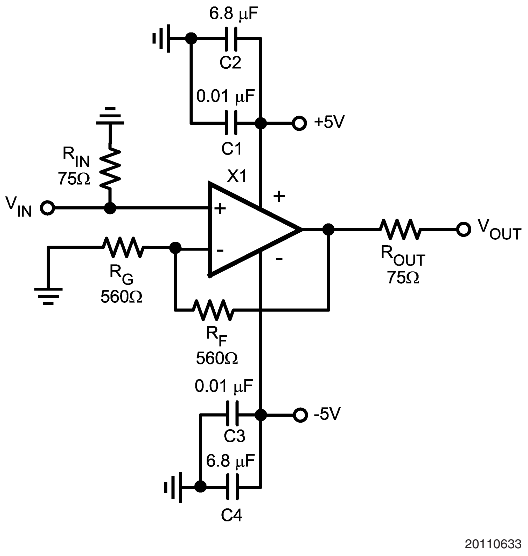
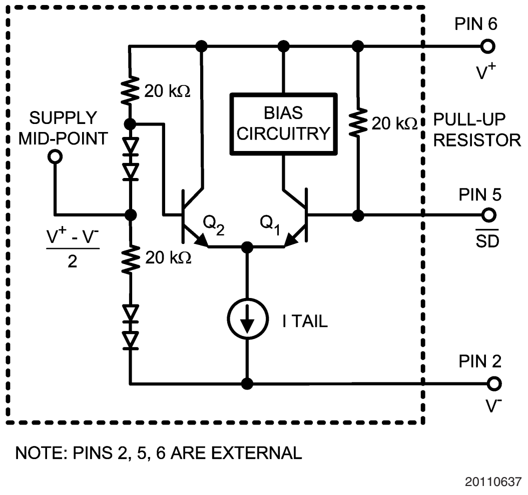


FIGURE 5. Typical Video Application

The LMH6703 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. NTSC and PAL performance is nearly flawless with DG of 0.01% and DP of 0.02°. Best performance will be obtained with back terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitance from the amplifier output stage. *Figure 5* shows a typical configuration for driving 75Ω cable. The amplifier is configured for a gain of two compensating for the 6 dB loss due to R_{OUT}.

ENABLE/DISABLE



NOTE: PINS 2, 5, 6 ARE EXTERNAL

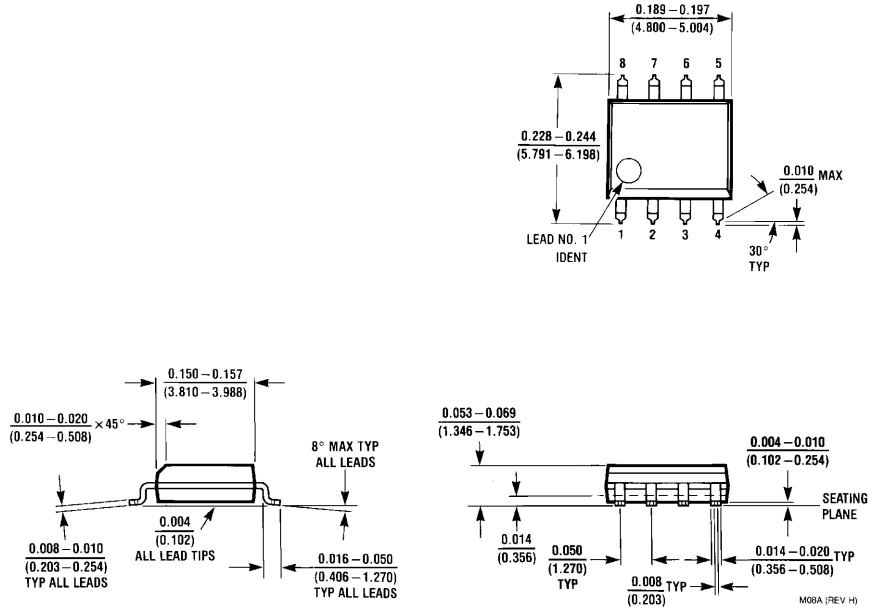
FIGURE 6. $\overline{SD}$ Pin Simplified Schematic (SOT23 Pinout Shown)

For ±5V supplies only the LMH6703 has a TTL logic compatible disable function. Apply a logic low (<.8V) to the $\overline{SD}$ pin and the LMH6703 is disabled. Apply a logic high (>2.0V), or let the pin float and the LMH6703 is enabled. Voltage, not current, at the Shutdown pin ($\overline{SD}$) determines the enable/disable state. Care must be exercised to prevent the shutdown pin voltage from going more than 0.8V below the midpoint of the supply voltages (0V with split supplies, $V^+/2$ with single supply biasing). Doing so could cause transistor Q1 to Zener resulting in damage to the disable circuit (See *Figure 6*). The core amplifier is unaffected by this, but the shutdown operation could become permanently slower as a result.

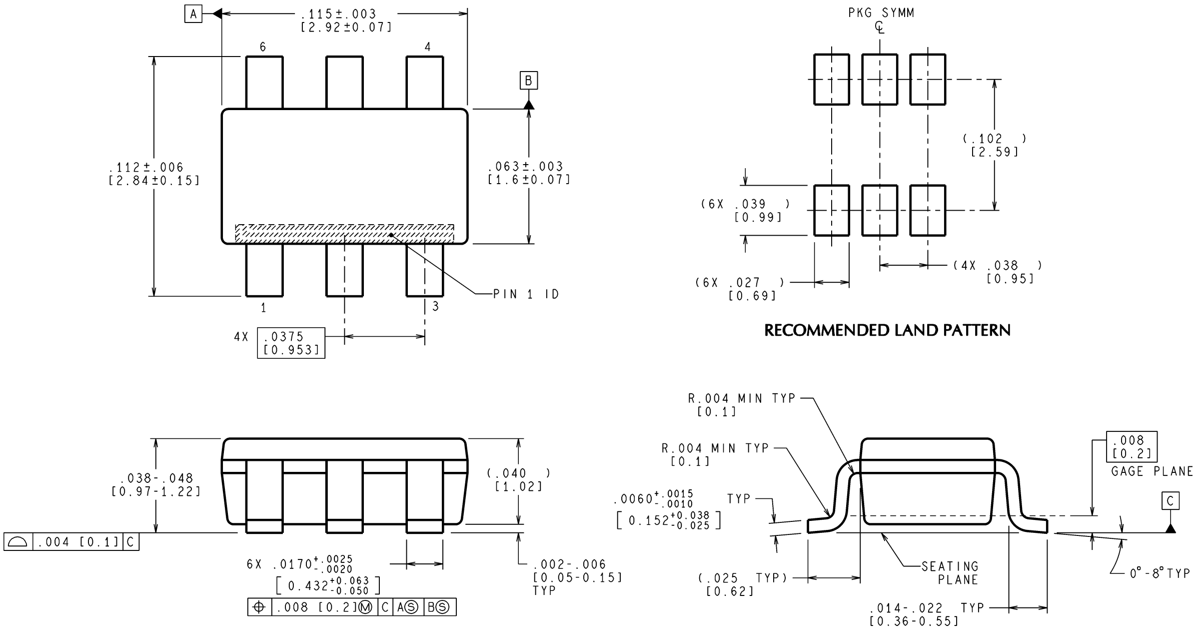
Disabled, the LMH6703 inputs and output become high impedances. While disabled the LMH6703 quiescent current is approximately 200 µA. Because of the pull up resistor on the shutdown circuit, the I_{CC} and I_{EE} currents (positive and negative supply currents respectively) are not balanced in the disabled state. The positive supply current (I_{CC}) is approximately 300 µA while the negative supply current (I_{EE}) is only 200 µA. The remaining I_{EE} current of 100 µA flows through the shutdown pin.

The disable function can be used to create analog switches or multiplexers. Implement a single analog switch with one LMH6703 positioned between an input and output. Create an analog multiplexer with several LMH6703's and tie the outputs together.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MF06A (Rev B)

6-Pin SOT23
NS Package Number M06A

Notes

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