

# LMC6061

## Precision CMOS Single Micropower Operational Amplifier

### General Description

The LMC6061 is a precision single low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption, make the LMC6061 ideally suited for battery powered applications.

Other applications using the LMC6061 include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with National's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6081 precision single operational amplifier.

For a dual or quad operational amplifier with similar features, see the LMC6062 or LMC6064 respectively.

**PATENT PENDING**

### Features

(Typical Unless Otherwise Noted)

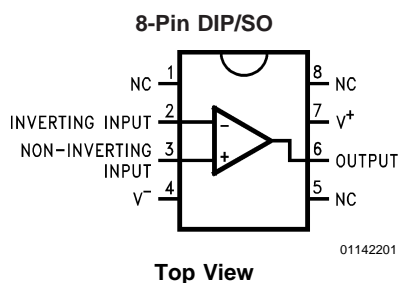
- Low offset voltage: 100  $\mu$ V

- Ultra low supply current: 20  $\mu$ A
- Operates from 4.5V to 15V single supply
- Ultra low input bias current: 10 fA
- Output swing within 10 mV of supply rail, 100k load
- Input common-mode range includes  $V^-$
- High voltage gain: 140 dB
- Improved latchup immunity

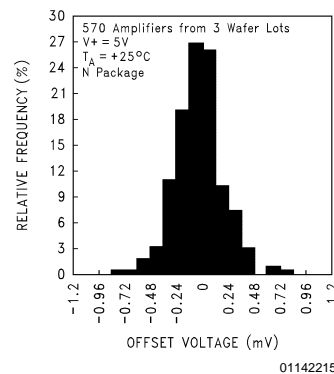
### Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Hand-held analytic instruments
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

### Connection Diagram



**Distribution of LMC6061  
Input Offset Voltage  
( $T_A = +25^\circ\text{C}$ )**



**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V <sup>+</sup> ) +0.3V, (V <sup>-</sup> ) -0.3V
Supply Voltage (V <sup>+</sup> – V <sup>-</sup> )	16V
Output Short Circuit to V <sup>+</sup>	(Note 10)
Output Short Circuit to V <sup>-</sup>	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	-65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA

Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

**Operating Ratings** (Note 1)

Temperature Range	
LMC6061AM	-55°C ≤ T <sub>J</sub> ≤ +125°C
LMC6061AI, LMC6082I	-40°C ≤ T <sub>J</sub> ≤ +85°C
Supply Voltage	4.5V ≤ V <sup>+</sup> ≤ 15.5V
Thermal Resistance (θ <sub>JA</sub> ) (Note 11)	
N Package, 8-Pin Molded DIP	115°C/W
M Package, 8-Pin Surface	
Mount	193°C/W
Power Dissipation	(Note 9)

**DC Electrical Characteristics**

Unless otherwise specified, all limits guaranteed for T<sub>J</sub> = 25°C. **Boldface** limits apply at the temperature extremes. V<sup>+</sup> = 5V, V<sup>-</sup> = 0V, V<sub>CM</sub> = 1.5V, V<sub>O</sub> = 2.5V and R<sub>L</sub> > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 9)	LMC6061AM Limit (Note 6)	LMC6061AI Limit (Note 6)	LMC6061I Limit (Note 6)	Units	
V <sub>OS</sub>	Input Offset Voltage		100	350 <b>1200</b>	350 <b>900</b>	800 <b>1300</b>	μV Max	
TCV <sub>OS</sub>	Input Offset Voltage Average Drift		1.0				μV/°C	
I <sub>B</sub>	Input Bias Current		0.010	<b>100</b>	<b>4</b>	<b>4</b>	pA Max	
I <sub>OS</sub>	Input Offset Current		0.005	<b>100</b>	<b>2</b>	<b>2</b>	pA Max	
R <sub>IN</sub>	Input Resistance		>10				Tera Ω	
CMRR	Common Mode Rejection Ratio	0V ≤ V <sub>CM</sub> ≤ 12.0V V <sup>+</sup> = 15V	85	75 <b>70</b>	75 <b>72</b>	66 <b>63</b>	dB Min	
+PSRR	Positive Power Supply Rejection Ratio	5V ≤ V <sup>+</sup> ≤ 15V V <sub>O</sub> = 2.5V	85	75 <b>70</b>	75 <b>72</b>	66 <b>63</b>	dB Min	
-PSRR	Negative Power Supply Rejection Ratio	0V ≤ V <sup>-</sup> ≤ -10V	100	84 <b>70</b>	84 <b>81</b>	74 <b>71</b>	dB Min	
V <sub>CM</sub>	Input Common-Mode Voltage Range	V <sup>+</sup> = 5V and 15V for CMRR ≥ 60 dB	-0.4	-0.1 <b>0</b>	-0.1 <b>0</b>	-0.1 <b>0</b>	V Max	
			V <sup>+</sup> – 1.9	V <sup>+</sup> – 2.3 <b>V<sup>+</sup> – 2.6</b>	V <sup>+</sup> – 2.3 <b>V<sup>+</sup> – 2.5</b>	V <sup>+</sup> – 2.3 <b>V<sup>+</sup> – 2.5</b>	V Min	
A <sub>V</sub>	Large Signal Voltage Gain	R <sub>L</sub> = 100 kΩ (Note 7)	Sourcing	4000	400 <b>200</b>	400 <b>300</b>	300 <b>200</b>	V/mV Min
			Sinking	3000	180 <b>70</b>	180 <b>100</b>	90 <b>60</b>	V/mV Min
		R <sub>L</sub> = 25 kΩ (Note 7)	Sourcing	3000	400 <b>150</b>	400 <b>150</b>	200 <b>80</b>	V/mV Min
			Sinking	2000	100 <b>35</b>	100 <b>50</b>	70 <b>35</b>	V/mV Min

**DC Electrical Characteristics** (Continued)

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ . **Boldface** limits apply at the temperature extremes.  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.5\text{V}$ ,  $V_O = 2.5\text{V}$  and  $R_L > 1\text{M}$  unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 9)	LMC6061AM Limit (Note 6)	LMC6061AI Limit (Note 6)	LMC6061I Limit (Note 6)	Units
$V_O$	Output Swing	$V^+ = 5\text{V}$ $R_L = 100\text{ k}\Omega$ to $2.5\text{V}$	4.995	4.990	4.990	4.950	V
				<b>4.970</b>	<b>4.980</b>	<b>4.925</b>	Min
			0.005	0.010	0.010	0.050	V
				<b>0.030</b>	<b>0.020</b>	<b>0.075</b>	Max
		$V^+ = 5\text{V}$ $R_L = 25\text{ k}\Omega$ to $2.5\text{V}$	4.990	4.975	4.975	4.950	V
				<b>4.955</b>	<b>4.965</b>	<b>4.850</b>	Min
			0.010	0.020	0.020	0.050	V
				<b>0.045</b>	<b>0.035</b>	<b>0.150</b>	Max
		$V^+ = 15\text{V}$ $R_L = 100\text{ k}\Omega$ to $7.5\text{V}$	14.990	14.975	14.975	14.950	V
				<b>14.955</b>	<b>14.965</b>	<b>14.925</b>	Min
		0.010	0.025	0.025	0.050	V	
			<b>0.050</b>	<b>0.035</b>	<b>0.075</b>	Max	
	$V^+ = 15\text{V}$ $R_L = 25\text{ k}\Omega$ to $7.5\text{V}$	14.965	14.900	14.900	14.850	V	
			<b>14.800</b>	<b>14.850</b>	<b>14.800</b>	Min	
		0.025	0.050	0.050	0.100	V	
			<b>0.200</b>	<b>0.150</b>	<b>0.200</b>	Max	
$I_O$	Output Current $V^+ = 5\text{V}$	Sourcing, $V_O = 0\text{V}$	22	16	16	13	mA
				<b>8</b>	<b>10</b>	<b>8</b>	Min
		Sinking, $V_O = 5\text{V}$	21	16	16	16	mA
				<b>7</b>	<b>8</b>	<b>8</b>	Min
$I_O$	Output Current $V^+ = 15\text{V}$	Sourcing, $V_O = 0\text{V}$	25	15	15	15	mA
				<b>9</b>	<b>10</b>	<b>10</b>	Min
		Sinking, $V_O = 13\text{V}$ (Note 10)	26	20	20	20	mA
				<b>7</b>	<b>8</b>	<b>8</b>	Min
$I_S$	Supply Current	$V^+ = +5\text{V}$ , $V_O = 1.5\text{V}$	20	24	24	32	$\mu\text{A}$
				<b>35</b>	<b>32</b>	<b>40</b>	Max
		$V^+ = +15\text{V}$ , $V_O = 7.5\text{V}$	24	30	30	40	$\mu\text{A}$
				<b>40</b>	<b>38</b>	<b>48</b>	Max

**AC Electrical Characteristics**

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ . **Boldface** limits apply at the temperature extremes.  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.5\text{V}$ ,  $V_O = 2.5\text{V}$  and  $R_L > 1\text{M}$  unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6061AM Limit (Note 6)	LMC6061AI Limit (Note 6)	LMC6061I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	35	20	20	15	V/ms
					<b>8</b>	<b>10</b>	<b>7</b>
GBW	Gain-Bandwidth Product		100				kHz
$\theta_m$	Phase Margin		50				Deg
$e_n$	Input-Referred Voltage Noise	$F = 1\text{ kHz}$	83				$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input-Referred Current Noise	$F = 1\text{ kHz}$	0.0002				$\text{pA}/\sqrt{\text{Hz}}$
T.H.D.	Total Harmonic Distortion	$F = 1\text{ kHz}$ , $A_V = -5$ $R_L = 100\text{ k}\Omega$ , $V_O = 2\text{ V}_{\text{PP}}$ $\pm 5\text{V}$ Supply	0.01				%

## AC Electrical Characteristics (Continued)

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

**Note 2:** Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of  $\pm 30$  mA over long term may adversely affect reliability.

**Note 3:** The maximum power dissipation is a function of  $T_{J(\text{Max})}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(\text{Max})} - T_A)/\theta_{JA}$ .

**Note 4:** Human body model, 1.5 k $\Omega$  in series with 100 pF.

**Note 5:** Typical values represent the most likely parametric norm.

**Note 6:** All limits are guaranteed by testing or statistical analysis.

**Note 7:**  $V^+ = 15V$ ,  $V_{CM} = 7.5V$  and  $R_L$  connected to 7.5V. For Sourcing tests,  $7.5V \leq V_O \leq 11.5V$ . For Sinking tests,  $2.5V \leq V_O \leq 7.5V$ .

**Note 8:**  $V^+ = 15V$ . Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

**Note 9:** For operating at elevated temperatures the device must be derated based on the thermal resistance  $\theta_{JA}$  with  $P_D = (T_J - T_A)/\theta_{JA}$ .

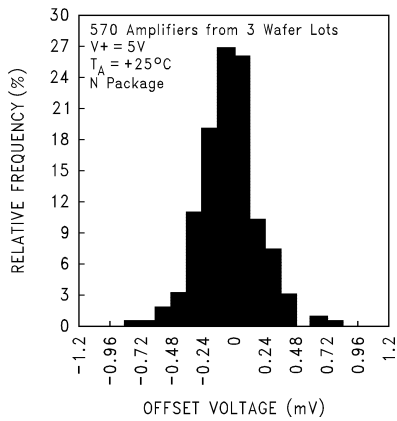
**Note 10:** Do not connect output to  $V^+$ , when  $V^+$  is greater than 13V or reliability will be adversely affected.

**Note 11:** All numbers apply for packages soldered directly into a PC board.

**Note 12:** For guaranteed Military Temperature Range parameters see RETSMC6061X.

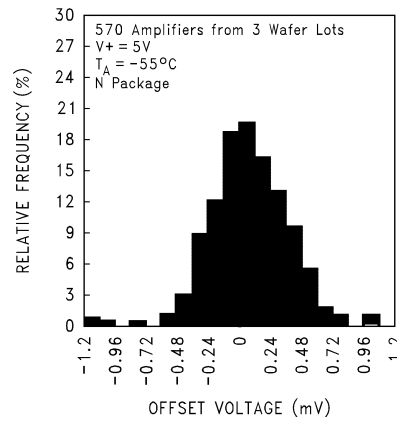
**Typical Performance Characteristics**  $V_S = \pm 7.5V$ ,  $T_A = 25^\circ C$ , Unless otherwise specified

**Distribution of LMC6061  
Input Offset Voltage  
( $T_A = +25^\circ C$ )**



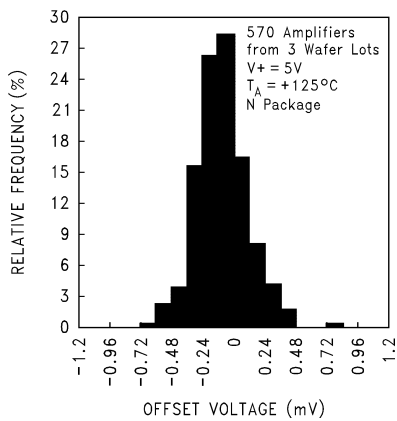
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**Distribution of LMC6061  
Input Offset Voltage  
( $T_A = -55^\circ C$ )**



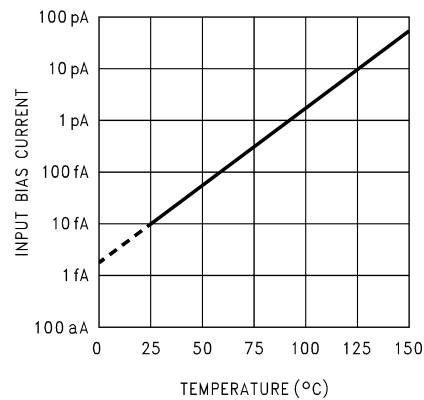
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**Distribution of LMC6061  
Input Offset Voltage  
( $T_A = +125^\circ C$ )**



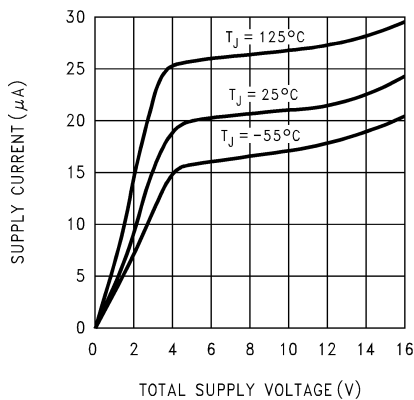
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**Input Bias Current  
vs Temperature**



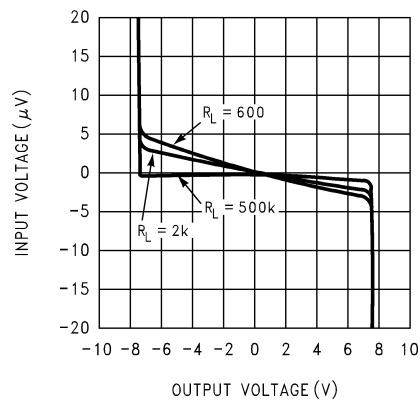
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**Supply Current  
vs Supply Voltage**



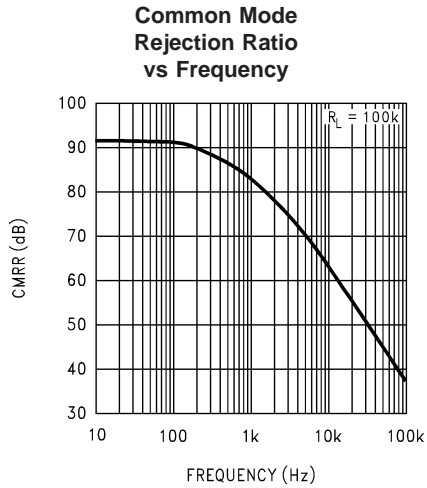
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**Input Voltage  
vs Output Voltage**

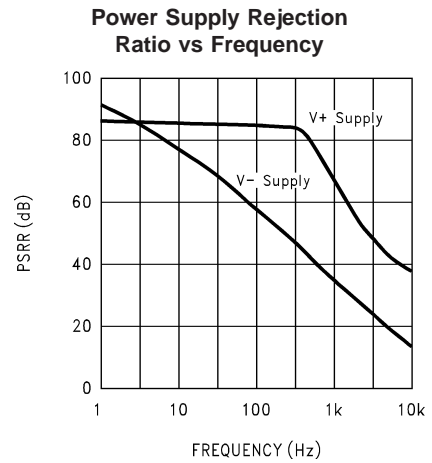


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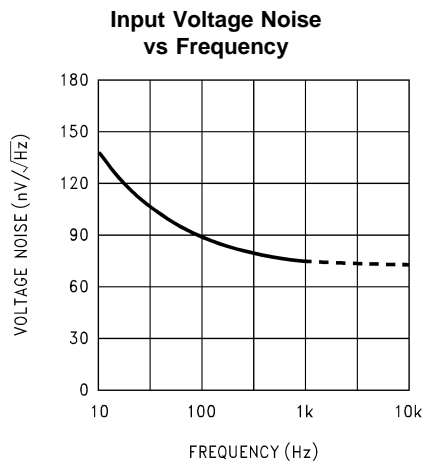
**Typical Performance Characteristics**  $V_S = \pm 7.5V$ ,  $T_A = 25^\circ C$ , Unless otherwise specified (Continued)



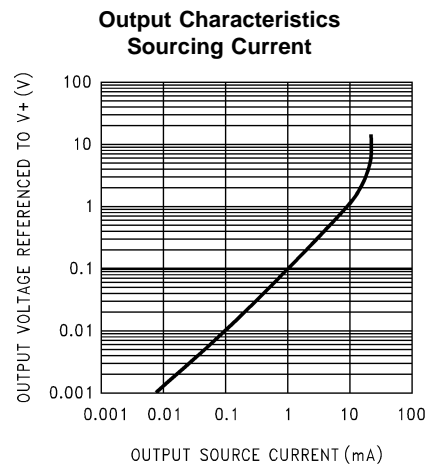
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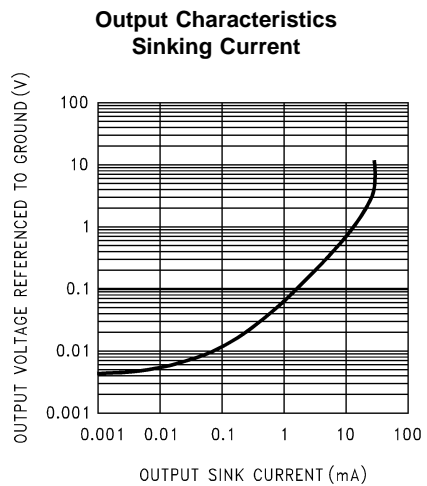
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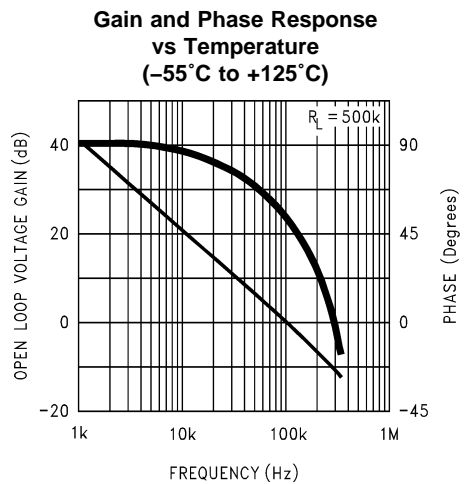
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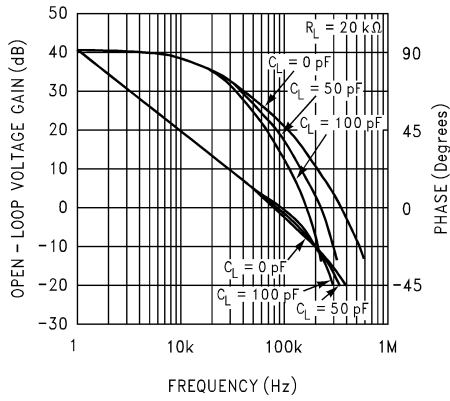


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# Typical Performance Characteristics

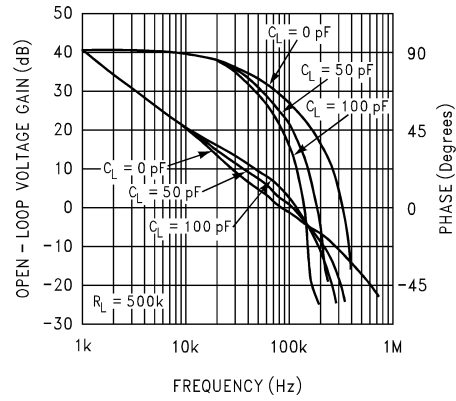
$V_S = \pm 7.5V$ ,  $T_A = 25^\circ C$ , Unless otherwise specified (Continued)

**Gain and Phase Response vs Capacitive Load with  $R_L = 20\text{ k}\Omega$**



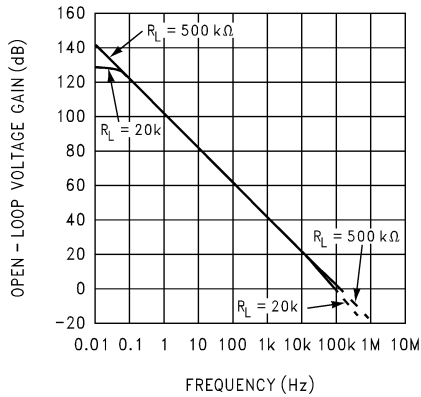
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**Gain and Phase Response vs Capacitive Load with  $R_L = 500\text{ k}\Omega$**



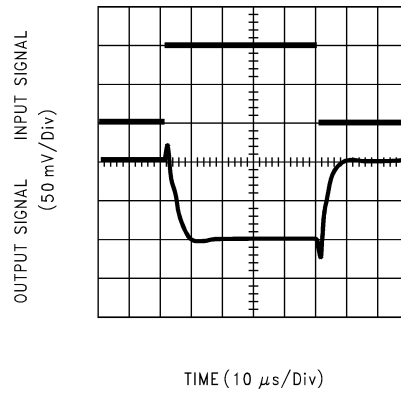
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**Open Loop Frequency Response**



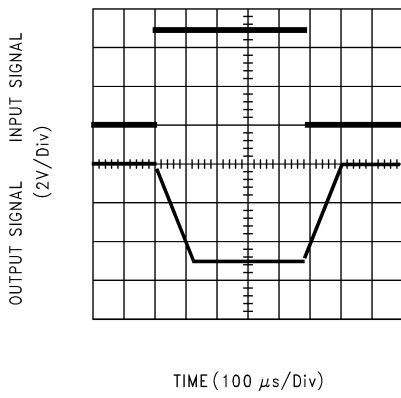
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**Inverting Small Signal Pulse Response**



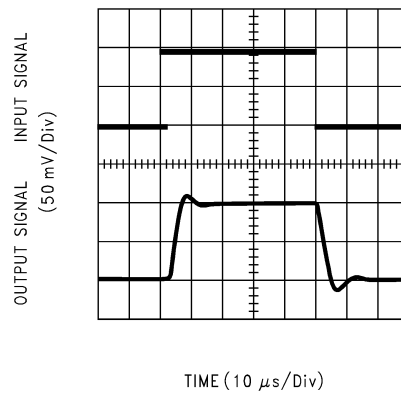
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**Inverting Large Signal Pulse Response**



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**Non-Inverting Small Signal Pulse Response**

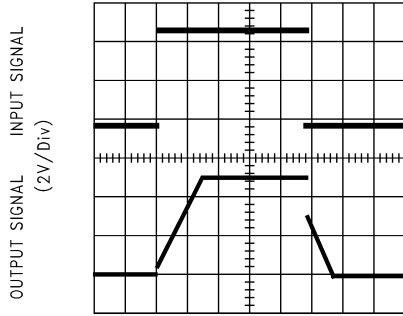


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# Typical Performance Characteristics

$V_S = \pm 7.5V$ ,  $T_A = 25^\circ C$ , Unless otherwise specified (Continued)

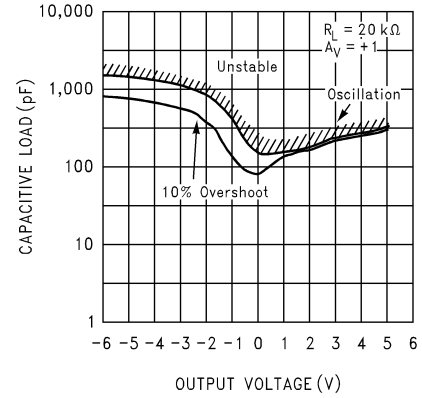
**Non-Inverting Large Signal Pulse Response**



TIME (100  $\mu s$ /Div)

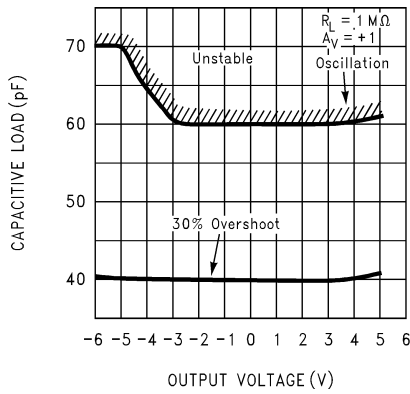
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**Stability vs Capacitive Load,  $R_L = 20\text{ k}\Omega$**



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**Stability vs Capacitive Load  $R_L = 1\text{ M}\Omega$**



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## Applications Hints

### AMPLIFIER TOPOLOGY

The LMC6061 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6061 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

### COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6061.

Although the LMC6061 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6061 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work*).

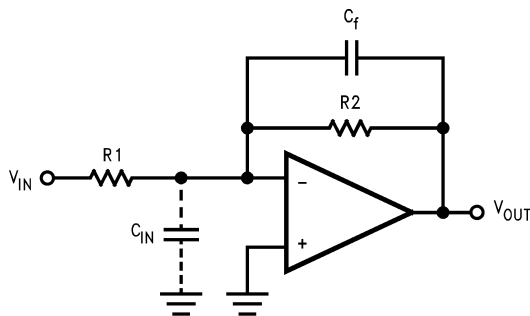
The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor,  $C_f$ , around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of  $C_{IN}$ ,  $C_f$  can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.



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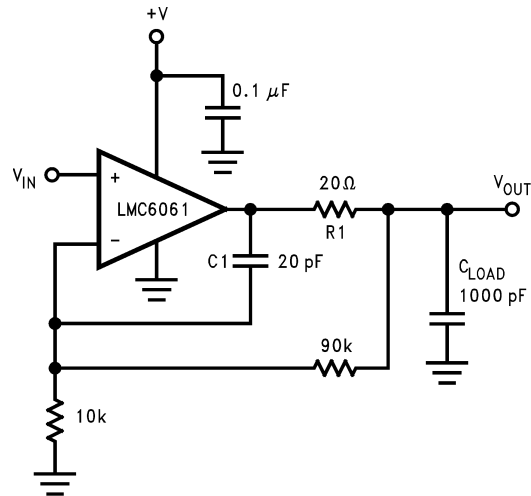
**FIGURE 1. Canceling the Effect of Input Capacitance**

### CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency

location of the dominate pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2*.

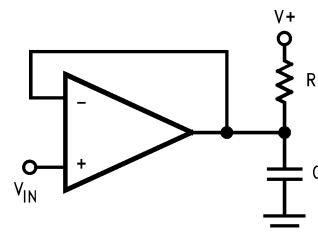


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**FIGURE 2. LMC6061 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads**

In the circuit of *Figure 2*,  $R_1$  and  $C_1$  serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to  $V^+$  *Figure 3*. Typically a pull up resistor conducting 10  $\mu A$  or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see electrical characteristics).



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**FIGURE 3. Compensating for Large Capacitive Loads with a Pull Up Resistor**

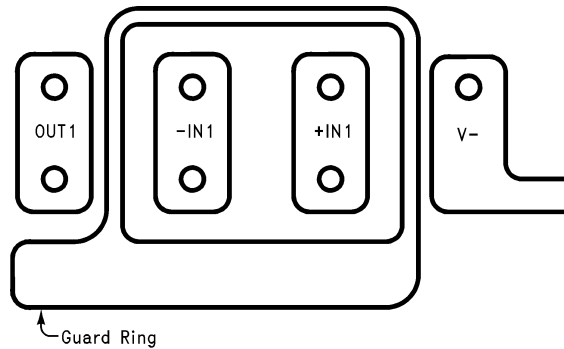
## Applications Hints (Continued)

### PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6061, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6061's inputs and the

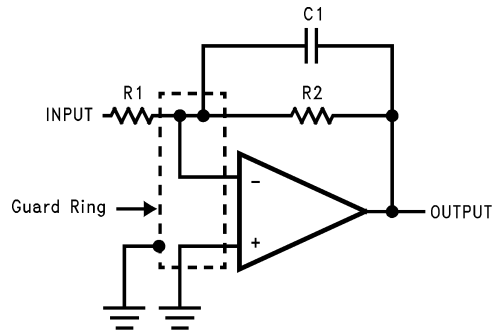
terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in *Figure 4*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of  $10^{12}\Omega$ , which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6061's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of  $10^{11}\Omega$  would cause only 0.05 pA of leakage current. See *Figure 5* for typical connections of guard rings for standard op-amp configurations.



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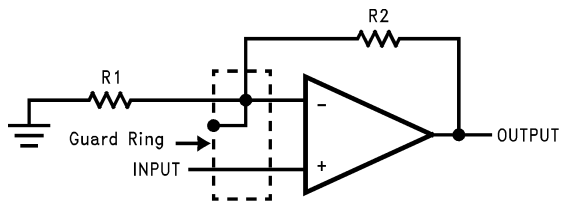
FIGURE 4. Example of Guard Ring in P.C. Board Layout

## Applications Hints (Continued)



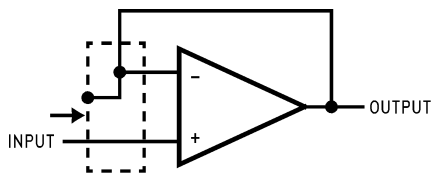
Inverting Amplifier

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Non-Inverting Amplifier

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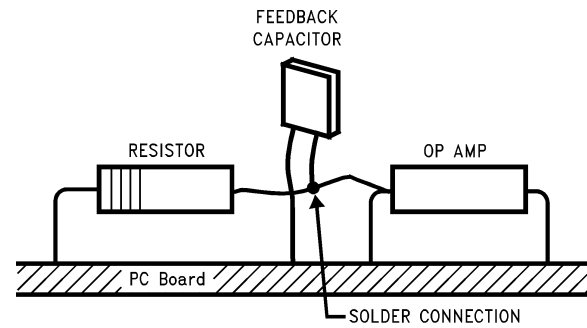


Follower

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**FIGURE 5. Typical Connections of Guard Rings**

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 6*.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

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**FIGURE 6. Air Wiring**

## Latchup

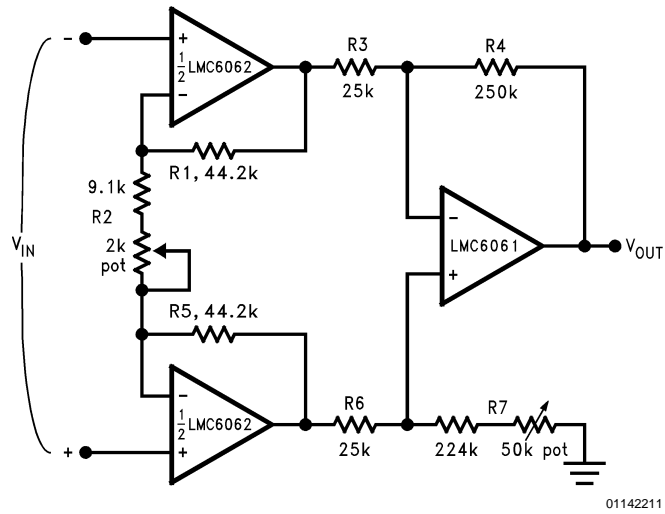
CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6061 and LMC6081 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.

## Typical Single-Supply Applications $(V^+ = 5.0 V_{DC})$

The extremely high input impedance, and low power consumption, of the LMC6061 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

*Figure 7* shows an instrumentation amplifier that features high differential and common mode input resistance ( $>10^{14}\Omega$ ), 0.01% gain accuracy at  $A_V = 100$ , excellent CMRR with 1 k $\Omega$  imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5  $\mu V/^{\circ}C$ .  $R_2$  provides a simple means of adjusting gain over a wide range without degrading CMRR.  $R_7$  is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.

# Typical Single-Supply Applications (V<sup>+</sup> = 5.0 V<sub>DC</sub>) (Continued)

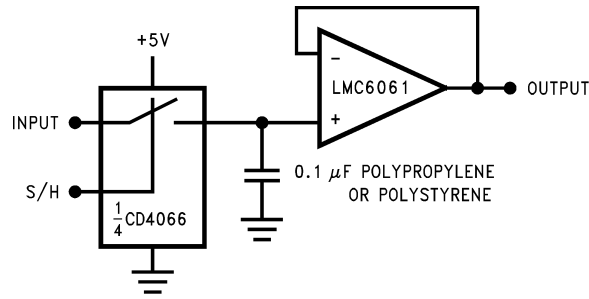


If  $R_1 = R_5$ ,  $R_3 = R_6$ , and  $R_4 = R_7$ ; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$  for circuit shown ( $R_2 = 9.822k$ ).

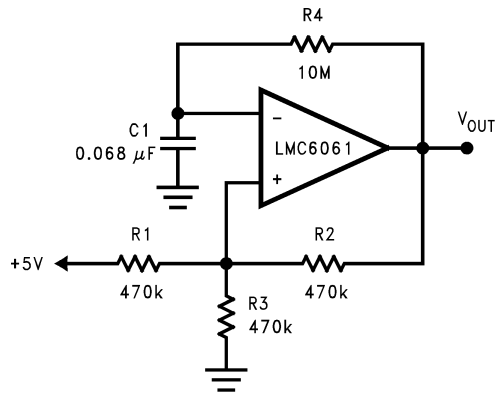
**FIGURE 7. Instrumentation Amplifier**



**FIGURE 8. Low-Leakage Sample and Hold**

## Typical Single-Supply Applications

( $V^+ = 5.0 V_{DC}$ ) (Continued)



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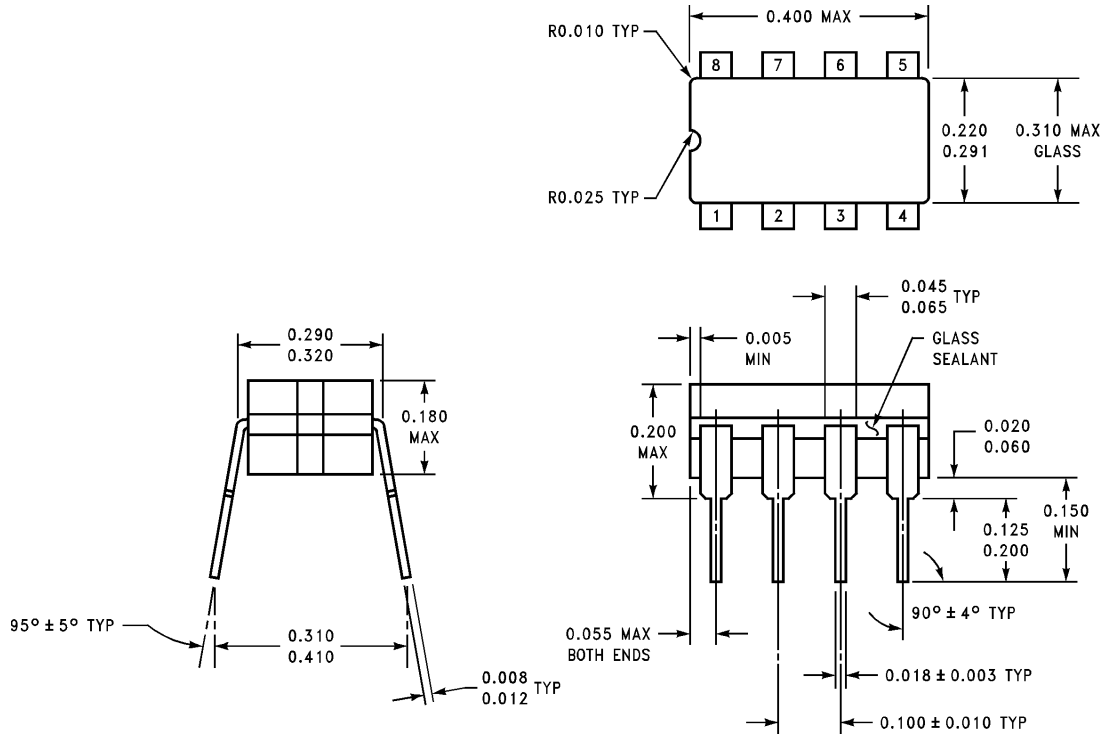
FIGURE 9. 1 Hz Square Wave Oscillator

## Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military -55°C to +125°C	Industrial -40°C to +85°C		
8-Pin Molded DIP		LMC6061AIN LMC6061IN	N08E	Rail
8-Pin Small Outline		LMC6061AIM, LMC606AIMX LMC6061IM, LMC6061IMX	M08A	Rail Tape and Reel
8-Pin Ceramic DIP	LMC6061AMJ/883		J08A	Rail

**Physical Dimensions** inches (millimeters)

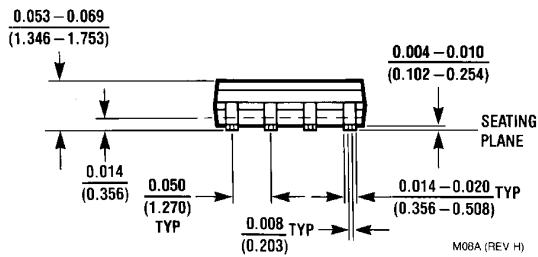
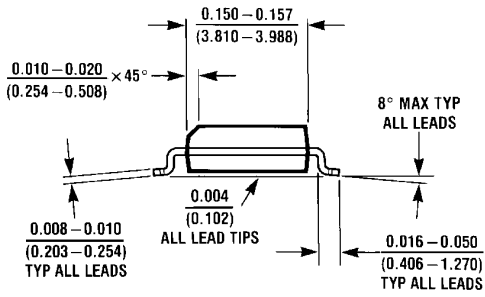
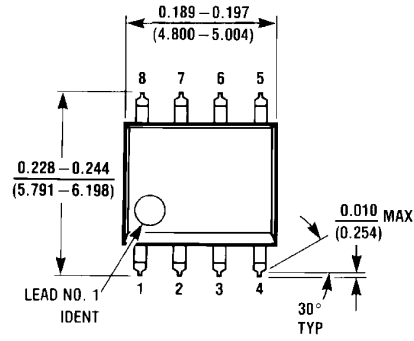
unless otherwise noted



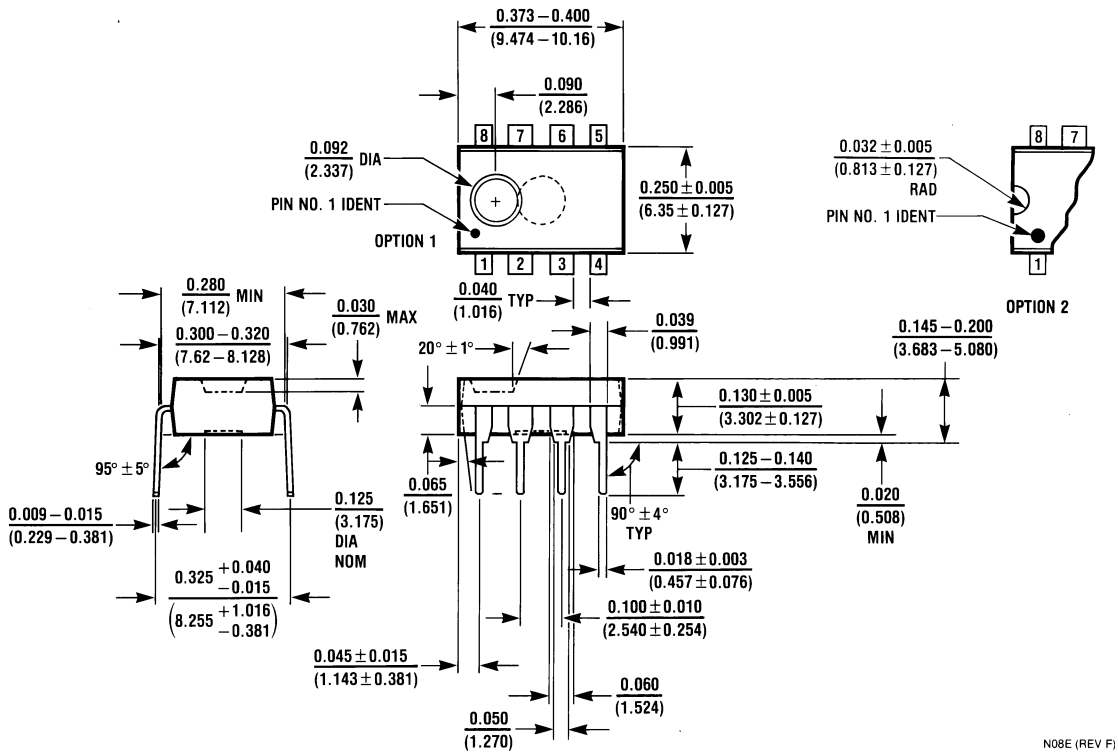
J08A (REV K)

**8-Pin Ceramic Dual-In-Line Package**  
**Order Number LMC6061AMJ/883**  
**NS Package Number J08A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**8-Pin Small Outline Package**  
 Order Number LMC6061AIM, LMC6061AIMX, LMC6061IM or LMC6061IMX  
 NS Package Number M08A



**8-Pin Molded Dual-In-Line Package**  
 Order Number LMC6061AIN or LMC6061IN  
 NS Package Number N08E

## Notes

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