



# TSV620, TSV620A, TSV621, TSV621A

## Rail-to-rail input/output 29 $\mu$ A 420 kHz CMOS operational amplifiers

### Features

- Low supply voltage: 1.5 V–5.5 V
- Rail-to-rail input and output
- Low input offset voltage: 800  $\mu$ V max (A version)
- Low power consumption: 29  $\mu$ A typ
- Low power shutdown mode: 5nA typ (TSV620)
- Gain bandwidth product: 420 kHz typ
- Unity gain stability
- Micropackages: SC70-5/6, SOT23-5/6
- Low input bias current: 1 pA typ
- Extended temperature range: -40 to +125° C
- 4 kV HBM

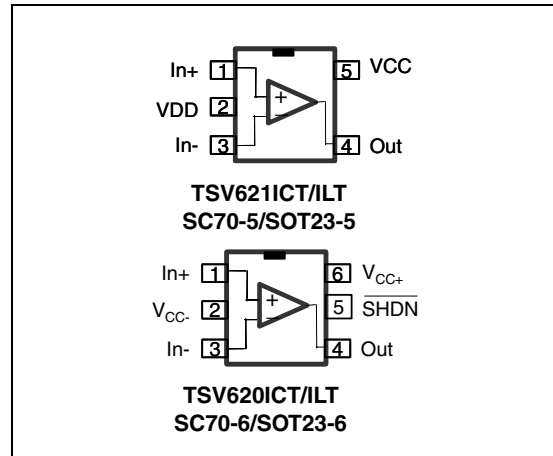
### Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation

### Description

The TSV620 and TSV621 are single operational amplifiers offering low voltage, low power operation and rail-to-rail input and output.

With a very low input bias current and low offset voltage (800  $\mu$ V maximum for the A version), the TSV62x is ideal for applications requiring precision. The device can operate at a power supply ranging from 1.5 to 5.5 V, and therefore suits battery-powered devices and extends their battery life.



This product features an excellent speed/power consumption ratio, offering a 420 kHz gain bandwidth while consuming only 29  $\mu$ A at a 5 V supply voltage.

These operational amplifiers are unity gain stable for capacitive loads up to 100 pF.

The device is internally adjusted to provide very narrow dispersion of AC and DC parameters, especially power consumption, product gain bandwidth and slew rate.

The TSV62x presents a high tolerance to ESD, sustaining 4 kV for the human body model.

The devices are offered in macropackages, SC70-6 and SOT23-6 for the TSV620 and SC70-5 and SOT23-5 for the TSV621. They are guaranteed for industrial temperature ranges from -40° C to +125° C.

All these features make the TSV620 and TSV621 ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering.

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# 1 Absolute maximum ratings and operating conditions

**Table 1. Absolute maximum ratings (AMR)**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage <sup>(1)</sup>	6	V
$V_{id}$	Differential input voltage <sup>(2)</sup>	$\pm V_{CC}$	V
$V_{in}$	Input voltage <sup>(3)</sup>	$V_{CC-} - 0.2$ to $V_{CC+} + 0.2$	V
$I_{in}$	Input current <sup>(4)</sup>	10	mA
$\overline{SHDN}$	Shutdown voltage <sup>(5)</sup>	$V_{CC-} - 0.2$ to $V_{CC+} + 0.2$	V
$T_{stg}$	Storage temperature	-65 to +150	°C
$R_{thja}$	Thermal resistance junction to ambient <sup>(6)(7)</sup>		°C/W
	SC70-5	205	
	SOT23-5	250	
	SOT23-6	240	
	SC70-6	232	
$T_j$	Maximum junction temperature	150	°C
ESD	HBM: human body model <sup>(8)</sup>	4	kV
	MM: machine model <sup>(9)</sup>	300	V
	CDM: charged device model <sup>(10)</sup>	1.5	kV
	Latch-up immunity	200	mA

- All voltage values, except differential voltage are with respect to network ground terminal.
- Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
- $V_{CC} - V_{in}$  must not exceed 6 V.
- Input current must be limited by a resistor in series with the inputs.
- $V_{CC} - \overline{SHDN}$  must not exceed 6 V.
- Short-circuits can cause excessive heating and destructive dissipation.
- $R_{th}$  are typical values.
- Human body model: 100 pF discharged through a 1.5 k $\Omega$  resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
- Machine mode: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5  $\Omega$ ), done for all couples of pin combinations with other pins floating.
- Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

**Table 2. Operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	1.5 to 5.5	V
$V_{icm}$	Common mode input voltage range	$V_{CC-} - 0.1$ to $V_{CC+} + 0.1$	V
$T_{oper}$	Operating free air temperature range	-40 to +125	°C

## 2 Electrical characteristics

**Table 3. Electrical characteristics at  $V_{CC+} = +1.8\text{ V}$  with  $V_{DD} = 0\text{ V}$ ,  $V_{icm} = V_{CC}/2$ ,  $T_{op} = 25^\circ\text{ C}$ , and  $R_L$  connected to  $V_{CC}/2$  (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$V_{io}$	Offset voltage	TSV62x TSV62xA			4 0.8	mV
		$T_{min} < T_{op} < T_{max}$ TSV62x TSV62xA			6 2.8	
$DV_{io}$	Input offset voltage drift			2		$\mu\text{V}/^\circ\text{C}$
$I_{io}$	Input offset current ( $V_{out} = V_{CC}/2$ )			1	$10^{(1)}$	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
$I_{ib}$	Input bias current ( $V_{out} = V_{CC}/2$ )			1	$10^{(1)}$	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	$0\text{ V to }1.8\text{ V}$ , $V_{out} = 0.9\text{ V}$	53	74		dB
		$T_{min} < T_{op} < T_{max}$	51			
$A_{vd}$	Large signal voltage gain	$R_L = 10\text{ k}\Omega$ , $V_{out} = 0.5\text{ V to }1.3\text{ V}$	78	95		dB
		$T_{min} < T_{op} < T_{max}$	73			
$V_{OH}$	High level output voltage	$R_L = 10\text{ k}\Omega$	35	5		mV
		$T_{min} < T_{op} < T_{max}$	50			
$V_{OL}$	Low level output voltage	$R_L = 10\text{ k}\Omega$		4	35	mV
		$T_{min} < T_{op} < T_{max}$			50	
$I_{out}$	Isink	$V_o = 1.8\text{ V}$	6	12		mA
		$T_{min} < T_{op} < T_{max}$	4			
	Isource	$V_o = 0\text{ V}$	6	10		mA
		$T_{min} < T_{op} < T_{max}$	4			
$I_{CC}$	Supply current (per operator)	No load, $V_{out} = V_{CC}/2$		25	31	$\mu\text{A}$
		$T_{min} < T_{op} < T_{max}$			33	
<b>AC performance</b>						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $f = 100\text{ kHz}$	275	340		kHz
$F_u$	Unity gain frequency	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		280		kHz
$\phi_m$	Phase margin	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		45		Degrees
$G_m$	Gain margin	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		9		dB
SR	Slew rate	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $A_v = 1$	0.084	0.11	0.14	$\text{V}/\mu\text{s}$

1. Guaranteed by design.

Table 4. Shutdown characteristics  $V_{CC} = 1.8\text{ V}$ 

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$I_{CC}$	Supply current in shutdown mode (all operators)	$\overline{\text{SHDN}} = V_{CC-}$		2.5	50	nA
		$T_{\min} < T_{\text{op}} < 85^\circ\text{ C}$			200	nA
		$T_{\min} < T_{\text{op}} < 125^\circ\text{ C}$			1.5	$\mu\text{A}$
$t_{\text{on}}$	Amplifier turn-on time	$R_L = 2\text{ k}\Omega$ , $V_{\text{out}} = V_{CC-}$ to $V_{CC} + 0.2$		300		ns
$t_{\text{off}}$	Amplifier turn-off time	$R_L = 2\text{ k}\Omega$ , $V_{\text{out}} = V_{CC+} - 0.5$ to $V_{CC+} + 0.7$		30		ns
$V_{\text{IH}}$	$\overline{\text{SHDN}}$ logic high		1.3			V
$V_{\text{IL}}$	$\overline{\text{SHDN}}$ logic low				0.5	V
$I_{\text{IH}}$	$\overline{\text{SHDN}}$ current high	$\overline{\text{SHDN}} = V_{CC+}$		10		$\mu\text{A}$
$I_{\text{IL}}$	$\overline{\text{SHDN}}$ current low	$\overline{\text{SHDN}} = V_{CC-}$		10		$\mu\text{A}$
$I_{\text{OLeak}}$	Output leakage in shutdown mode	$\overline{\text{SHDN}} = V_{CC-}$		50		$\mu\text{A}$
		$T_{\min} < T_{\text{op}} < 125^\circ\text{ C}$		1		nA

**Table 5.**  $V_{CC+} = +3.3\text{ V}$ ,  $V_{CC-} = 0\text{ V}$ ,  $V_{icm} = V_{CC}/2$ ,  $T_{op} = 25^\circ\text{ C}$ ,  $R_L$  connected to  $V_{CC}/2$   
(unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$V_{io}$	Offset voltage	TSV62x TSV62xA			4 0.8	mV
		$T_{min} < T_{op} < T_{max}$ TSV62x TSV62xA			6 2.8	
$DV_{io}$	Input offset voltage drift			2		$\mu\text{V}/^\circ\text{C}$
$I_{io}$	Input offset current			1	$10^{(1)}$	pA
		$T_{min} < T_{op} < T_{max}$		1	100	pA
$I_{ib}$	Input bias current			1	$10^{(1)}$	pA
		$T_{min} < T_{op} < T_{max}$		1	100	pA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	0 V to 3.3 V, $V_{out} = 1.75\text{ V}$	57	79		dB
		$T_{min} < T_{op} < T_{max}$	53			dB
$A_{vd}$	Large signal voltage gain	$R_L = 10\text{ k}\Omega$ , $V_{out} = 0.5\text{ V to } 2.8\text{ V}$	81	98		dB
		$T_{min} < T_{op} < T_{max}$	76			dB
$V_{OH}$	High level output voltage	$R_L = 10\text{ k}\Omega$	35	5		mV
		$T_{min} < T_{op} < T_{max}$	50			
$V_{OL}$	Low level output voltage	$R_L = 10\text{ k}\Omega$		4	35	mV
		$T_{min} < T_{op} < T_{max}$			50	
$I_{out}$	Isink	$V_o = 5\text{ V}$	30	45		mA
		$T_{min} < T_{op} < T_{max}$	25			
	Isource	$V_o = 0\text{ V}$	30	38		mA
		$T_{min} < T_{op} < T_{max}$	25			
$I_{CC}$	Supply current (per operator)	No load, $V_{out} = 2.5\text{ V}$		26	33	$\mu\text{A}$
		$T_{min} < T_{op} < T_{max}$			35	$\mu\text{A}$
<b>AC performance</b>						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $f = 100\text{ kHz}$	310	380		kHz
$F_u$	Unity gain frequency	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		310		kHz
$\phi_m$	Phase margin	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		45		Degrees
$G_m$	Gain margin	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		9		dB
SR	Slew rate	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $A_V = 1$	0.094	0.12		$\text{V}/\mu\text{s}$

1. Guaranteed by design.

**Table 6.**  $V_{CC+} = +5\text{ V}$ ,  $V_{CC-} = 0\text{ V}$ ,  $V_{icm} = V_{CC}/2$ ,  $T_{op} = 25^\circ\text{ C}$ ,  $R_L$  connected to  $V_{CC}/2$   
(unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$V_{io}$	Offset voltage	TSV62x TSV62xA			4 0.8	mV
		$T_{min} < T_{op} < T_{max}$ TSV62x TSV62xA			6 2.8	
$DV_{io}$	Input offset voltage drift			2		$\mu\text{V}/^\circ\text{C}$
$I_{io}$	Input offset current			1	$10^{(1)}$	pA
		$T_{min} < T_{op} < T_{max}$		1	100	pA
$I_{ib}$	Input bias current			1	$10^{(1)}$	pA
		$T_{min} < T_{op} < T_{max}$		1	100	pA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	0 V to 5 V, $V_{out} = 2.5\text{ V}$	60	80		dB
		$T_{min} < T_{op} < T_{max}$	55			
SVR	Supply voltage rejection ratio $20 \log (\Delta V_{CC}/\Delta V_{io})$	$V_{CC} = 1.8\text{ to }5\text{ V}$	75	102		dB
		$T_{min} < T_{op} < T_{max}$	73			
$A_{vd}$	Large signal voltage gain	$R_L = 10\text{ k}\Omega$ , $V_{out} = 0.5\text{ V to }4.5\text{ V}$	85	98		dB
		$T_{min} < T_{op} < T_{max}$	80			
$V_{OH}$	High level output voltage	$R_L = 10\text{ k}\Omega$	35	7		mV
		$T_{min} < T_{op} < T_{max}$	50			
$V_{OL}$	Low level output voltage	$R_L = 10\text{ k}\Omega$		6	35	mV
		$T_{min} < T_{op} < T_{max}$			50	
$I_{out}$	$I_{sink}$	$V_o = 5\text{ V}$	40	69		mA
		$T_{min} < T_{op} < T_{max}$	35	65		
	$I_{source}$	$V_o = 0\text{ V}$	40	74		mA
		$T_{min} < T_{op} < T_{max}$	35	68		
$I_{CC}$	Supply current (per operator)	No load, $V_{out} = 2.5\text{ V}$		29	36	$\mu\text{A}$
		$T_{min} < T_{op} < T_{max}$			38	$\mu\text{A}$
<b>AC performance</b>						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $f = 100\text{ kHz}$	350	420		kHz
$F_u$	Unity gain frequency	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		360		kHz
$\phi_m$	Phase margin	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		45		Degrees
$G_m$	Gain margin	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		9		dB
SR	Slew rate	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $A_V = 1$	0.108	0.14		$\text{V}/\mu\text{s}$

**Table 6.**  $V_{CC+} = +5\text{ V}$ ,  $V_{CC-} = 0\text{ V}$ ,  $V_{icm} = V_{CC}/2$ ,  $T_{op} = 25^\circ\text{ C}$ ,  $R_L$  connected to  $V_{CC}/2$   
(unless otherwise specified) (continued)

Symbol	Parameter		Min.	Typ.	Max.	Unit
$e_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$		70		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
THD	Total harmonic distortion	$A_v = 1$ , $f = 1\text{ kHz}$ , $R_L = 100\text{ k}\Omega$ $V_{icm} = V_{CC}/2$ , $V_{out} = 2\text{ V}_{pp}$		0.004		%

1. Guaranteed by design.

**Table 7.** Shutdown characteristics  $V_{CC} = 5\text{ V}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$I_{CC}$	Supply current in shutdown mode (all operators)	$\overline{\text{SHDN}} = V_{CC-}$		5	50	nA
		$T_{min} < T_{op} < 85^\circ\text{ C}$			200	nA
		$T_{min} < T_{op} < 125^\circ\text{ C}$			1.5	$\mu\text{A}$
$t_{on}$	Amplifier turn-on time	$R_L = 2\text{ k}\Omega$ , $V_{out} = V_{CC-}$ to $V_{CC+} - 0.2$		300		ns
$t_{off}$	Amplifier turn-off time	$R_L = 2\text{ k}\Omega$ , $V_{out} = V_{CC+} - 0.5$ to $V_{CC+} + 0.7$		30		ns
$V_{IH}$	$\overline{\text{SHDN}}$ logic high		4.5			V
$V_{IL}$	$\overline{\text{SHDN}}$ logic low				0.5	V
$I_{IH}$	$\overline{\text{SHDN}}$ current high	$\overline{\text{SHDN}} = V_{CC+}$		10		$\mu\text{A}$
$I_{IL}$	$\overline{\text{SHDN}}$ current low	$\overline{\text{SHDN}} = V_{CC-}$		10		$\mu\text{A}$
$I_{OLeak}$	Output leakage in shutdown mode	$\overline{\text{SHDN}} = V_{CC-}$		50		$\mu\text{A}$
		$T_{min} < T_{op} < 125^\circ\text{ C}$		1		nA



Figure 1. Input offset voltage vs input common mode at  $V_{CC+} = 1.5\text{ V}$

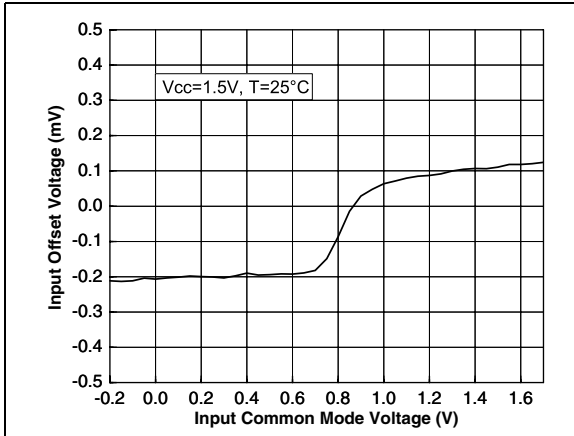


Figure 2. Input offset voltage vs input common mode at  $V_{CC+} = 5\text{ V}$

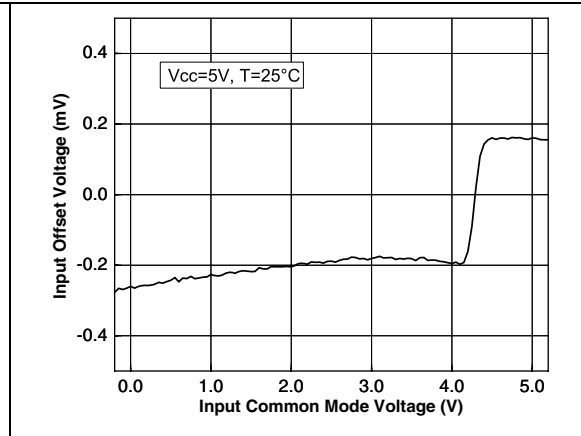


Figure 3. Supply current vs. supply voltage at  $V_{icm} = V_{CC}/2$

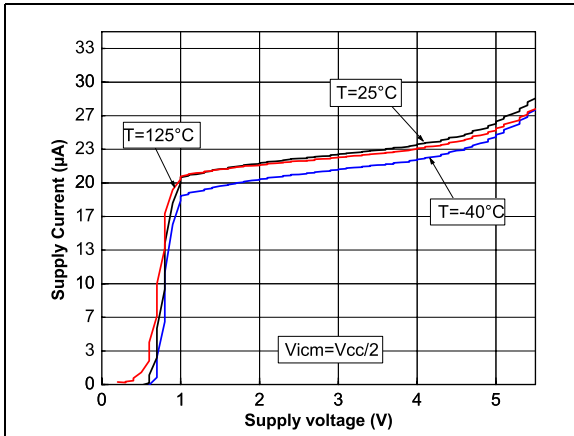


Figure 4. Output current vs. output voltage at  $V_{CC+} = 1.5\text{ V}$

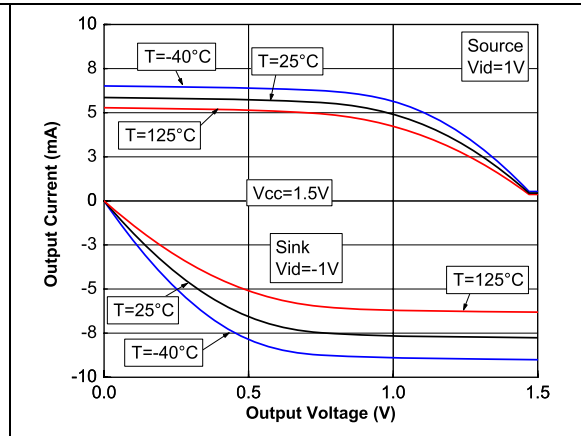


Figure 5. Output current vs. output voltage at  $V_{CC+} = 5\text{ V}$

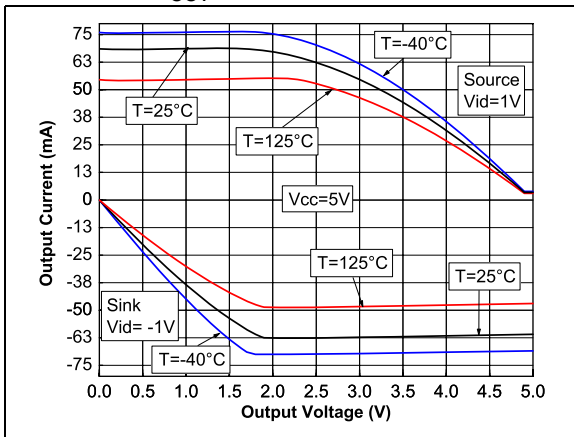


Figure 6. Voltage gain and phase vs. frequency at  $V_{CC+} = 1.5\text{ V}$

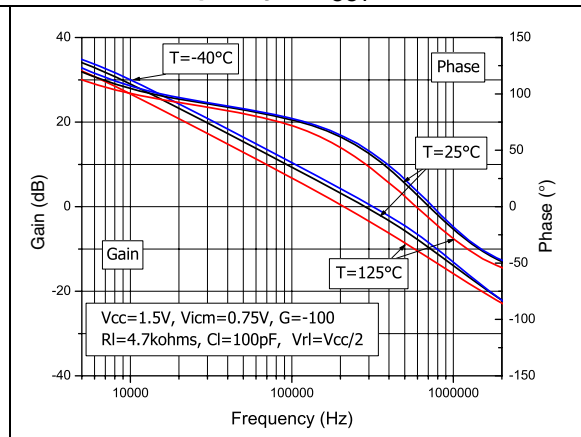


Figure 7. Voltage gain and phase vs. frequency at  $V_{CC+} = 5\text{ V}$

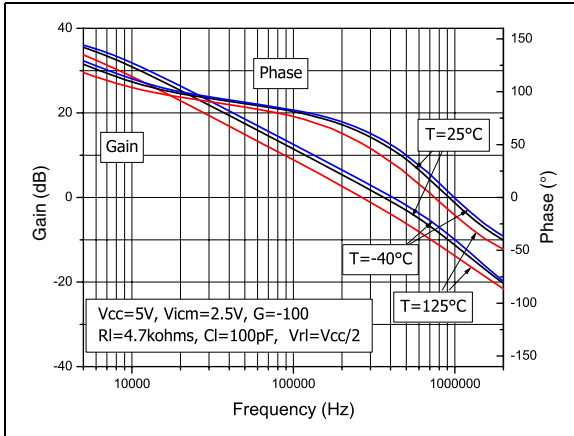


Figure 8. Phase margin vs. output current at  $V_{CC+} = 1.5\text{ V}$  and  $V_{CC+} = 5\text{ V}$

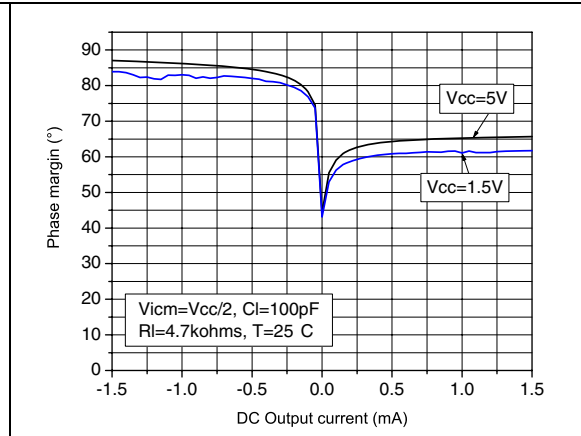


Figure 9. Slew rate vs. supply voltage

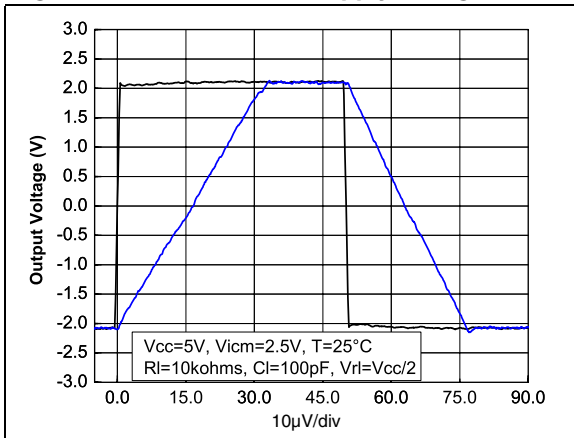


Figure 10. Slew rate vs. supply voltage

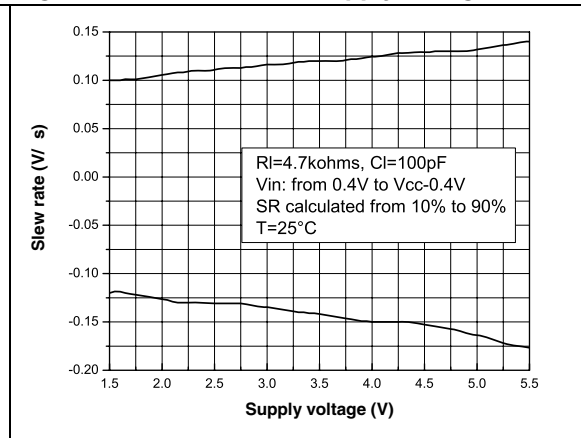


Figure 11. Distortion + noise vs. output voltage

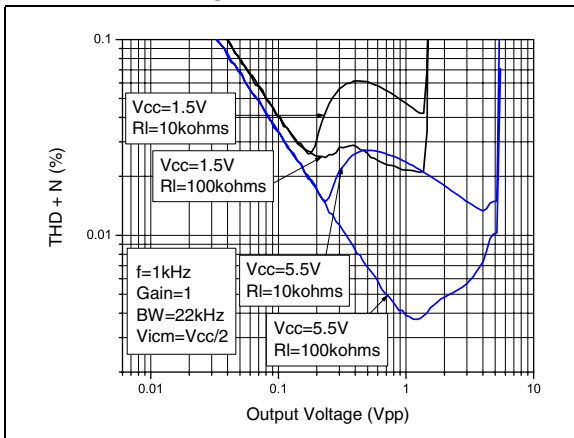


Figure 12. Distortion + noise vs. frequency

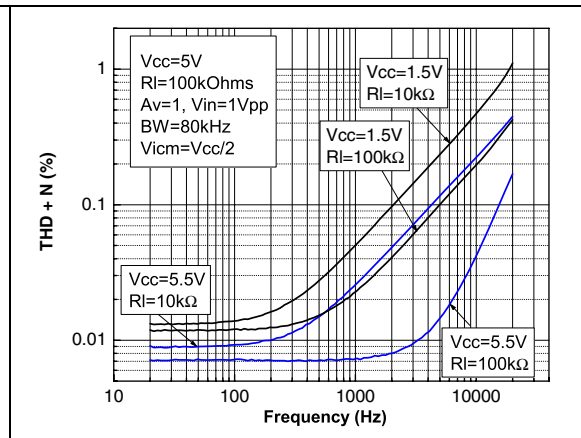
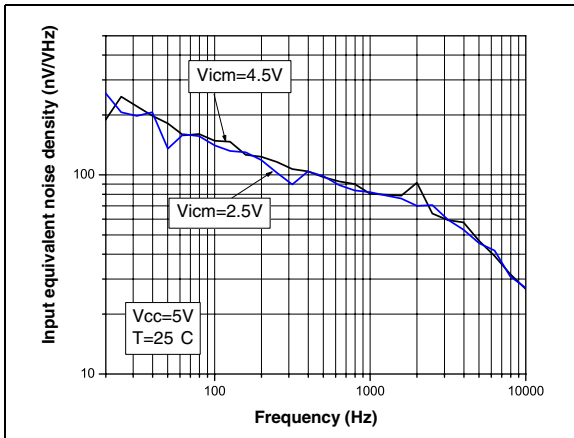


Figure 13. Noise vs. frequency



## 3 Application information

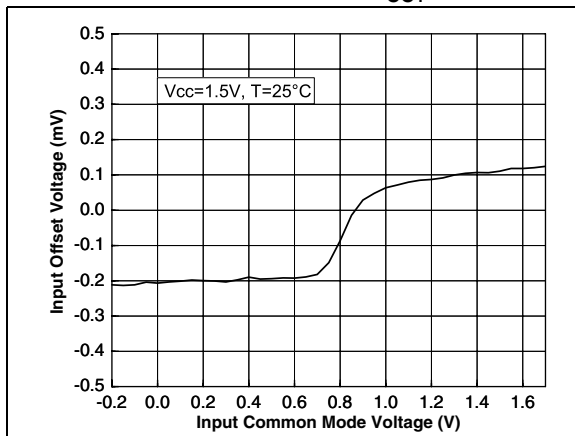
### 3.1 Operating voltages

The TSV620 and TSV621 can operate from 1.5 to 5.5 V. Their parameters are fully specified for 1.8, 3.3 and 5 V power supplies. However, the parameters are very stable in the full  $V_{CC}$  range and several characterization curves show the TSV62x characteristics at 1.5 V. Additionally, the main specifications are guaranteed in extended temperature ranges from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

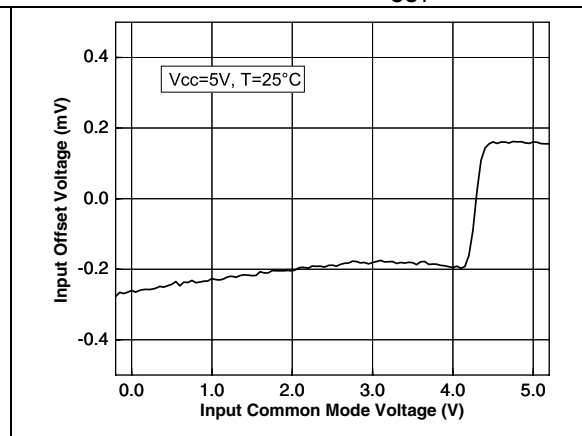
### 3.2 Rail-to-rail input

The TSV62x is built with two complementary PMOS and NMOS input differential pairs. The device has a rail-to-rail input and the input common mode range is extended from  $V_{CC-} - 0.1\text{ V}$  to  $V_{CC+} + 0.1\text{ V}$ . The transition between the two pairs appears at  $V_{CC-} - 0.7\text{ V}$ . In the transition region, the performances of CMRR, PSRR,  $V_{io}$  and THD are slightly degraded (as shown in [Figure 14](#) and [Figure 15](#) for  $V_{io}$  vs.  $V_{icm}$ ).

**Figure 14. Input offset voltage vs input common mode at  $V_{CC+} = 1.5\text{ V}$**



**Figure 15. Input offset voltage vs input common mode at  $V_{CC+} = 5\text{ V}$**



The device is guaranteed without phase reversal.

### 3.3 Rail-to-rail output

The operational amplifier's output level can go close to the rails: 35 mV maximum above and below the rail when connected to a 10 k $\Omega$  resistive load to  $V_{CC}/2$ .

### 3.4 Shutdown function (TSV620)

The operational amplifier is enabled when the  $\overline{\text{SHDN}}$  pin is pulled high. To disable the amplifier, the  $\overline{\text{SHDN}}$  pin must be pulled down to  $V_{\text{CC-}}$ . When in shutdown mode, the amplifier output is in a high impedance state. The  $\overline{\text{SHDN}}$  pin must never be left floating but tied to  $V_{\text{CC+}}$  or  $V_{\text{CC-}}$ .

The turn-on and turn-off times are calculated for an output variation of  $\pm 200$  mV (Figure 16 and Figure 17 show the test configurations).

Figure 16. Test configuration for turn-on time (Vout pulled down)

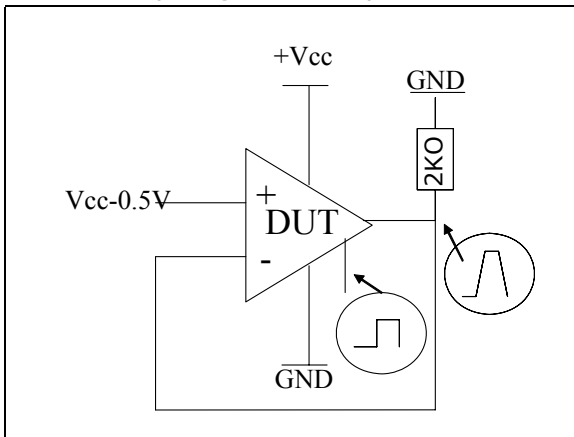


Figure 17. Test configuration for turn-off time (Vout pulled down)

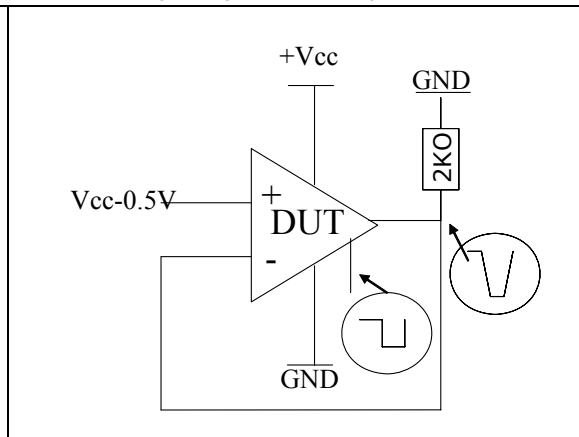


Figure 18. Turn-on time,  $V_{\text{CC}} = 5$  V, Vout pulled down,  $T = 25^\circ\text{C}$

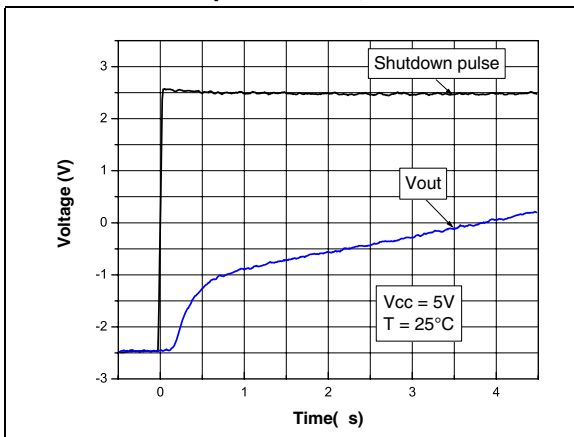
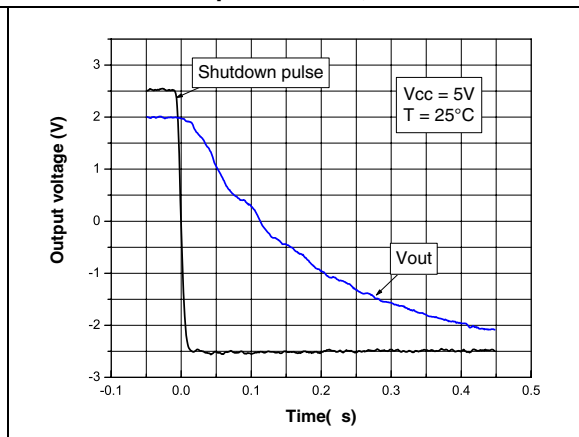


Figure 19. Turn-off time,  $V_{\text{CC}} = 5$  V, Vout pulled down,  $T = 25^\circ\text{C}$



### 3.5 Optimization of DC and AC parameters

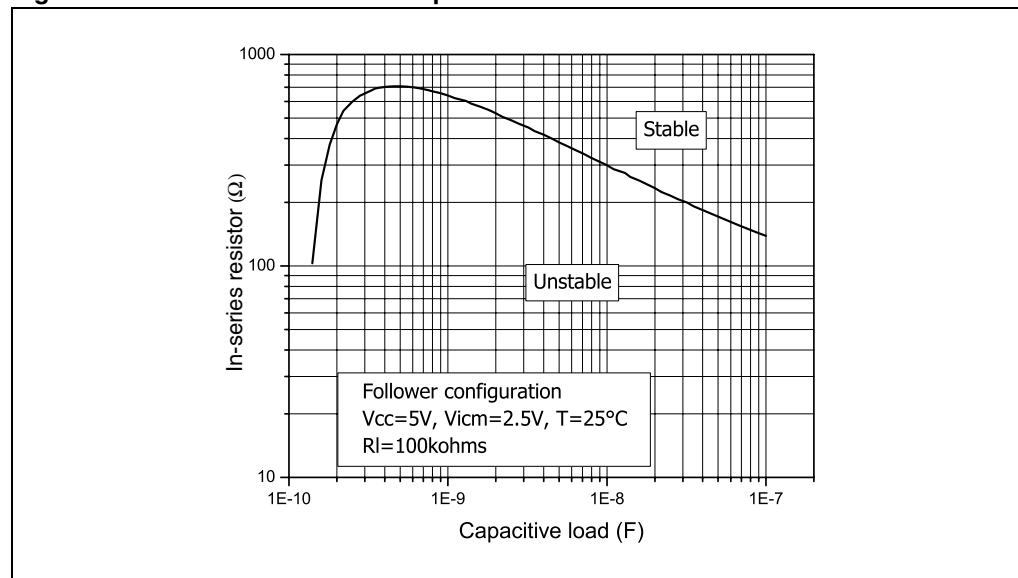
This device uses an innovative approach to reduce the spread of the main DC and AC parameters. An internal adjustment achieves a very narrow spread of current consumption (29  $\mu\text{A}$  typical, min/max at  $\pm 17\%$ ). Parameters linked to the current consumption value, such as GBP, SR and AVd benefit from this narrow dispersion. All parts present a similar speed and the same behavior in terms of stability. In addition, the minimum values of GBP and SR are guaranteed (GBP = 350 kHz min, SR = 0.15 V/ $\mu\text{s}$  min).

### 3.6 Driving resistive and capacitive loads

These products are micro-power, low-voltage operational amplifiers optimized to drive rather large resistive loads, above 5 k $\Omega$ . For lower resistive loads, the THD level may significantly increase.

In a *follower* configuration, these operational amplifiers can drive capacitive loads up to 100 pF with no oscillations. When driving larger capacitive loads, adding a small in-series resistor at the output can improve the stability of the device (see [Figure 20](#) for recommended in-series resistor values). Once the in-series resistor has been selected, the stability of the circuit should be tested on bench and simulated with the simulation model.

**Figure 20. In-series resistor vs. capacitive load**



### 3.7 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

### 3.8 Macromodel

An accurate macromodel of TSV620-TSV621 is available on STMicroelectronics' web site at [www.st.com](http://www.st.com). This model is a trade-off between accuracy and complexity (that is, time simulation) of the TSV62x operational amplifiers. It emulates the nominal performances of a typical device within the specified operating conditions mentioned in the datasheet. It helps to validate a design approach and to select the right operational amplifier, *but it does not replace on-board measurements*.

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.



## 4.1 SOT23-5 package mechanical data

Figure 21. SOT23-5L package mechanical drawing

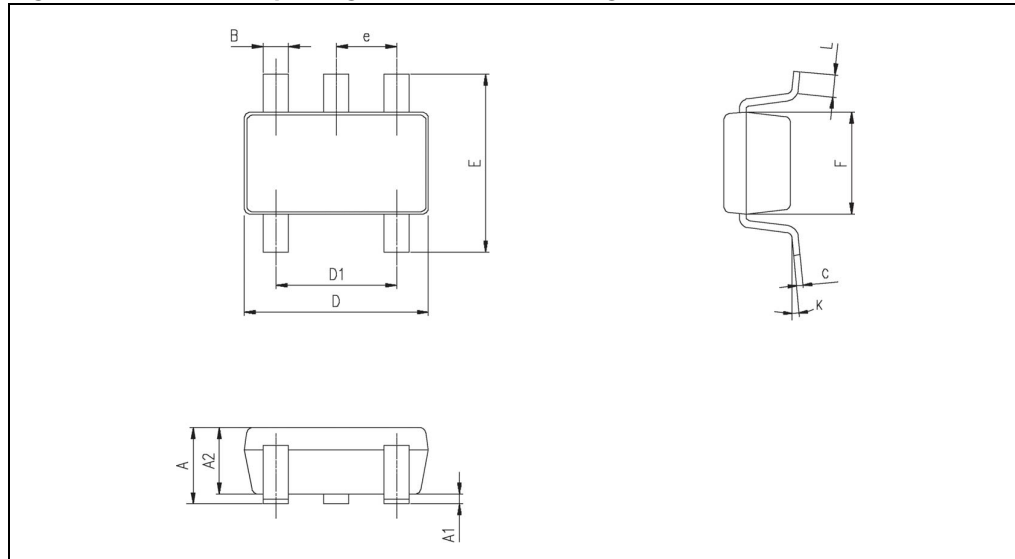


Table 8. SOT23-5L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.013	0.015	0.019
C	0.09	0.15	0.20	0.003	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.013	0.023
K	0°		10°			

## 4.2 SOT23-6 package mechanical data

Figure 22. SOT23-6L package mechanical drawing

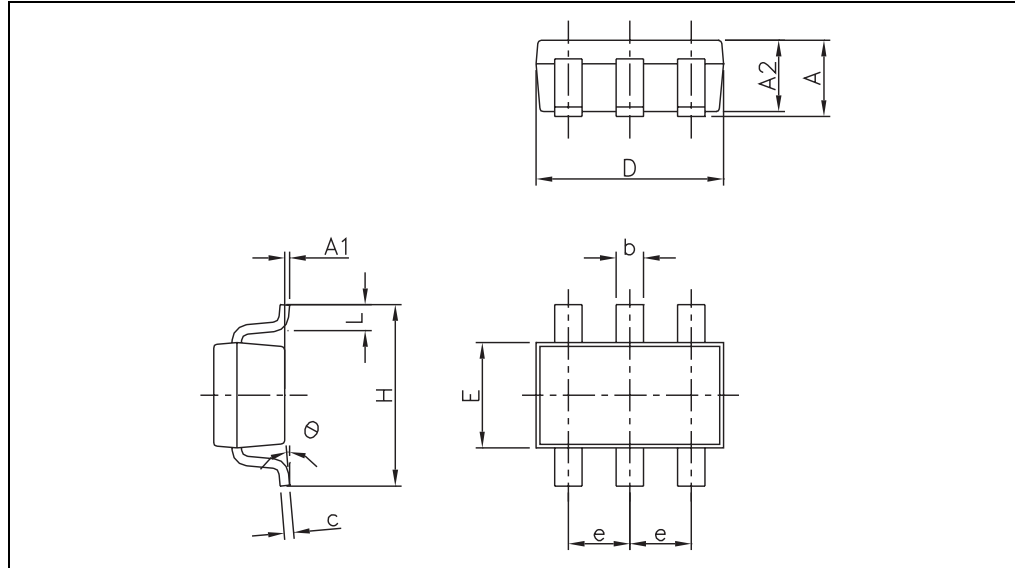


Table 9. SOT23-6L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1			0.10			0.004
A2	0.90		1.30	0.035		0.051
b	0.35		0.50	0.013		0.019
c	0.09		0.20	0.003		0.008
D	2.80		3.05	0.110		0.120
E	1.50		1.75	0.060		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.10		0.60	0.004		0.024
°	0		10°			

### 4.3 SC70-5 (or SOT323-5) package mechanical data

Figure 23. SC70-5 (or SOT323-5) package mechanical drawing

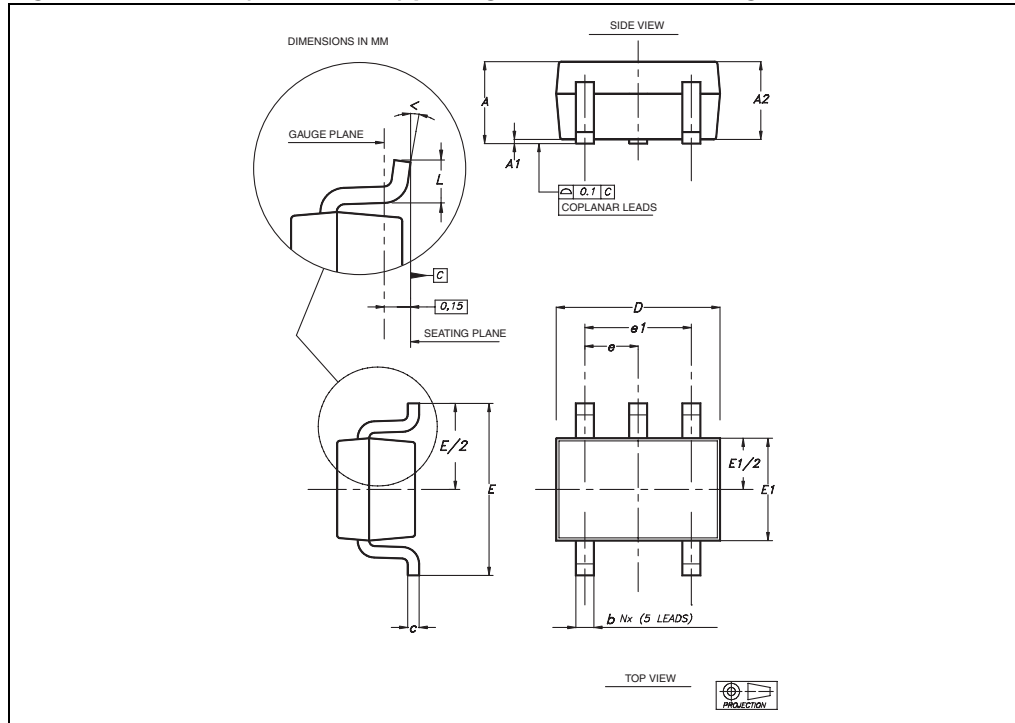


Table 10. SC70-5 (or SOT323-5) package mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.80		1.10	0.315		0.043
A1			0.10			0.004
A2	0.80	0.90	1.00	0.315	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.22	0.004		0.009
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65			0.025	
e1		1.30			0.051	
L	0.26	0.36	0.46	0.010	0.014	0.018
<	0°		8°			

### 4.4 SC70-6 (or SOT323-6) package mechanical data

Figure 24. SC70-6 (or SOT323-6) package mechanical drawing

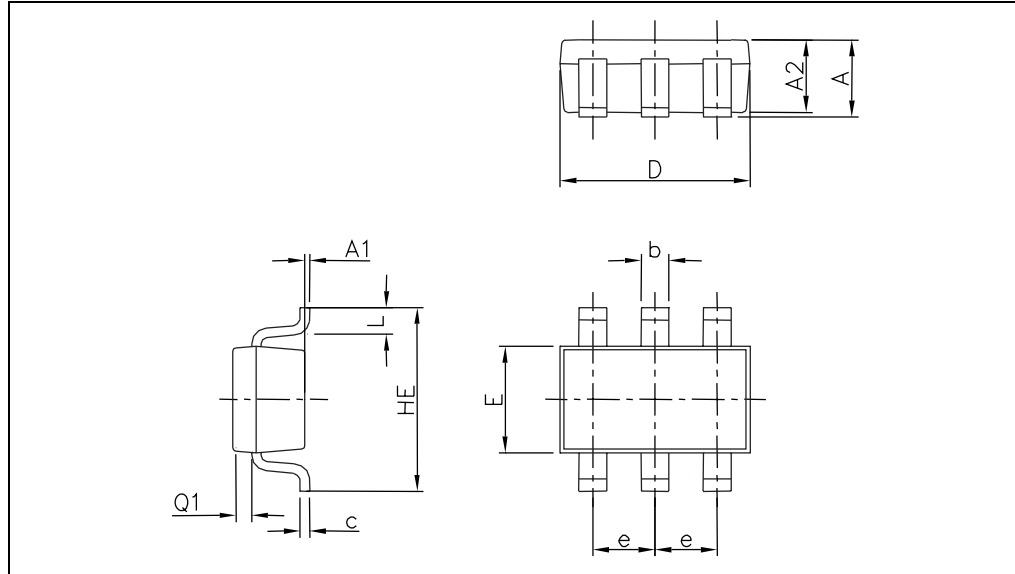
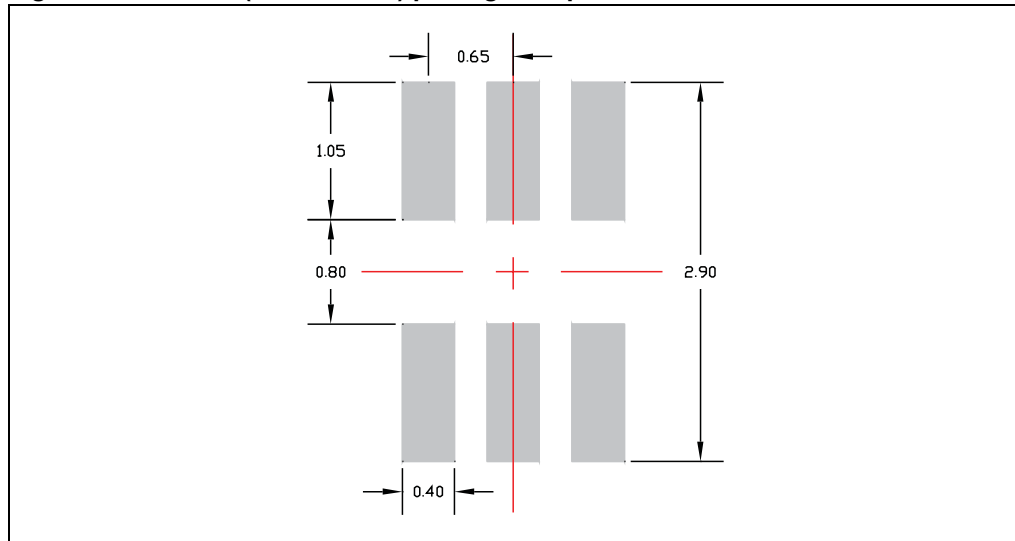


Table 11. SC70-6 (or SOT323-6) package mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.031		0.043
A1			0.10			0.004
A2	0.80		1.00	0.031		0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.18	0.004		0.007
D	1.80		2.20	0.071		0.086
E	1.15		1.35	0.045		0.053
e		0.65			0.026	
HE	1.80		2.40	0.071		0.094
L	0.10		0.40	0.004		0.016
Q1	0.10		0.40	0.004		0.016

Figure 25. SC70-6 (or SOT323-6) package footprint



## 5 Ordering information

Table 12. Order codes

Part number	Temperature range	Package	Packing	Marking
TSV620ILT	-40° C to +125° C	SOT23-6	Tape & reel	K107
TSV620ICT		SC70-6		K14
TSV620AILT		SOT23-6		K110
TSV620AICT		SC70-6		K15
TSV621ILT		SOT23-5		K106
TSV621ICT		SC70-5		K16
TSV621AILT		SOT23-5		K139
TSV621AICT		SC70-5		K39

## 6 Revision history

**Table 13. Document revision history**

Date	Revision	Changes
12-Jan-2009	1	Initial release.
19-Oct-2009	2	Added TSV620 device (version with shutdown function). Added <a href="#">Table 4: Shutdown characteristics <math>V_{CC} = 1.8\text{ V}</math></a> . Added <a href="#">Table 7: Shutdown characteristics <math>V_{CC} = 5\text{ V}</math></a> . Added <a href="#">Section 3.4: Shutdown function (TSV620) on page 13</a> . Added <a href="#">Section 4.2: SOT23-6 package mechanical data</a> . Added <a href="#">Section 4.4: SC70-6 (or SOT323-6) package mechanical data</a> . Added order codes in <a href="#">Table 12</a> .

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