

### FEATURES

- Very low voltage noise: 1.8 nV/ $\sqrt{\text{Hz}}$**
- Low input bias current: 100 nA maximum**
- Offset voltage: 100  $\mu\text{V}$  maximum**
- High gain: 120 dB**
- Wide bandwidth: 12 MHz**
- $\pm 5\text{ V}$  to  $\pm 15\text{ V}$  operation**

### APPLICATIONS

- Precision instrumentation**
- Filter blocks**
- Microphone preamplifier**
- Industrial control**
- Thermocouples and RTDs**
- Reference buffers**

### GENERAL DESCRIPTION

The ADA4004-4 is a 1.8 nV/ $\sqrt{\text{Hz}}$  precision quad amplifier in a 16-lead, 4 mm  $\times$  4 mm LFCSP package featuring 40  $\mu\text{V}$  offset, 0.7  $\mu\text{V}/^\circ\text{C}$  drift, 12 MHz bandwidth, and low 1.7 mA per amplifier supply current.

The ADA4004-4 is designed on the high performance *iPolar*<sup>™</sup> process, enabling improvements such as reduced noise and power consumption, increased speed and stability, and smaller footprint size. Novel design techniques enable the ADA4004-4 to achieve 1.8 nV/ $\sqrt{\text{Hz}}$  voltage noise density and a low 6 Hz 1/f noise corner frequency while consuming just 1.7 mA per amplifier. The small package saves board space, reduces cost, and improves layout flexibility.

Applications for these amplifiers include high precision controls, PLL filters, high performance precision filters, medical and analytical instrumentation, precision power supply controls, ATE, and data acquisition systems.

The high performance ADA4004-4 is offered in the very small 16-lead, 4 mm  $\times$  4 mm LFCSP and the 14-lead, narrow SOIC, RoHS compliant, surface-mount packages. Operation is fully specified from  $\pm 5\text{ V}$  to  $\pm 15\text{ V}$  from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

### PIN CONFIGURATIONS

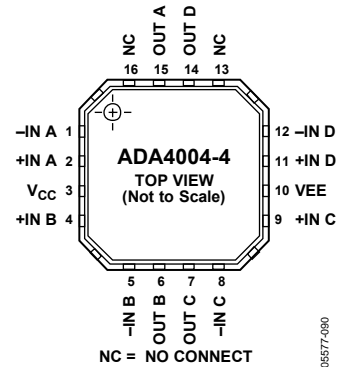


Figure 1. 16-Lead LFCSP  
(CP-16-4 Suffix)

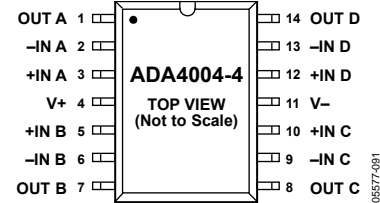


Figure 2. 14-Lead SOIC  
(R-14 Suffix)

#### Rev. B

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

## TABLE OF CONTENTS

Features .....	1	Absolute Maximum Ratings .....	5
Applications.....	1	Thermal Resistance .....	5
General Description .....	1	ESD Caution.....	5
Pin Configurations .....	1	Typical Performance Characteristics .....	6
Revision History .....	2	Outline Dimensions .....	12
Specifications.....	3	Ordering Guide .....	12

## REVISION HISTORY

### 11/07—Rev. A to Rev. B

Changed $V_S$ to $V_{SY}$ .....	Universal
Changes to General Description .....	1
Changes to Supply Current per Amplifier .....	3
Changes to Open-Loop Gain .....	4
Changes to Supply Current per Amplifier .....	4
Changes to Figure 10, Figure 11, Figure 13, and Figure 14.....	7
Changes to Figure 26.....	9
Updated Outline Dimensions .....	12
Changes to Ordering Guide .....	12

### 7/06—Rev. 0 to Rev. A

Changes to Table 4.....	5
Updated Outline Dimensions .....	12
Changes to Ordering Guide .....	12

### 1/06—Revision 0: Initial Version

## SPECIFICATIONS

$V_{SY} = \pm 5.0\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	140	$\mu\text{V}$
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	85	nA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	85	nA
Input Voltage Range		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-3.5		+3.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -3.0\text{ V to }+3.0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	105	111		dB
Open-Loop Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = -2.5\text{ V to }+2.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	250	400		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.7	1	$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	$V_{OH}$	$R_L = 2\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	3.7	3.9		V
Output Voltage Low	$V_{OL}$	$R_L = 2\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	3.4	3.6		V
Short-Circuit Limit	$I_{SC}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		25	-3.6	mA
Output Current	$I_O$	$V_{OUT} = \pm 3.6\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		$\pm 10$	-3.5	mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 5.0\text{ V to } \pm 15.0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110	118		dB
Supply Current per Amplifier	$I_{SY}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110		1.8	mA
					2.1	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$ to ground		2.7		V/ $\mu\text{s}$
Gain Bandwidth Product	GBP			12		MHz
NOISE PERFORMANCE						
Voltage Noise	$e_{n\text{ p-p}}$	0.1 Hz to 10 Hz		0.1		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		1.8		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 10\text{ Hz}$		3.5		pA/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 200\text{ Hz}$		1.2		pA/ $\sqrt{\text{Hz}}$

# ADA4004-4

$V_{SY} = \pm 15\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	125	$\mu\text{V}$
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	90	nA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			165	nA
Input Voltage Range		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-12.5		+12.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -12.5\text{ V to } +12.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110	113		dB
Open-Loop Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = -12.0\text{ V to } +12.0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	500	1200		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.7	1	$\mu\text{V}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 2\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	13.4	13.6		V
Output Voltage Low	$V_{OL}$	$R_L = 2\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	13.1	13.3		V
Short-Circuit Limit	$I_{SC}$			25		mA
Output Current	$I_O$	$V_{OUT} = \pm 13.6\text{ V}$		$\pm 10$		mA
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 5.0\text{ V to } \pm 15.0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110	118		dB
Supply Current per Amplifier	$I_{SY}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110		2.0	mA
					2.3	mA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$ to ground		2.7		V/ $\mu\text{s}$
Gain Bandwidth Product	GBP			12		MHz
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_{n,p-p}$	0.1 Hz to 10 Hz		0.15		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		1.8		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 10\text{ Hz}$		3.5		pA/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 200\text{ Hz}$		1.2		pA/ $\sqrt{\text{Hz}}$

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	$\pm 18\text{ V}$ or $+36\text{ V}$
Input Voltage	$\pm\text{V}$ supply
Differential Input Voltage	$\pm\text{V}$ supply
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Operating Temperature Range	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
Junction Temperature Range	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Lead Temperature (Soldering 60 sec)	$300^{\circ}\text{C}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4.

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
14-Lead SOIC (R-14)	120	36	$^{\circ}\text{C}/\text{W}$
16-Lead LFCSP (CP-16-4)	44	31.5	$^{\circ}\text{C}/\text{W}$

## ESD CAUTION



### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## TYPICAL PERFORMANCE CHARACTERISTICS

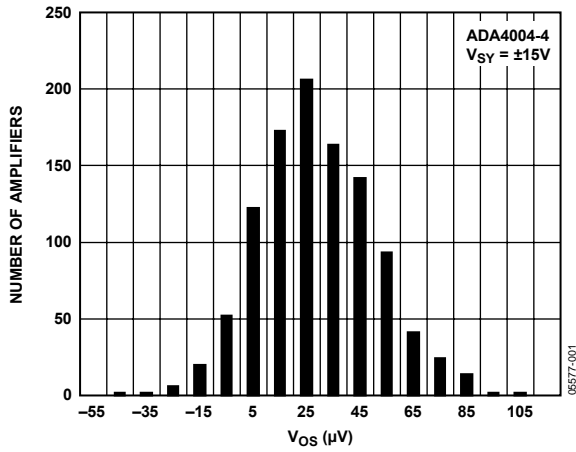


Figure 3. Number of Amplifiers vs. Input Offset Voltage

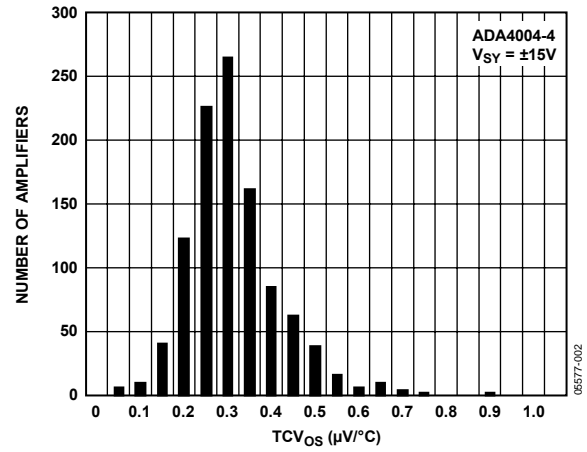


Figure 6. Number of Amplifiers vs.  $TCV_{OS}$

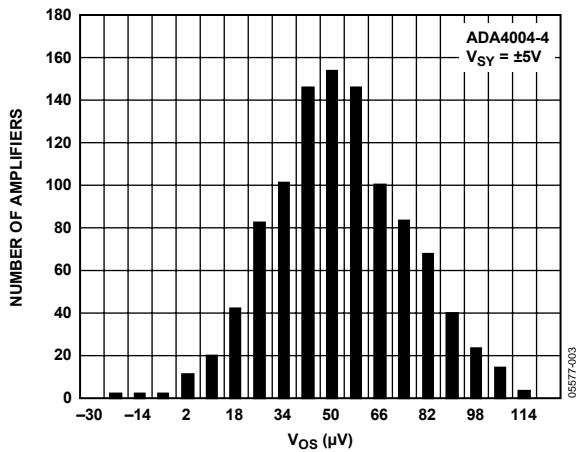


Figure 4. Number of Amplifiers vs. Input Offset Voltage

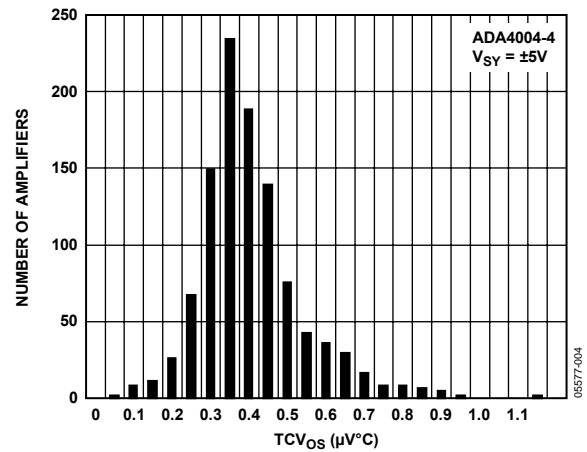


Figure 7. Number of Amplifiers vs.  $TCV_{OS}$

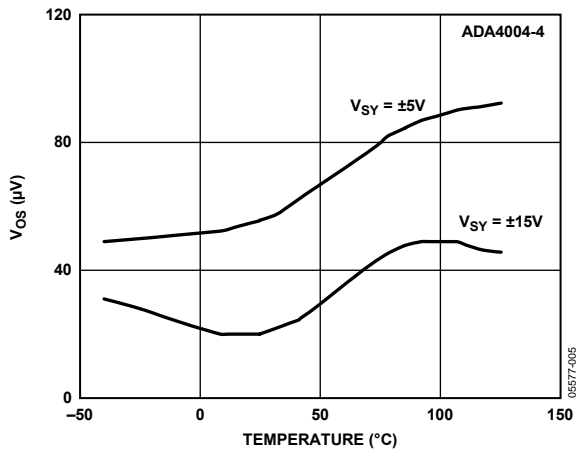


Figure 5. Input Offset Voltage vs. Temperature

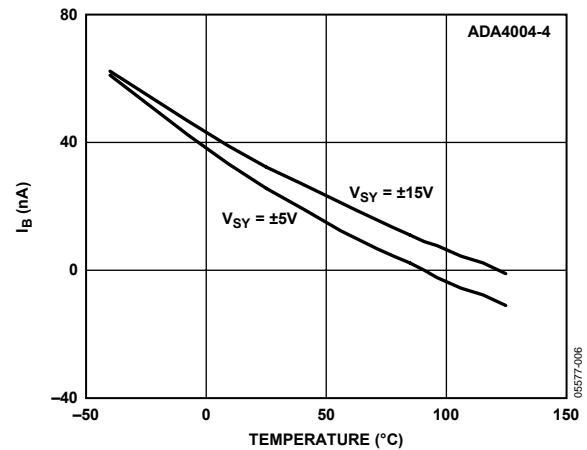


Figure 8. Input Bias Current vs. Temperature

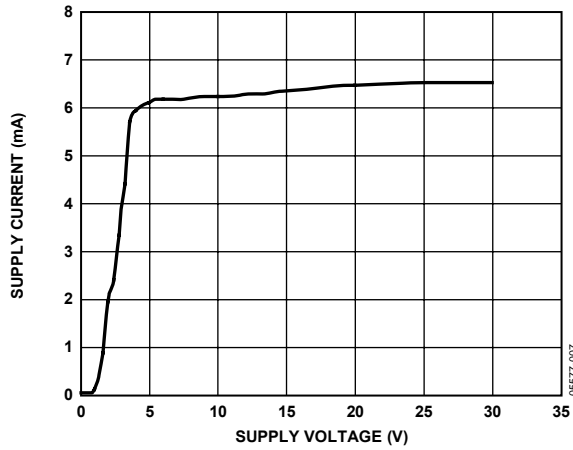


Figure 9. Supply Current vs. Total Supply Voltage

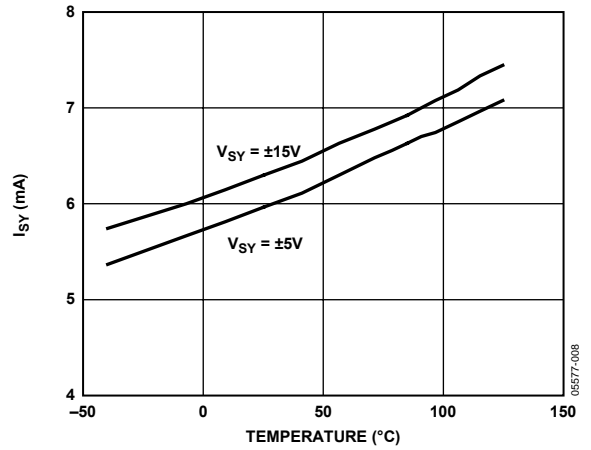


Figure 12. Supply Current vs. Temperature

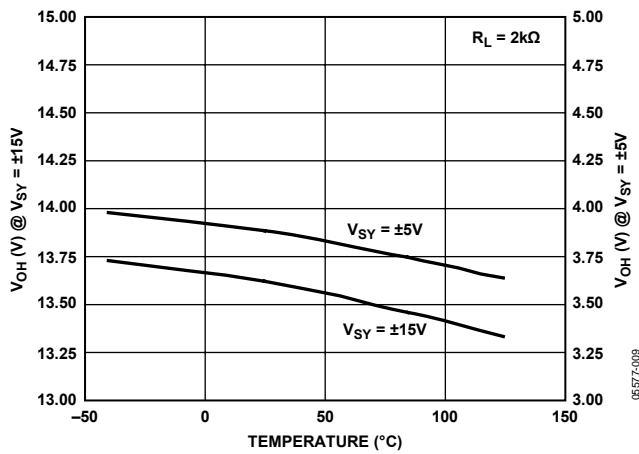


Figure 10.  $V_{OH}$  vs. Temperature

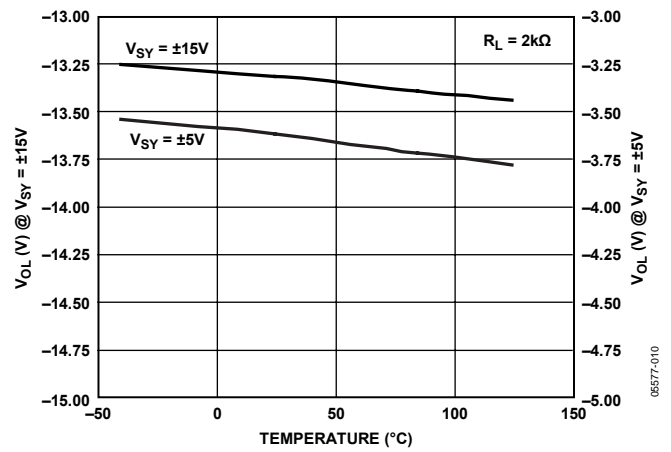


Figure 13.  $V_{OL}$  vs. Temperature

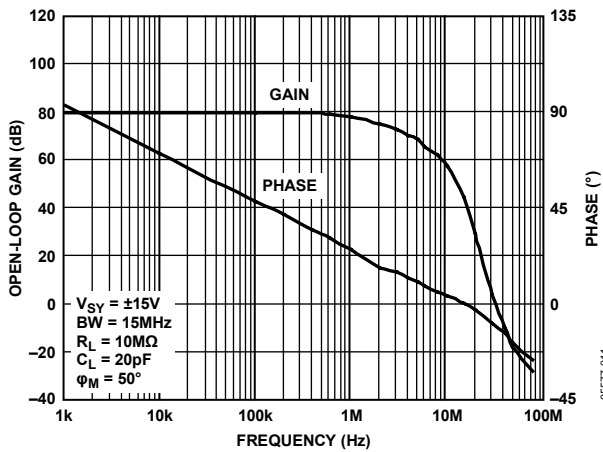


Figure 11. Open-Loop Gain and Phase vs. Frequency

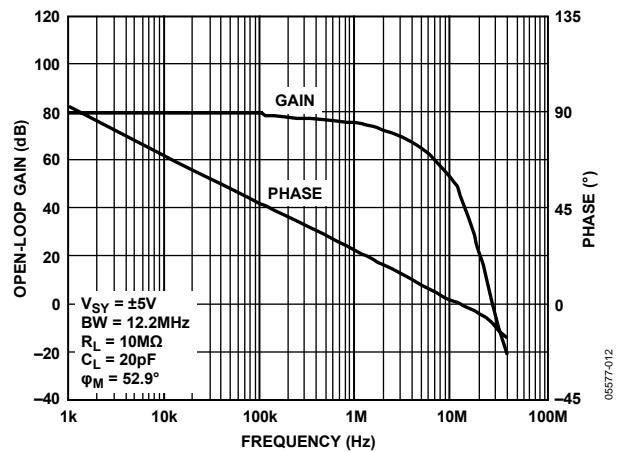


Figure 14. Open-Loop Gain and Phase vs. Frequency

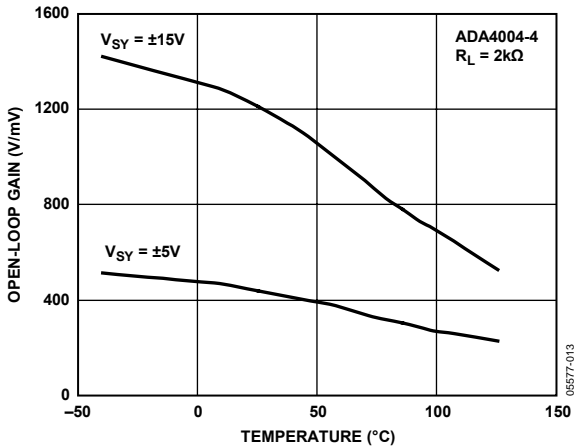


Figure 15. Open-Loop Gain vs. Temperature

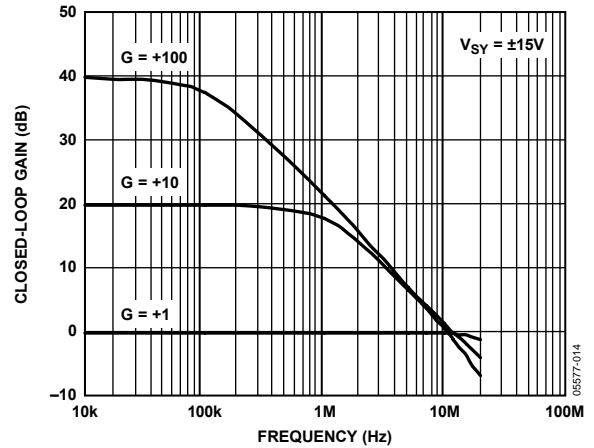


Figure 18. Closed-Loop Gain vs. Frequency

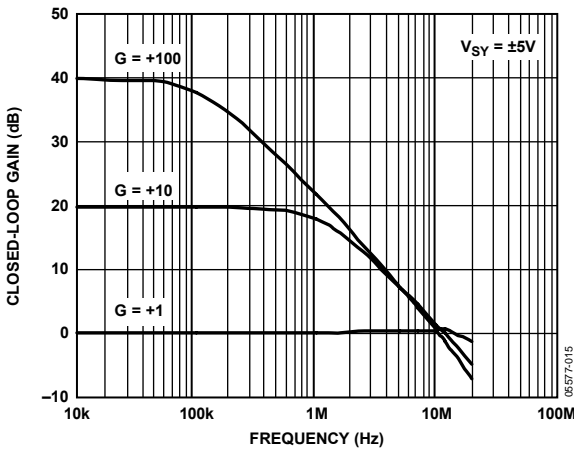


Figure 16. Closed-Loop Gain vs. Frequency

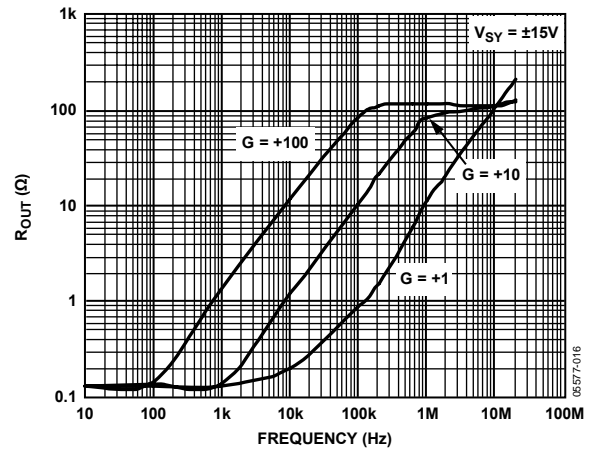


Figure 19. Output Impedance vs. Frequency

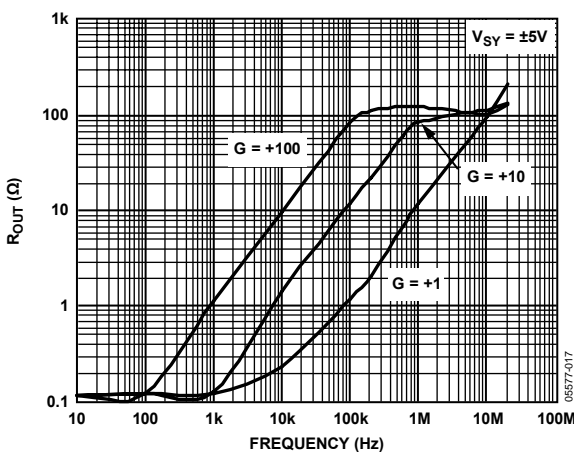


Figure 17. Output Impedance vs. Frequency

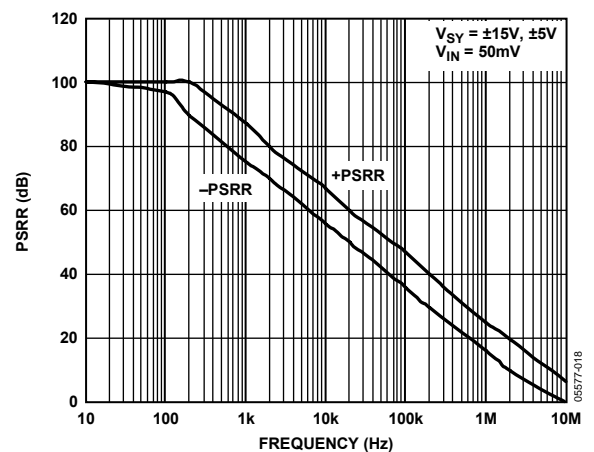


Figure 20. PSRR vs. Frequency



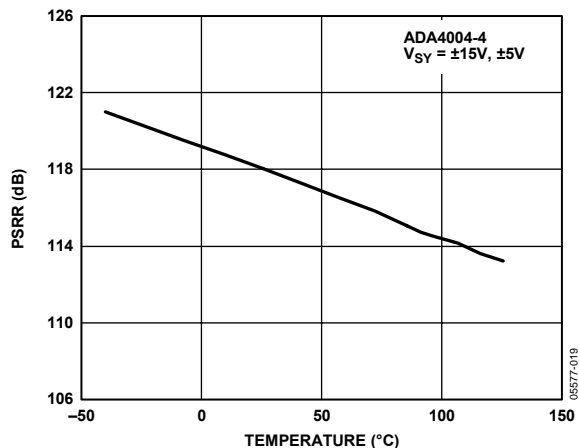


Figure 21. PSRR vs. Temperature

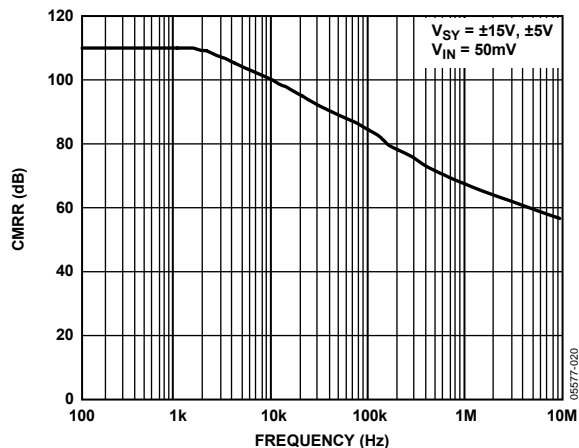


Figure 24. CMRR vs. Frequency

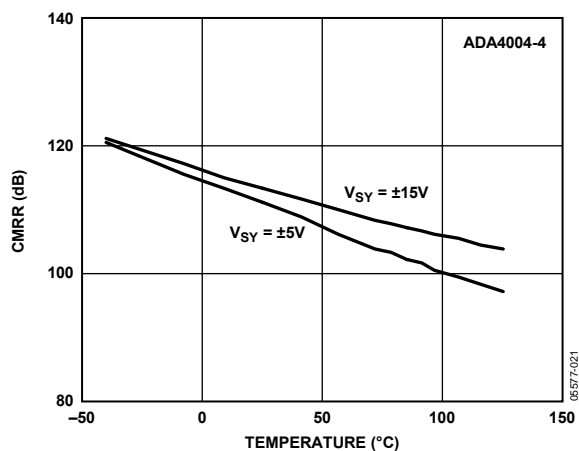


Figure 22. CMRR vs. Temperature

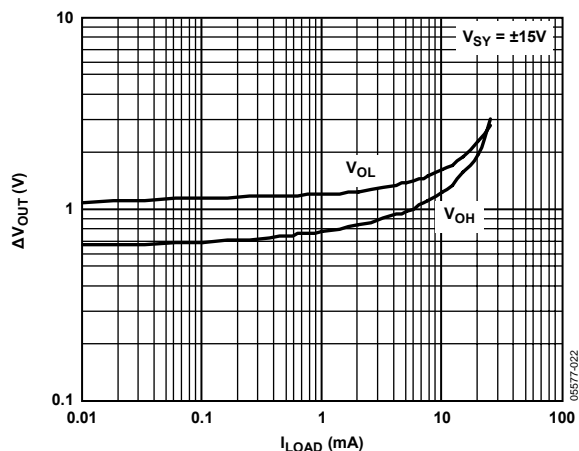


Figure 25. Output Voltage vs. Current Load

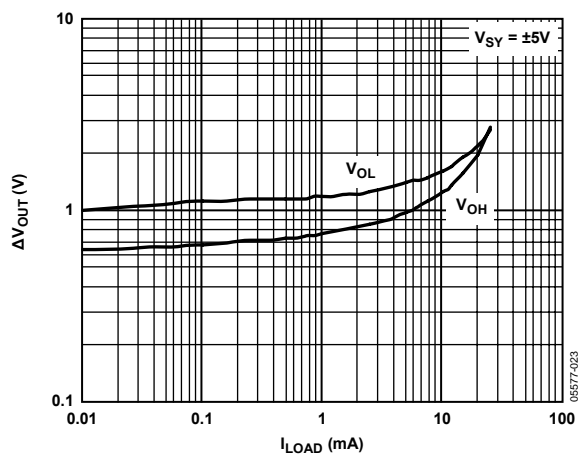


Figure 23. Output Voltage vs. Current Load

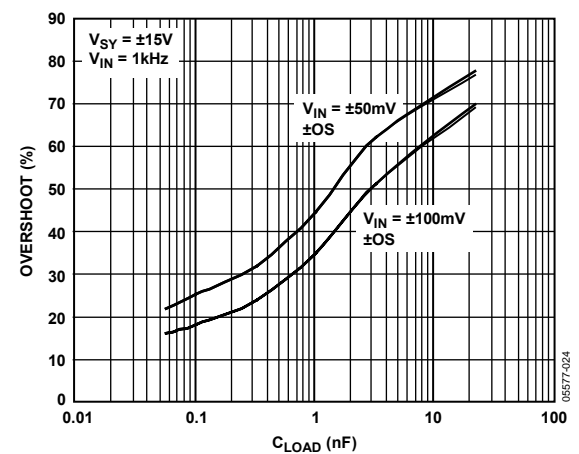


Figure 26. Small-Signal Overshoot vs. Capacitive Load

# ADA4004-4

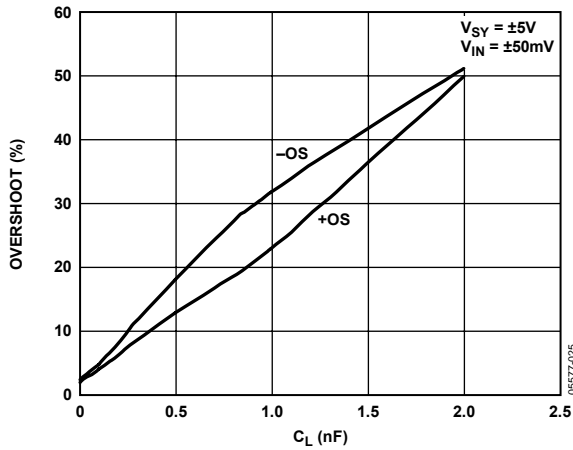


Figure 27. Small-Signal Overshoot vs. Capacitive Load

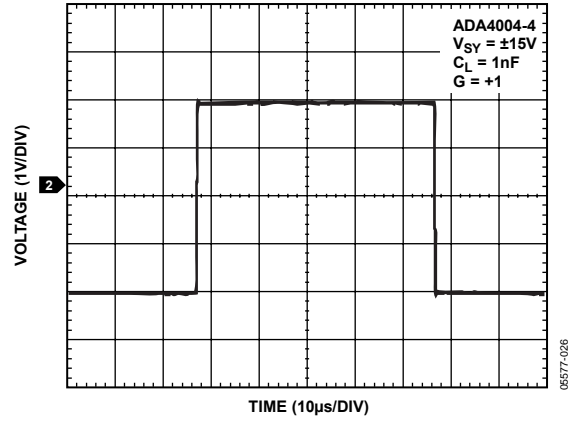


Figure 30. Large-Signal Transient Response

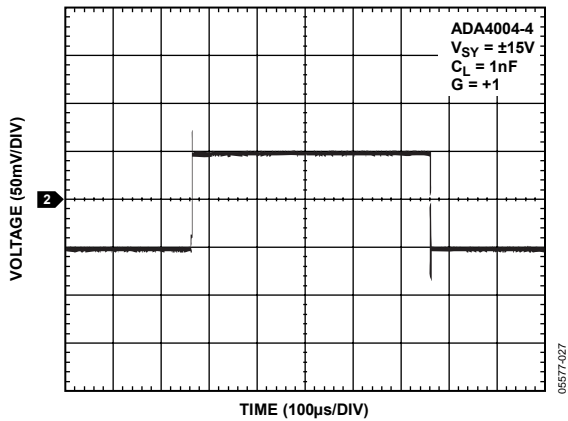


Figure 28. Small-Signal Transient Response

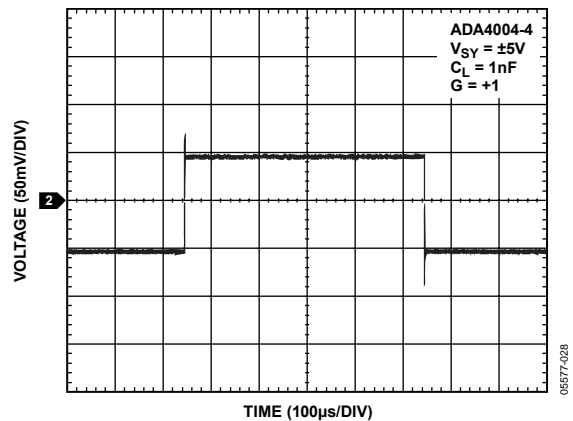


Figure 31. Small-Signal Transient Response

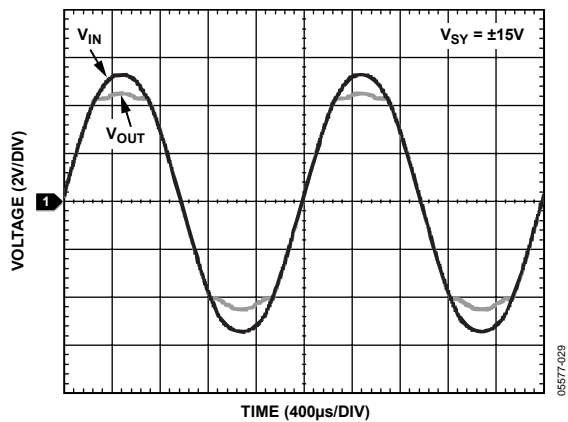


Figure 29. No Phase Reversal

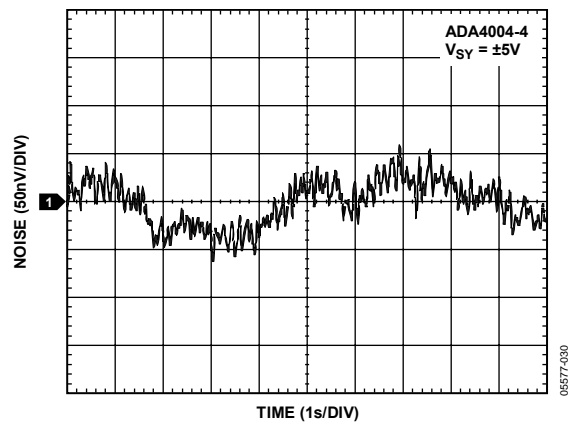


Figure 32. Voltage Noise (0.1 Hz to 10 Hz)

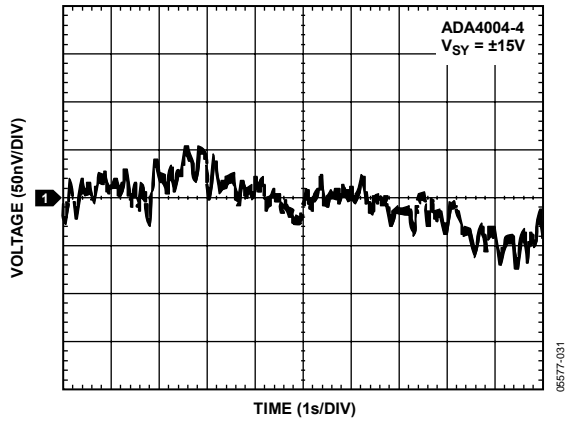


Figure 33. Voltage Noise (0.1 Hz to 10 Hz)

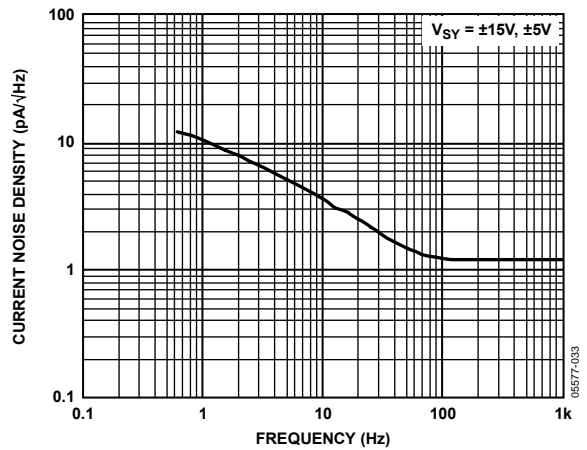


Figure 35. Current Noise Density vs. Frequency

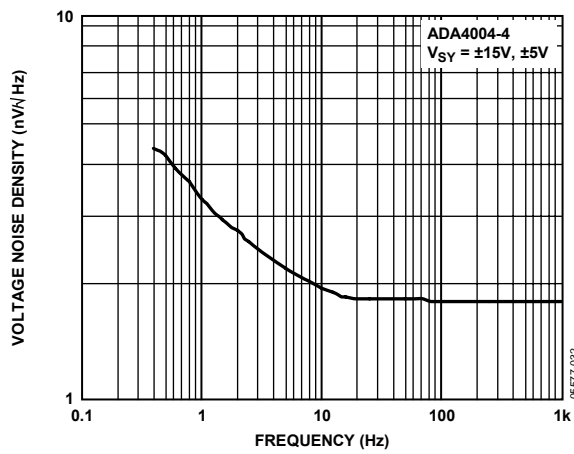


Figure 34. Voltage Noise Density vs. Frequency

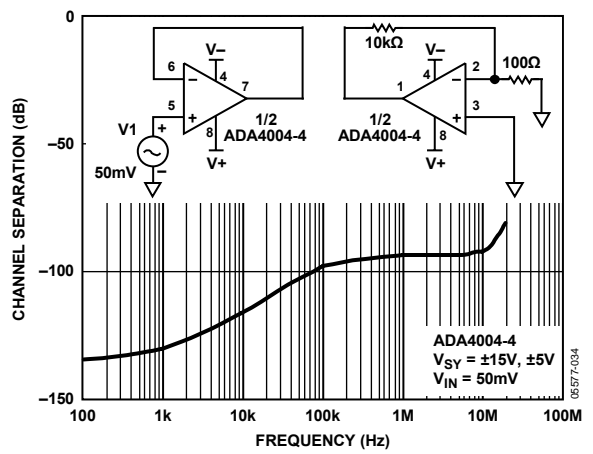
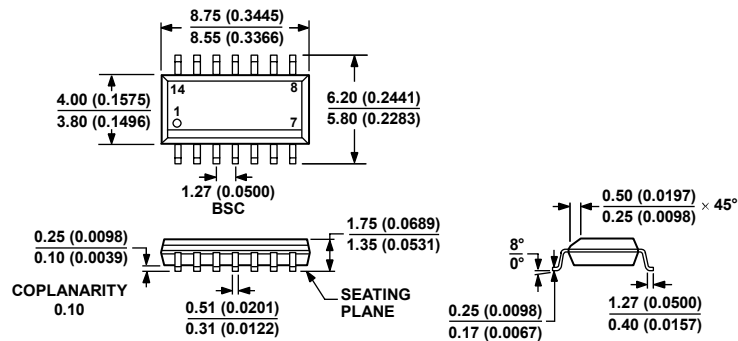


Figure 36. Channel Separation vs. Frequency

## OUTLINE DIMENSIONS

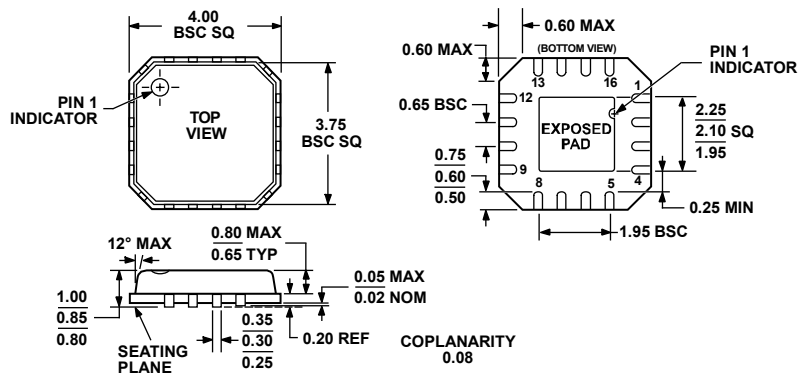


COMPLIANT TO JEDEC STANDARDS MS-012-AB  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 37. 14-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-14)

Dimensions shown in millimeters and (inches)

060606-A



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

Figure 38. 16-Lead Lead Frame Chip Scale Package [LFCSP\_VQ] 4 mm x 4 mm Body, Very Thin Quad (CP-16-4)

Dimensions shown in millimeters

031207-A

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADA4004-4ACPZ-R2 <sup>1</sup>	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4
ADA4004-4ACPZ-R7 <sup>1</sup>	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4
ADA4004-4ACPZ-RL <sup>1</sup>	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4
ADA4004-4ARZ <sup>1</sup>	-40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
ADA4004-4ARZ-R7 <sup>1</sup>	-40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
ADA4004-4ARZ-RL <sup>1</sup>	-40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14

<sup>1</sup> Z = RoHS Compliant Part.