# Unity-Gain Stable, Ultralow Distortion, 1 nV/√Hz Voltage Noise, High Speed Op Amp

# ADA4899-1

## FEATURES

**Unity-gain stable**
**Ultralow noise: 1 nV/√Hz, 2.6 pA/√Hz**
**Ultralow distortion −117 dBc at 1 MHz**
**High speed**
- **−3 dB bandwidth: 600 MHz (G = +1)**
- **Slew rate: 310 V/μs**

**Offset voltage: 230 μV maximum**
**Low input bias current: 100 nA**
**Wide supply voltage range: 5 V to 12 V**
**Supply current: 14.7 mA**
**High performance pinout**
**Disable mode**

## APPLICATIONS

**Analog-to-digital drivers**
**Instrumentation**
**Filters**
**IF and baseband amplifiers**
**DAC buffers**
**Optical electronics**

## CONNECTION DIAGRAMS

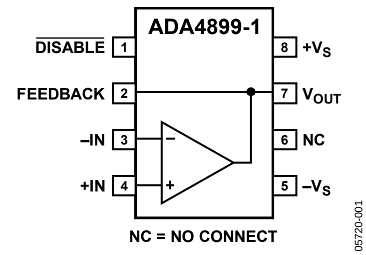


*Figure 1. 8-Lead LFCSP_VD (CP-8-2)*

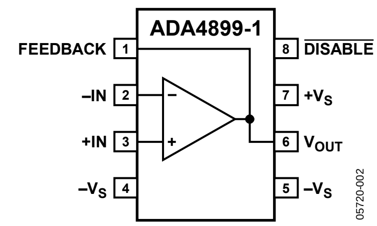


*Figure 2. 8-Lead SOIC_N_EP (RD-8-1)*

## GENERAL DESCRIPTION

The ADA4899-1 is an ultralow noise (1 nV/√Hz) and distortion (<−117 dBc @1 MHz) unity-gain stable voltage feedback op amp, the combination of which makes it ideal for 16-bit and 18-bit systems. The ADA4899-1 features a linear, low noise input stage and internal compensation that achieves high slew rates and low noise even at unity gain. The Analog Devices, Inc. proprietary next-generation XFCB process and innovative circuit design enable such high performance amplifiers.

The ADA4899-1 drives 100 Ω loads at breakthrough performance levels with only 15 mA of supply current. With the wide supply voltage range (4.5 V to 12 V), low offset voltage (230 μV maximum), wide bandwidth (600 MHz), and slew rate (310 V/μs), the ADA4899-1 is designed to work in the most demanding applications. The ADA4899-1 also features an input bias current cancellation mode that reduces input bias current by a factor of 60.

The ADA4899-1 is available in a 3 mm × 3 mm LFCSP and an 8-lead SOIC package. Both packages feature an exposed metal paddle that improves heat transfer to the ground plane, which is a significant improvement over traditional plastic packages. The ADA4899-1 is rated to work over the extended industrial temperature range, −40°C to +125°C.

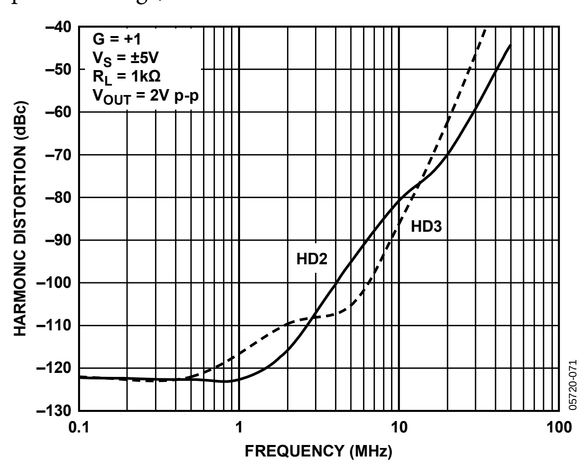


*Figure 3. Harmonic Distortion vs. Frequency*

**Rev. B**



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## REVISION HISTORY

**6/07—Rev. A to Rev. B**

Changes to Table 1 ... 3
Changes to Table 2 ... 4
Changes to Figure 21 and Figure 22 ... 8
Changes to Packaging Innovation Section ... 13
Changes to Figure 49 and Figure 50 ... 15
Updated Outline Dimensions ... 18

**4/06—Rev. 0 to Rev. A**

Changes to Figure 2 ... 1

**10/05—Revision 0: Initial Version**

# SPECIFICATIONS WITH ±5 V SUPPLY

$T_A$ = 25°C, G = +1, $R_L$ = 1 kΩ to ground, unless otherwise noted.

**Table 1.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Bandwidth | $V_{OUT}$ = 25 mV p-p | | 600 | | MHz |
| | $V_{OUT}$ = 2 V p-p | | 80 | | MHz |
| Bandwidth for 0.1 dB Flatness | G = +2, $V_{OUT}$ = 2 V p-p | | 35 | | MHz |
| Slew Rate | $V_{OUT}$ = 5 V step | | 310 | | V/µs |
| Settling Time to 0.1% | $V_{OUT}$ = 2 V step | | 50 | | ns |
| NOISE/DISTORTION PERFORMANCE | | | | | |
| Harmonic Distortion, HD2/HD3 (dBc) | $f_C$ = 500 kHz, $V_{OUT}$ = 2 V p-p | | −123/−123 | | dBc |
| | $f_C$ = 10 MHz, $V_{OUT}$ = 2 V p-p | | −80/−86 | | dBc |
| Input Voltage Noise | f = 100 kHz | | 1.0 | | nV/√Hz |
| Input Current Noise | f = 100 kHz, $\overline{\text{DISABLE}}$ pin floating | | 2.6 | | pA/√Hz |
| | f = 100 kHz, $\overline{\text{DISABLE}}$ pin = $+V_S$ | | 5.2 | | pA/√Hz |
| DC PERFORMANCE | | | | | |
| Input Offset Voltage | | | 35 | 230 | µV |
| Input Offset Voltage Drift | | | 5 | | µV/°C |
| Input Bias Current | $\overline{\text{DISABLE}}$ pin floating | | −6 | −12 | µA |
| | $\overline{\text{DISABLE}}$ pin = $+V_S$ | | −0.1 | −1 | µA |
| Input Bias Current Drift | | | 3 | | nA/°C |
| Input Bias Offset Current | | | 0.05 | 0.7 | µA |
| Open-Loop Gain | | 82 | 85 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Input Resistance | Differential mode | | 4 | | kΩ |
| | Common mode | | 7.3 | | MΩ |
| Input Capacitance | | | 4.4 | | pF |
| Input Common-Mode Voltage Range | | | −3.7 to +3.7 | | V |
| Common-Mode Rejection Ratio | | 98 | 130 | | dB |
| $\overline{\text{DISABLE}}$ PIN | | | | | |
| $\overline{\text{DISABLE}}$ Input Threshold Voltage | Output disabled | | <2.4 | | V |
| Turn-Off Time | 50% of $\overline{\text{DISABLE}}$ voltage to 10% of $V_{OUT}$, $V_{IN}$ = 0.5 V | | 100 | | ns |
| Turn-On Time | 50% of $\overline{\text{DISABLE}}$ voltage to 90% of $V_{OUT}$, $V_{IN}$ = 0.5 V | | 40 | | ns |
| Input Bias Current | $\overline{\text{DISABLE}}$ = $+V_S$ (enabled) | | 17 | 21 | µA |
| | $\overline{\text{DISABLE}}$ = $-V_S$ (disabled) | | −35 | −44 | µA |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Overdrive Recovery Time (Rise/Fall) | $V_{IN}$ = −2.5 V to +2.5 V, G = +2 | | 30/50 | | ns |
| Output Voltage Swing | $R_L$ = 1 kΩ | −3.65 to +3.65 | −3.7 to +3.7 | | V |
| | $R_L$ = 100 Ω | −3.13 to +3.15 | −3.25 to +3.25 | | V |
| Short-Circuit Current | Sinking/sourcing | | 160/200 | | mA |
| Off Isolation | f = 1 MHz, $\overline{\text{DISABLE}}$ = $-V_S$ | | −48 | | dB |
| POWER SUPPLY | | | | | |
| Operating Range | | 4.5 | | 12 | V |
| Quiescent Current | | | 14.7 | 16.2 | mA |
| Quiescent Current (Disabled) | $\overline{\text{DISABLE}}$ = $-V_S$ | | 1.8 | 2.1 | mA |
| Positive Power Supply Rejection Ratio | $+V_S$ = 4 V to 6 V (input referred) | 84 | 90 | | dB |
| Negative Power Supply Rejection Ratio | $-V_S$ = −6 V to −4 V (input referred) | 87 | 93 | | dB |

# SPECIFICATIONS WITH +5 V SUPPLY

$V_S$ = 5 V @ $T_A$ = 25°C, G = +1, $R_L$ = 1 kΩ to midsupply, unless otherwise noted.

**Table 2.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Bandwidth | $V_{OUT}$ = 25 mV p-p | | 535 | | MHz |
| | $V_{OUT}$ = 2 V p-p | | 60 | | MHz |
| Bandwidth for 0.1 dB Flatness | G = +2, $V_{OUT}$ = 2 V p-p | | 25 | | MHz |
| Slew Rate | $V_{OUT}$ = 2 V step | | 185 | | V/µs |
| Settling Time to 0.1% | $V_{OUT}$ = 2 V step | | 50 | | ns |
| NOISE/DISTORTION PERFORMANCE | | | | | |
| Harmonic Distortion, HD2/HD3 (dBc) | $f_C$ = 500 kHz, $V_{OUT}$ = 1 V p-p | | −100/−113 | | dBc |
| | $f_C$ = 10 MHz, $V_{OUT}$ = 1 V p-p | | −89/−100 | | dBc |
| Input Voltage Noise | f = 100 kHz | | 1.0 | | nV/√Hz |
| Input Current Noise | f = 100 kHz, $\overline{\text{DISABLE}}$ pin floating | | 2.6 | | pA/√Hz |
| | f = 100 kHz, $\overline{\text{DISABLE}}$ pin = $+V_S$ | | 5.2 | | pA/√Hz |
| DC PERFORMANCE | | | | | |
| Input Offset Voltage | | | 5 | 210 | µV |
| Input Offset Voltage Drift | | | 5 | | µV/°C |
| Input Bias Current | $\overline{\text{DISABLE}}$ pin floating | | −6 | −12 | µA |
| | $\overline{\text{DISABLE}}$ pin = $+V_S$ | | −0.2 | −1.5 | µA |
| Input Bias Offset Current | | | 0.05 | | µA |
| Input Bias Offset Current Drift | | | 2.5 | | nA/°C |
| Open-Loop Gain | | 76 | 80 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Input Resistance | Differential mode | | 4 | | kΩ |
| | Common mode | | 7.7 | | MΩ |
| Input Capacitance | | | 4.4 | | pF |
| Input Common-Mode Voltage Range | | | 1.3 to 3.7 | | V |
| Common-Mode Rejection Ratio | | 90 | 114 | | dB |
| $\overline{\text{DISABLE}}$ PIN | | | | | |
| $\overline{\text{DISABLE}}$ Input Threshold Voltage | Output disabled | | <2.4 | | V |
| Turn-Off Time | 50% of $\overline{\text{DISABLE}}$ voltage to 10% of $V_{OUT}$, $V_{IN}$ = 0.5 V | | 100 | | ns |
| Turn-On Time | 50% of $\overline{\text{DISABLE}}$ voltage to 90% of $V_{OUT}$, $V_{IN}$ = 0.5 V | | 60 | | ns |
| Input Bias Current | $\overline{\text{DISABLE}}$ = $+V_S$ (enabled) | | 16 | 18 | µA |
| | $\overline{\text{DISABLE}}$ = $-V_S$ (disabled) | | −33 | −42 | µA |
| OUTPUT CHARACTERISTICS | | | | | |
| Overdrive Recovery Time (Rise/Fall) | $V_{IN}$ = 0 V to 2.5 V, G = +2 | | 50/70 | | ns |
| Output Voltage Swing | $R_L$ = 1 kΩ | 1.25 to 3.75 | 1.2 to 3.8 | | V |
| | $R_L$ = 100 Ω | 1.4 to 3.6 | 1.35 to 3.65 | | V |
| Short-Circuit Current | Sinking/sourcing | | 60/80 | | mA |
| Off Isolation | f = 1 MHz, $\overline{\text{DISABLE}}$ = $-V_S$ | | −48 | | dB |
| POWER SUPPLY | | | | | |
| Operating Range | | 4.5 | | 12 | V |
| Quiescent Current | | | 14.3 | 16 | mA |
| Quiescent Current (Disabled) | $\overline{\text{DISABLE}}$ = $-V_S$ | | 1.5 | 1.7 | mA |
| Positive Power Supply Rejection Ratio | $+V_S$ = 4.5 V to 5.5 V, $-V_S$ = 0 V (input referred) | 84 | 90 | | dB |
| Negative Power Supply Rejection Ratio | $+V_S$ = 5 V, $-V_S$ = −0.5 V to +0.5 V (input referred) | 86 | 90 | | dB |

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 12.6 V |
| Power Dissipation | See Figure 4 |
| Differential Input Voltage | ±1.2 V |
| Differential Input Current | ±10 mA |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | −40°C to +125°C |
| Lead Temperature (Soldering 10 sec) | 300°C |
| Junction Temperature | 150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADA4899-1 package is limited by the associated rise in junction temperature ($T_J$) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4899-1. Exceeding a junction temperature of 150°C for an extended period can result in changes in silicon devices, potentially causing failure.

The still-air thermal properties of the package and PCB ($\theta_{JA}$), the ambient temperature ($T_A$), and the total power dissipated in the package ($P_D$) determine the junction temperature of the die. The junction temperature is calculated as

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package ($P_D$) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins ($V_S$) times the quiescent current ($I_S$). Assuming the load ($R_L$) is referenced to midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$).

The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

RMS output voltages should be considered. If $R_L$ is referenced to $V_S-$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for $R_L$ to midsupply

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with $R_L$ referenced to $V_S-$, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing $\theta_{JA}$. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the $\theta_{JA}$. Soldering the exposed paddle to the ground plane significantly reduces the overall thermal resistance of the package.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the exposed paddle (EPAD) 8-lead SOIC (70°C/W) and 8-lead LFCSP (70°C/W) packages on a JEDEC standard 4-layer board. $\theta_{JA}$ values are approximations.

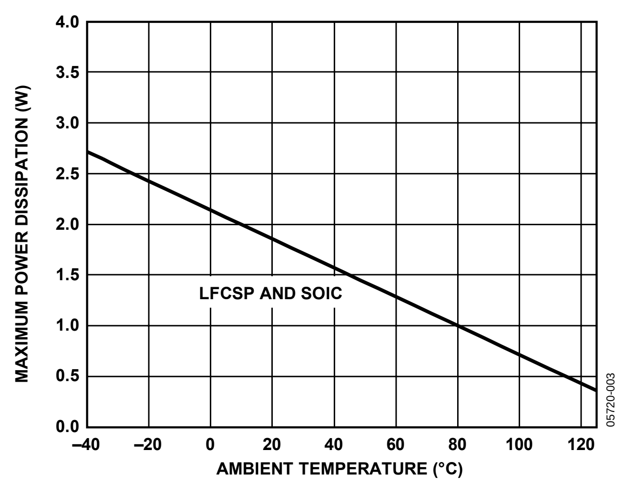
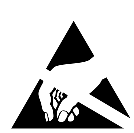



*Figure 4. Maximum Power Dissipation vs. Ambient Temperature*

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

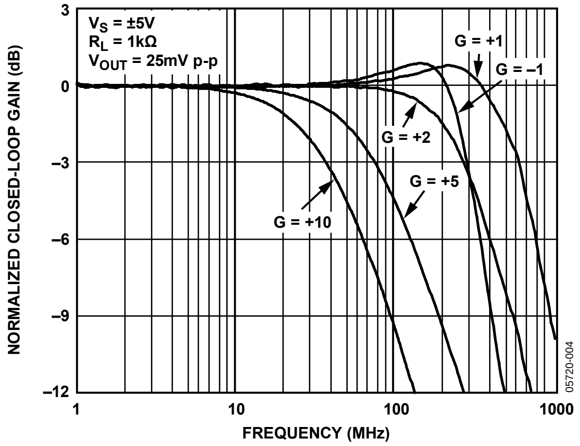



*Figure 5. Small Signal Frequency Response for Various Gains, $R_L$ = 1 kΩ*

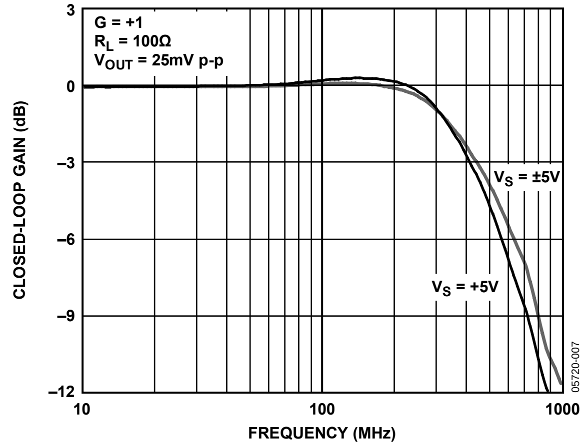



*Figure 8. Small Signal Frequency Response for Various Supply Voltages*

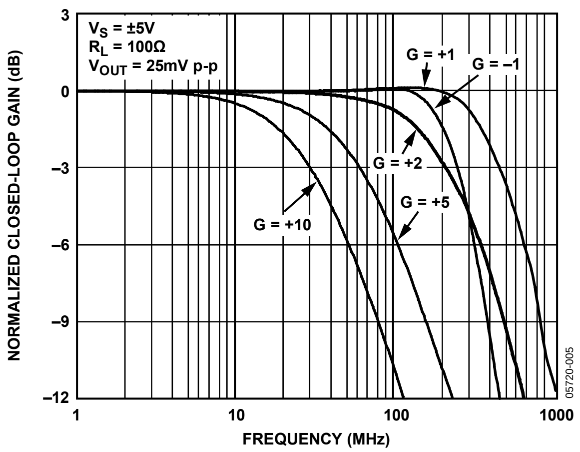



*Figure 6. Small Signal Frequency Response for Various Gains, $R_L$ = 100 Ω*

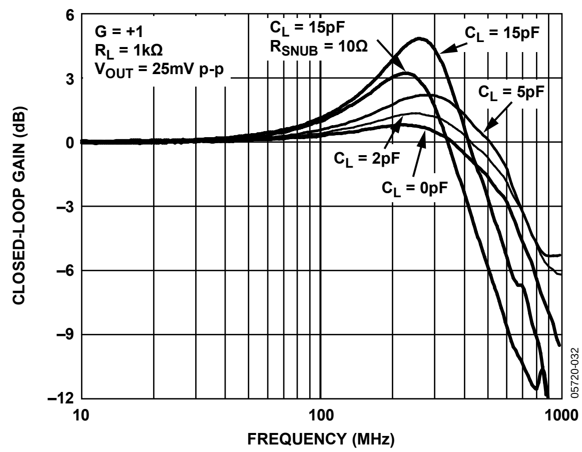



*Figure 9. Small Signal Frequency Response for Capacitive Loads*

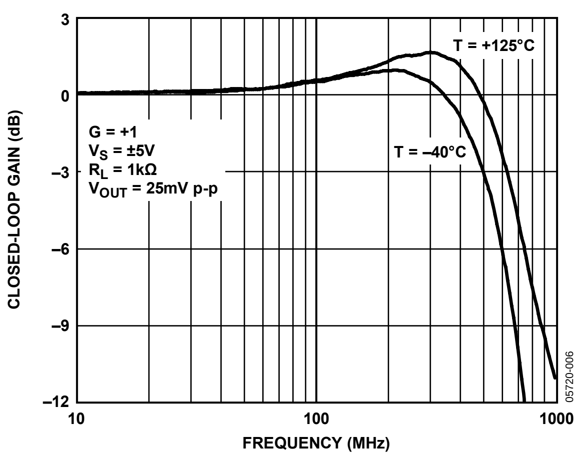



*Figure 7. Small Signal Frequency Response for Various Temperatures*

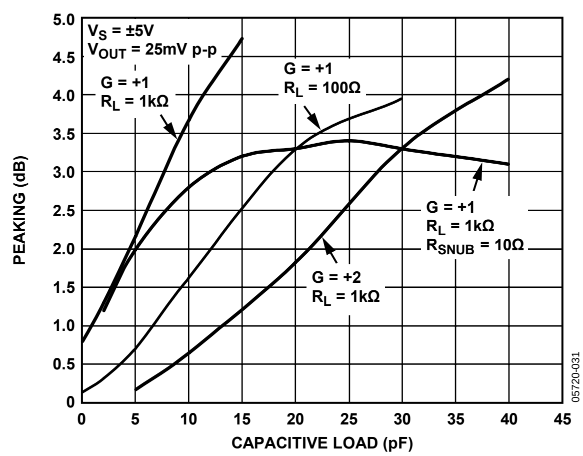



*Figure 10. Small Signal Frequency Response Peaking vs. Capacitive Load for Various Gains*

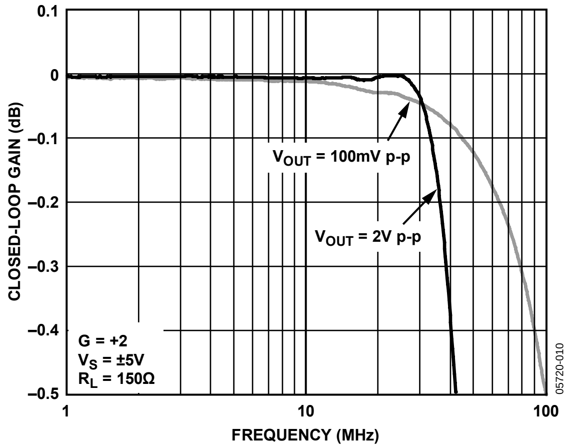



*Figure 11. 0.1 dB Flatness for Various Output Voltages*

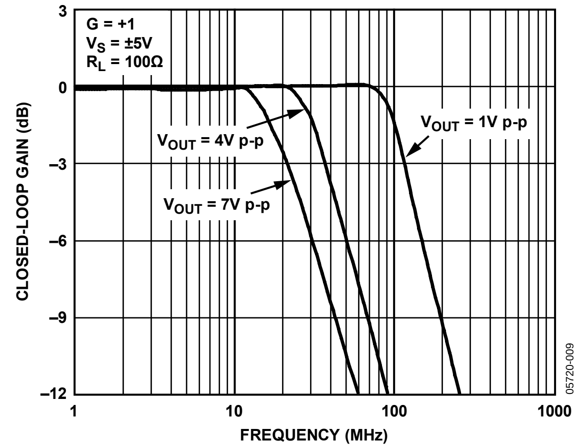



*Figure 14. Large Signal Frequency Response for Various Output Voltages*

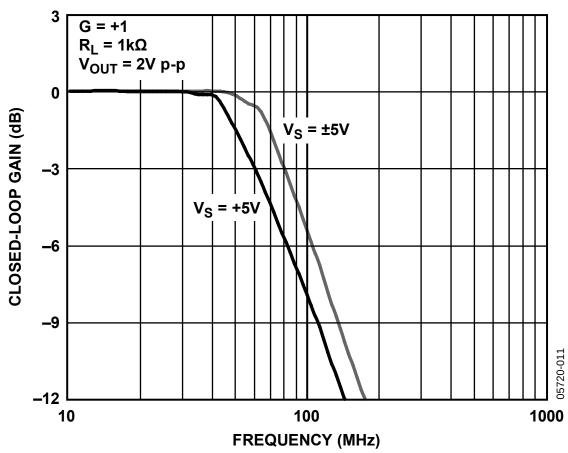



*Figure 12. Large Signal Frequency Response for Various Supply Voltages*

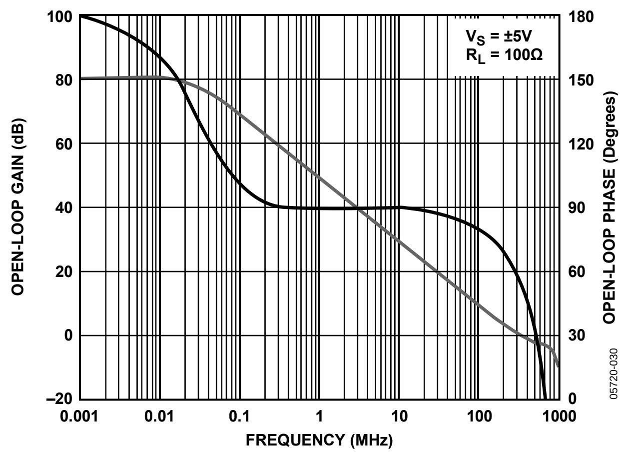



*Figure 15. Open-Loop Gain/Phase vs. Frequency*

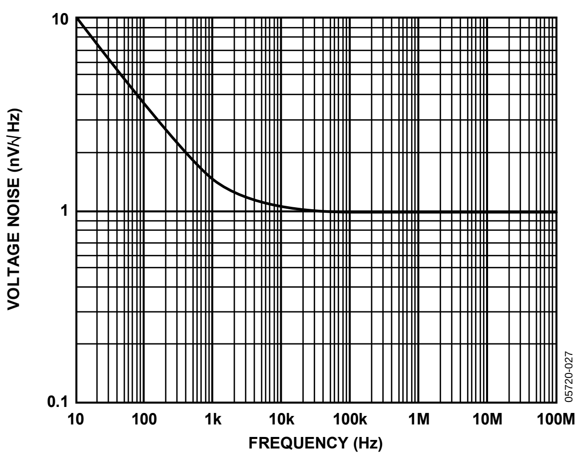



*Figure 13. Voltage Noise vs. Frequency*

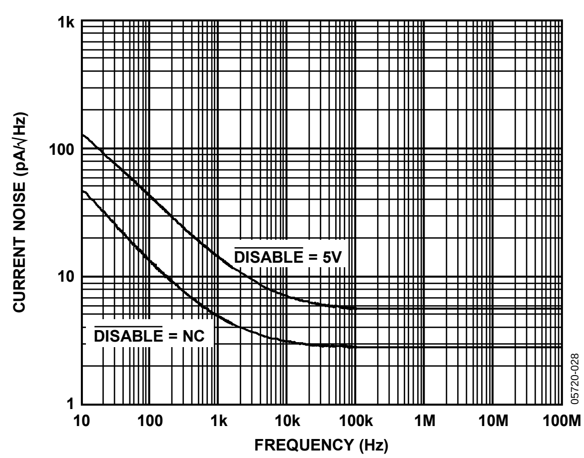



*Figure 16. Input Current Noise vs. Frequency*

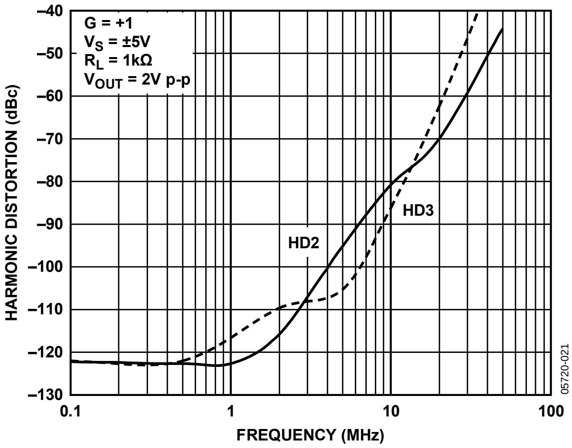



*Figure 17. Harmonic Distortion vs. Frequency*

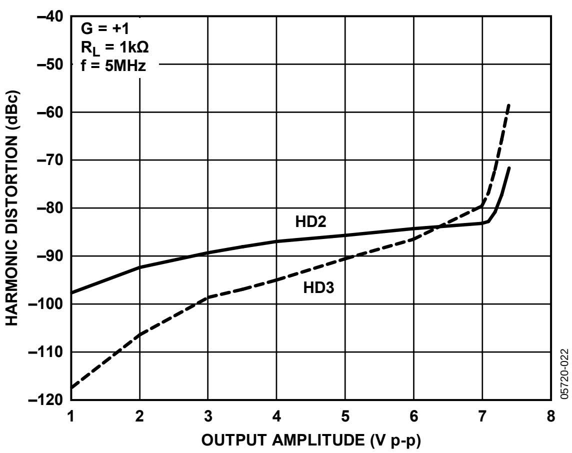



*Figure 18. Harmonic Distortion vs. Output Amplitude*

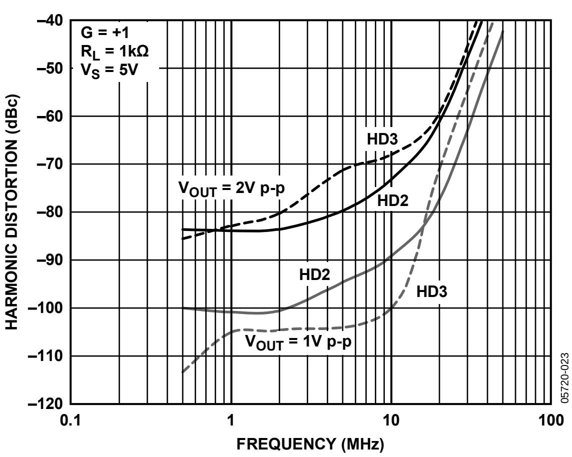



*Figure 19. Harmonic Distortion vs. Frequency*

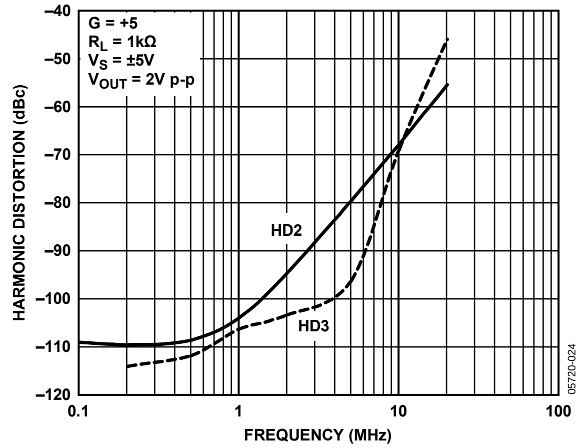



*Figure 20. Harmonic Distortion vs. Frequency*

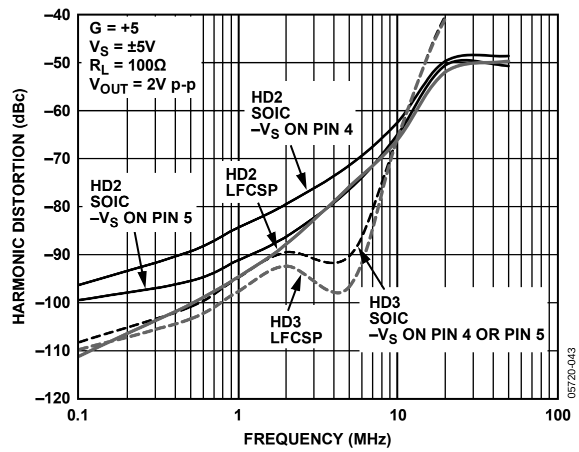



*Figure 21. Harmonic Distortion vs. Frequency for Various Pinouts and Packages*

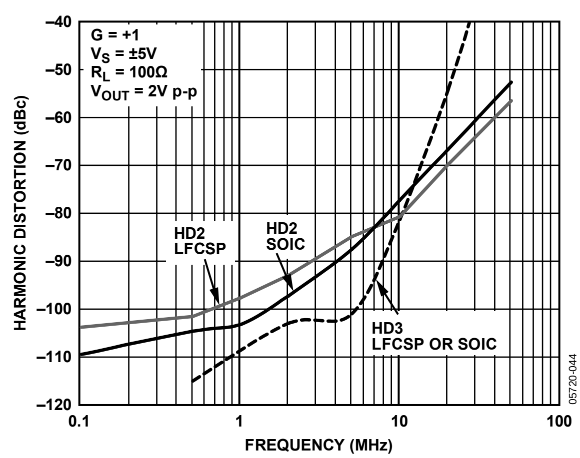



*Figure 22. Harmonic Distortion vs. Frequency for Both Packages*

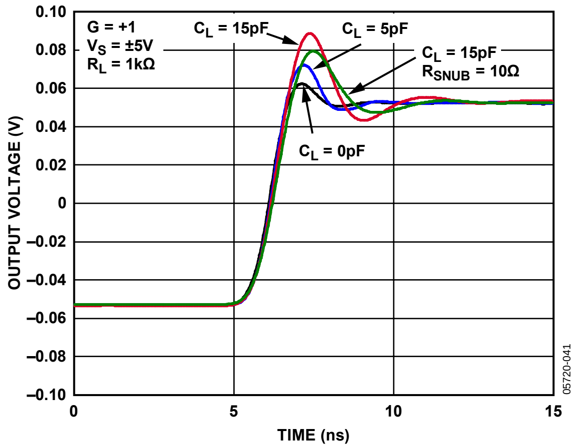



Figure 23. Small Signal Transient Response for Various Capacitive Loads (Rising Edge)

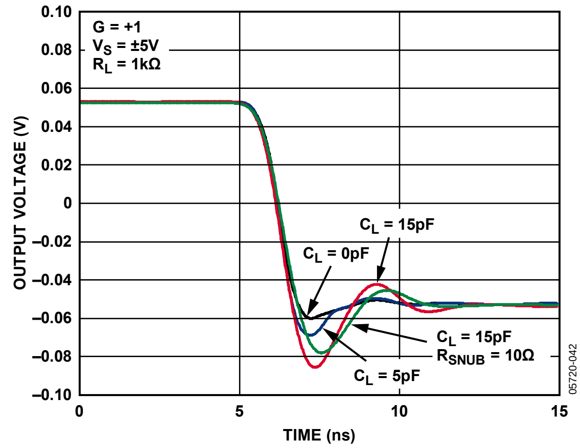



Figure 26. Small Signal Transient Response for Various Capacitive Loads (Falling Edge)

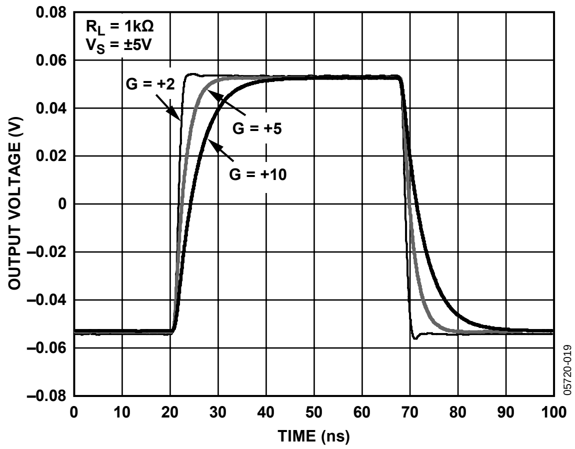



Figure 24. Small Signal Transient Response for Various Gains

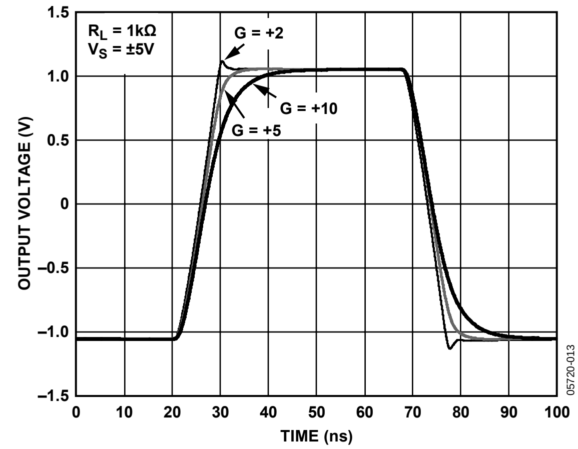



Figure 27. Large Signal Transient Response for Various Gains

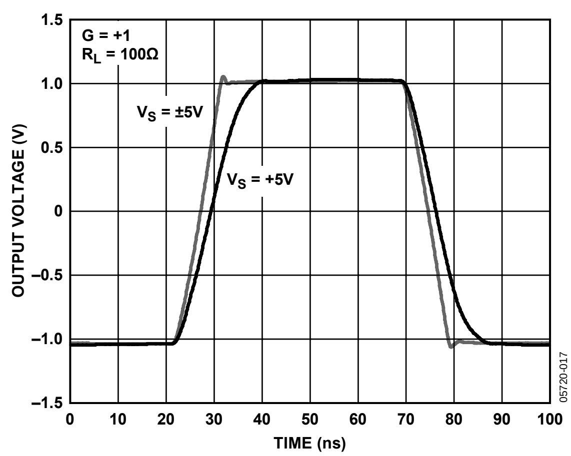



Figure 25. Large Signal Transient Response for Various Supply Voltages, $R_L = 100\ \Omega$

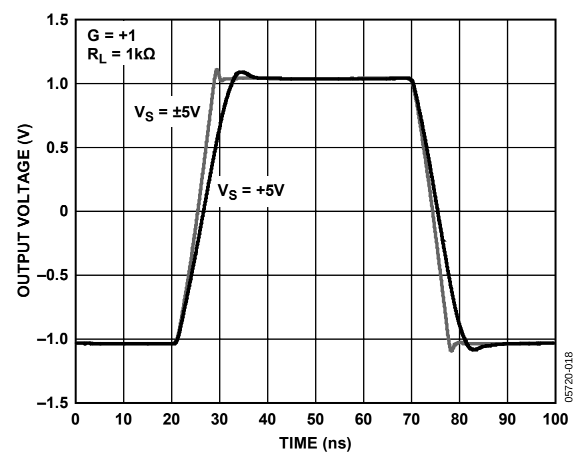



Figure 28. Large Signal Transient Response for Various Supply Voltages, $R_L = 1\ k\Omega$

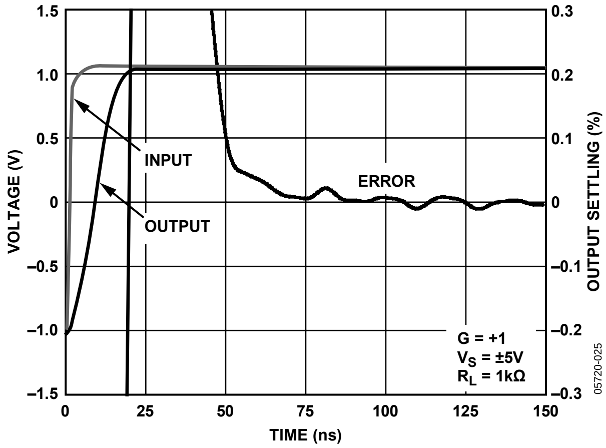



Figure 29. Settling Time, G = +1

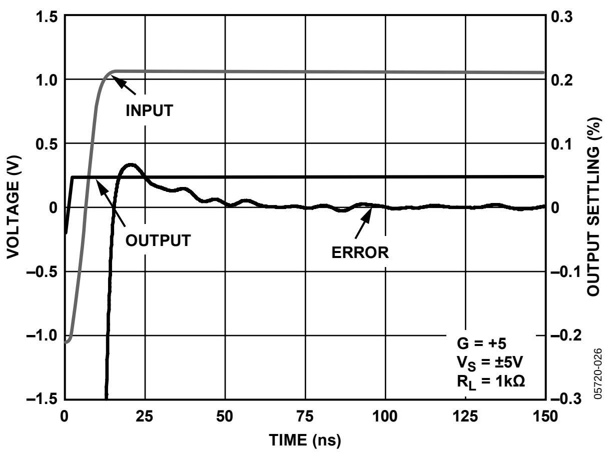



Figure 30. Settling Time, G = +5

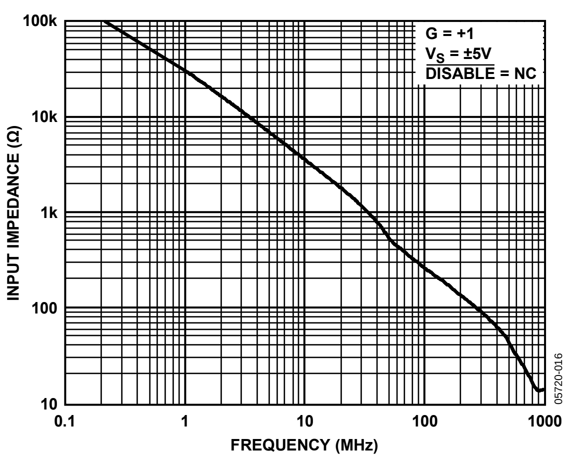



Figure 31. Input Impedance vs. Frequency

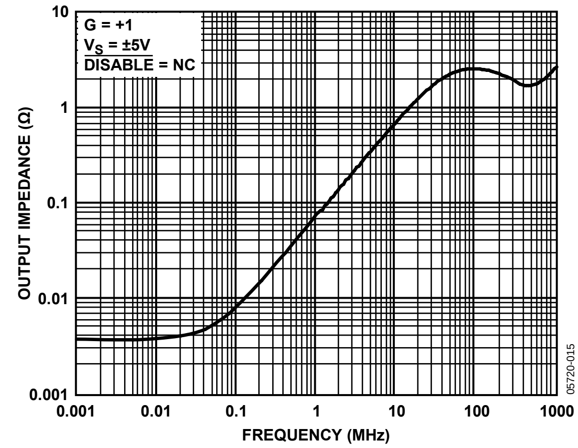



Figure 32. Output Impedance vs. Frequency

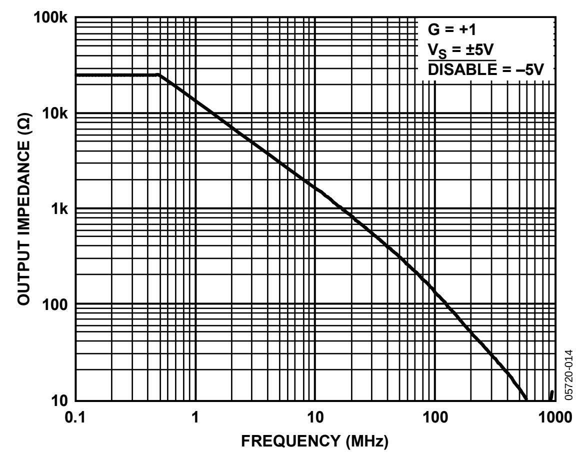



Figure 33. Output Impedance vs. Frequency (Disabled)

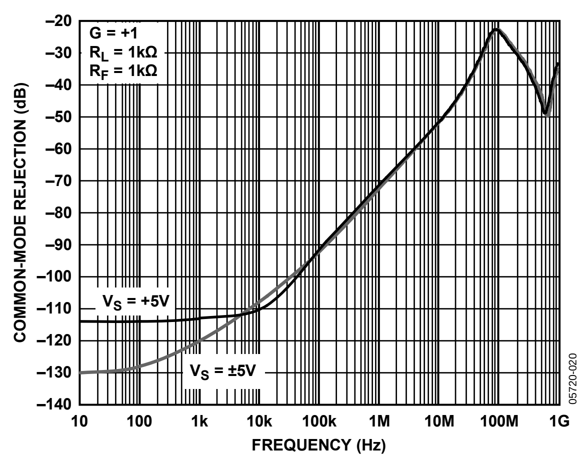



Figure 34. Common-Mode Rejection vs. Frequency

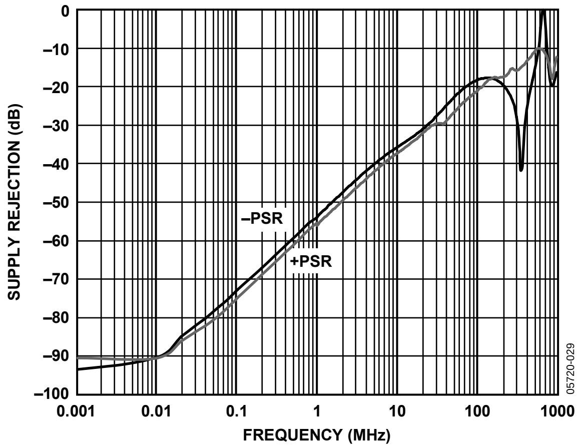



Figure 35. Power Supply Rejection

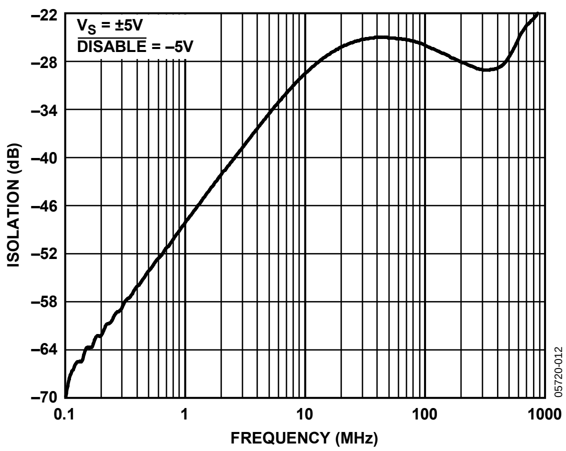



Figure 36. Off Isolation vs. Frequency

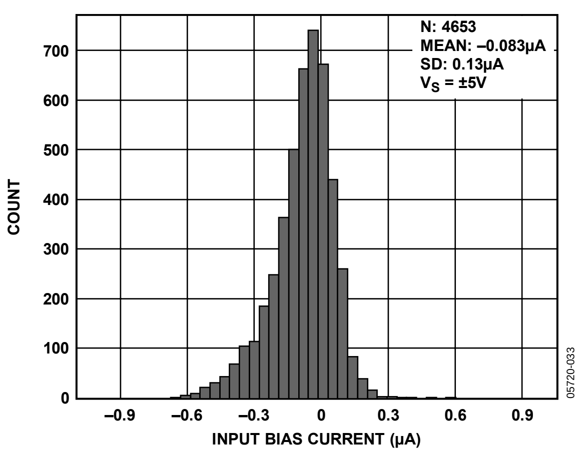



Figure 37. Input Bias Current Distribution

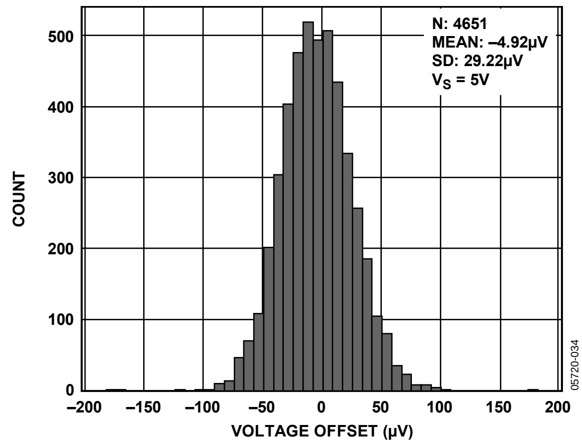



Figure 38. Input Offset Voltage Distribution ($V_S$ = 5 V)

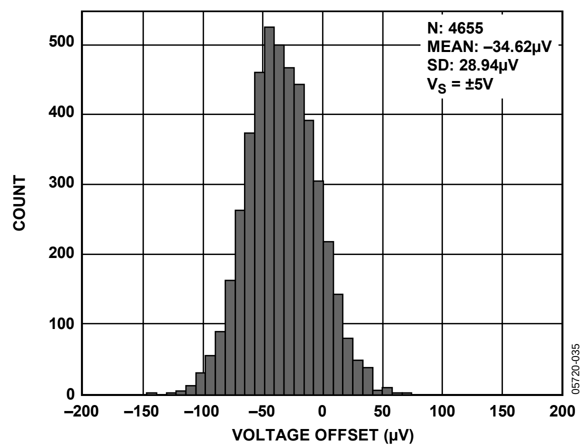



Figure 39. Input Offset Voltage Distribution ($V_S$ = ±5 V)

# TEST CIRCUITS

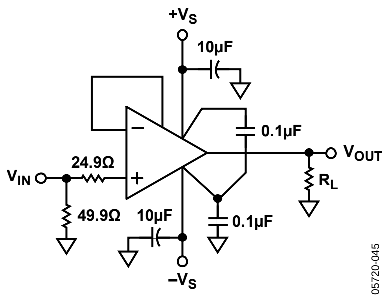



*Figure 40. Typical Noninverting Load Configuration*

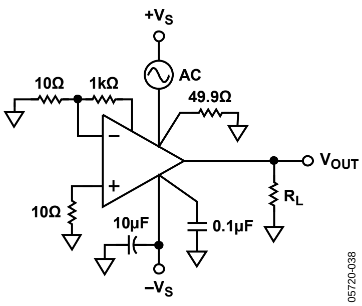



*Figure 41. Positive Power Supply Rejection*

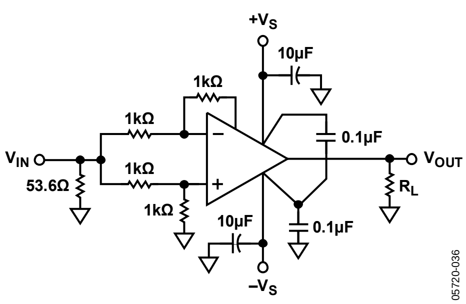



*Figure 42. Common-Mode Rejection*

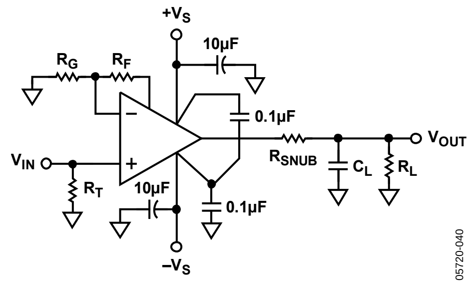



*Figure 43. Typical Capacitive Load Configuration*

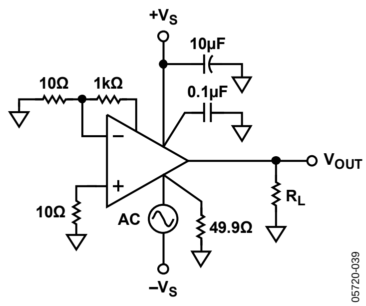



*Figure 44. Negative Power Supply Rejection*

# THEORY OF OPERATION

The ADA4899-1 is a voltage feedback op amp that combines unity-gain stability with a 1 nV/√Hz input noise. It employs a highly linear input stage that can maintain greater than −80 dBc (@ 2 V p-p) distortion out to 10 MHz while in a unity-gain configuration. This rare combination of low gain stability, input-referred noise, and extremely low distortion is the result of Analog Devices proprietary op amp architecture and high speed complementary bipolar processing technology.

The simplified ADA4899-1 topology, shown in Figure 45, is a single gain stage with a unity-gain output buffer. It has over 80 dB of open-loop gain and maintains precision specifications such as CMRR, PSRR, and offset to levels that are normally associated with topologies having two or more gain stages.

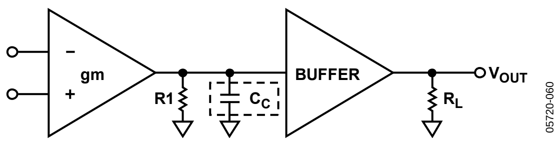



*Figure 45. ADA4899-1 Topology*

A pair of internally connected diodes limits the differential voltage between the noninverting input and the inverting input of the ADA4899-1. Each set of diodes has two series diodes connected in antiparallel, which limits the differential voltage between the inputs to approximately ±1.2 V. All of the ADA4899-1 pins are ESD protected with voltage-limiting diodes connected between both rails. The protection diodes can handle 10 mA. Currents should be limited through these diodes to 10 mA or less by using a series limiting resistor.

## PACKAGING INNOVATION

The ADA4899-1 is available in both a SOIC and an LFCSP, each of which has a thermal pad that allows the device to run cooler, thereby increasing reliability. To help avoid routing around the pad when laying out the board, both packages have a dedicated feedback pin on the opposite side of the package for ease in connecting the feedback network to the inverting input. The secondary output pin also isolates the interaction of any capacitive load on the output and the self-inductance of the package and bond wire from the feedback loop. When using the dedicated feedback pin, inductance in the primary output helps to isolate capacitive loads from the output impedance of the amplifier.

Both the SOIC and LFCSP have modified pinouts to improve heavy load second harmonic distortion performance. The intent of both is to isolate the negative supply pin from the noninverting input. The LFCSP accomplishes this by rotating the standard 8-lead package pinout counterclockwise by one pin, which puts the supply and output pins on the right side of the package and the input pins on the left side of the package. The SOIC is slightly different with the intent of both isolating the inputs from the supply pins and giving the user the option of using the ADA4899-1 in a standard SOIC board layout with little or no modification. Taking the unused Pin 5 and making it a second negative supply pin allows for both an input isolated layout and a traditional layout to be supported.

## $\overline{\text{DISABLE}}$ PIN

A three-state input pin is provided on the ADA4899-1 for a high impedance disable and an optional input bias current cancellation circuit. The high impedance output allows several ADA4899-1s to drive the same ADC or output line time interleaved. Pulling the $\overline{\text{DISABLE}}$ pin low activates the high impedance state (see Table 7 for threshold levels). When the $\overline{\text{DISABLE}}$ pin is left floating (open), the ADA4899-1 operates normally. With the $\overline{\text{DISABLE}}$ pin pulled within 0.7 V of the positive supply, an optional input bias current cancellation circuit is turned on, which lowers the input bias current to less than 200 nA. In this mode, the user can drive the ADA4899-1 from a high dc source impedance and still maintain minimal output-referred offset without having to use impedance matching techniques. In addition, the ADA4899-1 can be ac-coupled while setting the bias point on the input with a high dc impedance network. The input bias current cancellation circuit doubles the input-referred current noise, but this effect is minimal as long as the wideband impedances are kept low (see Figure 16).

# APPLICATIONS

## UNITY-GAIN OPERATION

The ADA4899-1 schematic for unity-gain configuration is nearly a textbook example (see Figure 46). The only exception is the small 24.9 Ω series resistor at the noninverting input. The series resistor is only required in unity-gain configurations; higher gains negate the need for the resistor. In Table 4, it can be seen that the overall noise contribution of the amplifier and the 24.9 Ω resistor is equivalent to the noise of a single 87 Ω resistor.

Figure 47 shows the small signal frequency response for the unity-gain amplifier shown in Figure 46.

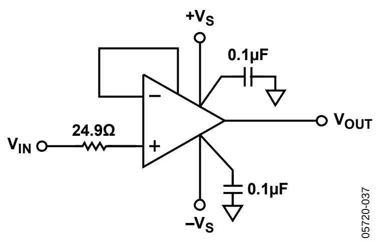



*Figure 46. Unity-Gain Schematic*

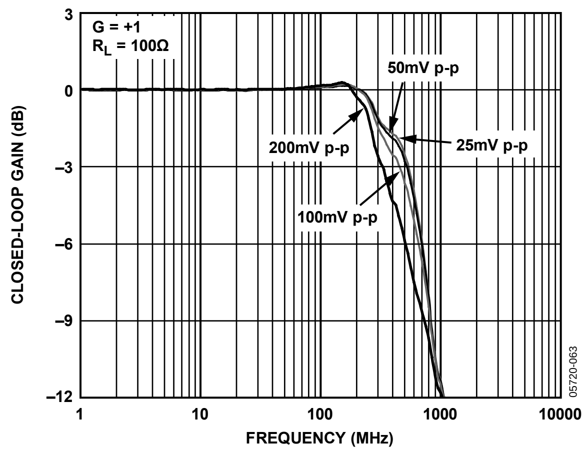



*Figure 47. Small Signal Frequency Response for Various Output Voltages*

## RECOMMENDED VALUES FOR VARIOUS GAINS

Table 4 provides a handy reference for determining various gains and associated performance. For noise gains greater than one, the Series Resistor $R_S$ is not required. Resistors $R_F$ and $R_G$ are kept low to minimize their contribution to the overall noise performance of the amplifier.

**Table 4. Conditions: $V_S$ = ±5 V, $T_A$ = 25°C, $R_L$ = 1 kΩ**

| Gain | $R_F$ (Ω) | $R_G$ (Ω) | $R_S$ (Ω) | −3 dB SS BW (MHz) (25 mV p-p) | Slew Rate (V/µs) (2 V Step) | ADA4899-1 Voltage Noise (nV/√Hz) | Total Voltage Noise (nV/√Hz) |
|---|---|---|---|---|---|---|---|
| +1 | 0 | NA | 24.9 | 605 | 274 | 1 | 1.2 |
| −1 | 100 | 100 | 0 | 294 | 265 | 2 | 2.7 |
| +2 | 100 | 100 | 0 | 277 | 253 | 2 | 2.7 |
| +5 | 200 | 49.9 | 0 | 77 | 227 | 5 | 6.5 |
| +10 | 453 | 49.9 | 0 | 37 | 161 | 10 | 13.3 |

## NOISE

To analyze the noise performance of an amplifier circuit, first identify the noise sources, then determine if the source has a significant contribution to the overall noise performance of the amplifier. To simplify the noise calculations, noise spectral densities were used, rather than actual voltages to leave bandwidth out of the expressions (noise spectral density, which is generally expressed in nV/√Hz, is equivalent to the noise in a 1 Hz bandwidth).

The noise model shown in Figure 48 has six individual noise sources: the Johnson noise of the three resistors, the op amp voltage noise, and the current noise in each input of the amplifier. Each noise source has its own contribution to the noise at the output. Noise is generally specified referred to input (RTI), but it is often simpler to calculate the noise referred to the output (RTO) and then divide by the noise gain to obtain the RTI noise.

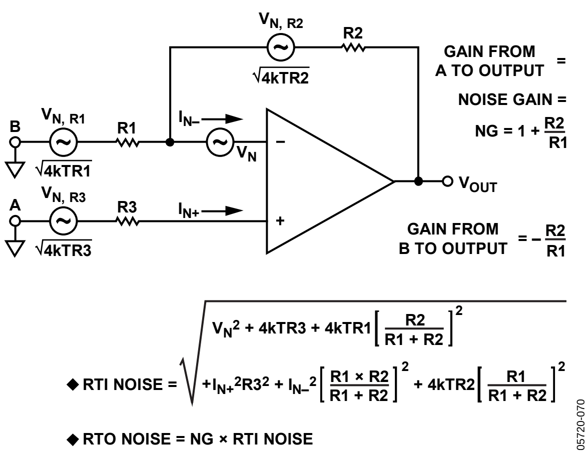



*Figure 48. Op Amp Noise Analysis Model*

All resistors have a Johnson noise that is calculated by

$$\sqrt{(4kBTR)}$$

where:
$k$ is Boltzmann's Constant ($1.38 \times 10^{-23}$ J/K).
$B$ is the bandwidth in Hz.
$T$ is the absolute temperature in Kelvin.
$R$ is the resistance in ohms.

A simple relationship that is easy to remember is that a 50 Ω resistor generates a Johnson noise of 1 nV√Hz at 25°C.

In applications where noise sensitivity is critical, care must be taken not to introduce other significant noise sources to the amplifier. Each resistor is a noise source. Attention to the following areas is critical to maintain low noise performance: design, layout, and component selection. A summary of noise performance for the amplifier and associated resistors can be seen in Table 4.

## ADC DRIVER

The ultralow noise and distortion performance of the ADA4899-1 makes it an excellent candidate for driving 16-bit ADCs. The schematic for a single-ended input buffer using the ADA4899-1 and the AD7677, a 1 MSPS, 16-bit ADC, is shown in Figure 49. Table 5 shows the performance data of the ADA4899-1 and the AD7677.

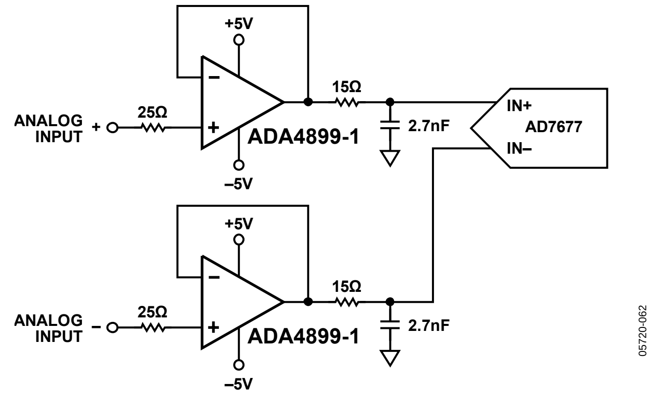



*Figure 49. Single-Ended Input ADC Driver*

**Table 5. ADA4899-1, Single-Ended Driver for AD7677 16-Bit, 1 MSPS, $f_C$ = 50 kHz**

| Parameter | Measurement (dB) |
|---|---|
| Second Harmonic Distortion | −116.5 |
| Third Harmonic Distortion | −111.9 |
| THD | −108.6 |
| SFDR | +101.4 |
| SNR | +92.6 |

The ADA4899-1 configured as a single-ended-to-differential driver for the AD7677 is shown in Figure 50. Table 6 shows the associated performance.

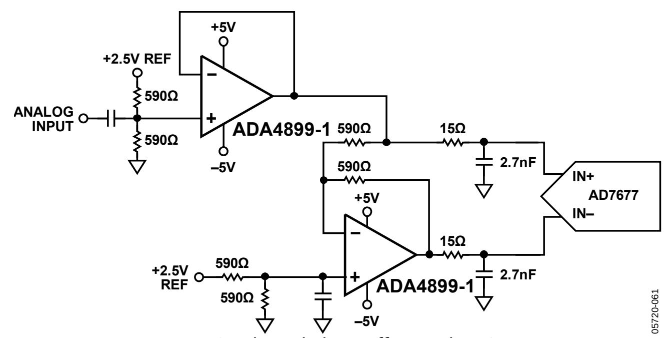



*Figure 50. Single-Ended-to-Differential ADC Driver*

**Table 6. ADA4899-1, Single Ended-to-Differential Driver for AD7677 16-Bit, 1 MSPS, $f_C$ = 500 kHz**

| Parameter | Measurement (dB) |
|---|---|
| THD | −92.7 |
| SFDR | +91.8 |
| SNR | +90.6 |

## DISABLE PIN OPERATION

The ADA4899-1 $\overline{\text{DISABLE}}$ pin performs three functions: enable, disable, and reduction of the input bias current. When the $\overline{\text{DISABLE}}$ pin is brought to within 0.7 V of the positive supply, the input bias current circuit is enabled, which reduces the input bias current by a factor of 100. In this state, the input current noise doubles from 2.6 pA/√Hz to 5.2 pA/√Hz. Table 7 outlines the $\overline{\text{DISABLE}}$ pin operation.

**Table 7. $\overline{\text{DISABLE}}$ Pin Truth Table**

| Supply Voltage | ±5 V | +5 V |
|---|---|---|
| Disable | −5 V to +2.4 V | 0 V to 2.4 V |
| Enable | Open | Open |
| Low Input Bias Current | 4.3 V to 5 V | 4.3 V to 5 V |

## ADA4899-1 MUX

With a true output disable, the ADA4899-1 can be used in multiplexer applications. The outputs of two ADA4899-1s are wired together to form a 2:1 mux. Figure 51 shows the 2:1 mux schematic.

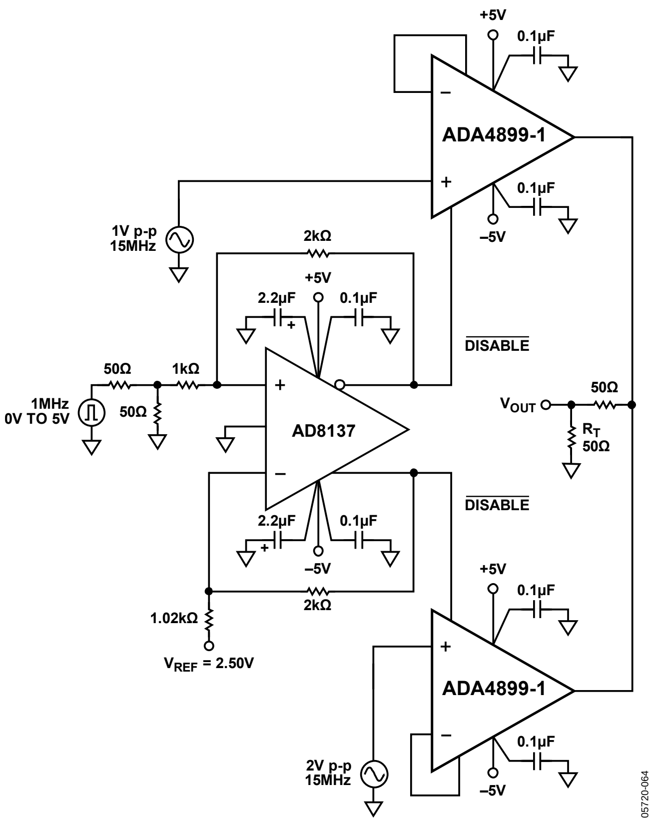



*Figure 51. ADA4899-1 2:1 Mux Schematic*

An AD8137 differential amplifier is used as a level translator that converts the TTL input to a complementary ±3 V output to drive the $\overline{\text{DISABLE}}$ pins of the ADA4899-1s. The transient response for the 2:1 mux is shown in Figure 52.

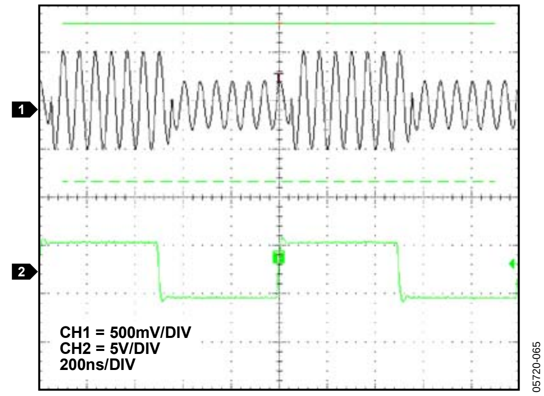



*Figure 52. ADA4899-1 2:1 Mux Transient Response*

## CIRCUIT CONSIDERATIONS

Careful and deliberate attention to detail when laying out the ADA4899-1 board yields optimal performance. Power supply bypassing, parasitic capacitance, and component selection all contribute to the overall performance of the amplifier.

### *PCB Layout*

Because the ADA4899-1 can operate up to 600 MHz, it is essential that RF board layout techniques be employed. All ground and power planes under the pins of the ADA4899-1 should be cleared of copper to prevent the formation of parasitic capacitance between the input pins to ground and the output pins to ground. A single mounting pad on a SOIC footprint can add as much as 0.2 pF of capacitance to ground if the ground plane is not cleared from under the mounting pads. The low distortion pinout of the ADA4899-1 reduces the distance between the output and the inverting input of the amplifier. This helps minimize the parasitic inductance and capacitance of the feedback path, which reduces ringing and second harmonic distortion.

### *Power Supply Bypassing*

Power supply bypassing for the ADA4899-1 has been optimized for frequency response and distortion performance. Figure 40 shows the recommended values and location of the bypass capacitors. Power supply bypassing is critical for stability, frequency response, distortion, and PSR performance. The 0.1 µF capacitors shown in Figure 40 should be as close to the supply pins of the ADA4899-1 as possible. The electrolytic capacitors should be directly adjacent to the 0.1 µF capacitors. The capacitor between the two supplies helps improve PSR and distortion performance. In some cases, additional paralleled capacitors can help improve frequency and transient response.

### *Grounding*

Ground and power planes should be used where possible. Ground and power planes reduce the resistance and inductance of the power planes and ground returns. The returns for the input, output terminations, bypass capacitors, and $R_G$ should all be kept as close to the ADA4899-1 as possible. The output load ground and the bypass capacitor grounds should be returned to the same point on the ground plane to minimize parasitic trace inductance, ringing, and overshoot and to improve distortion performance.

The ADA4899-1 packages feature an exposed paddle. For optimum electrical and thermal performance, solder this paddle to ground. For more information on high speed circuit design, see *A Practical Guide to High-Speed Printed-Circuit-Board Layout*.

# OUTLINE DIMENSIONS

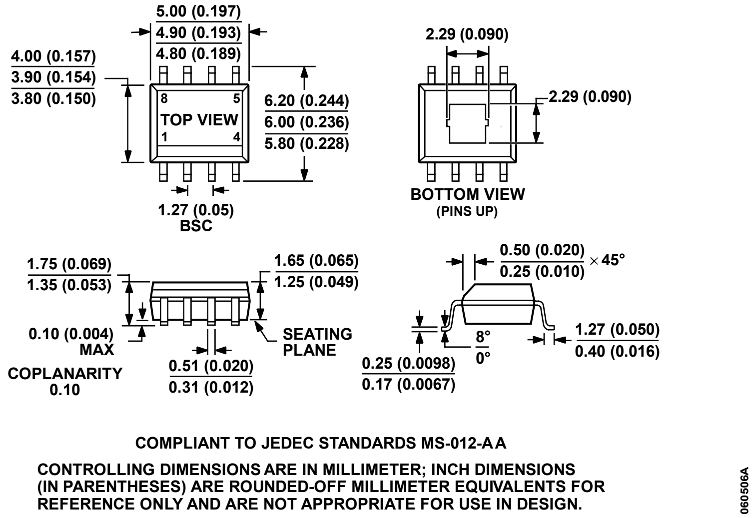



*Figure 53. 8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]*
*(RD-8-1)*
*Dimensions shown in millimeters and (inches)*

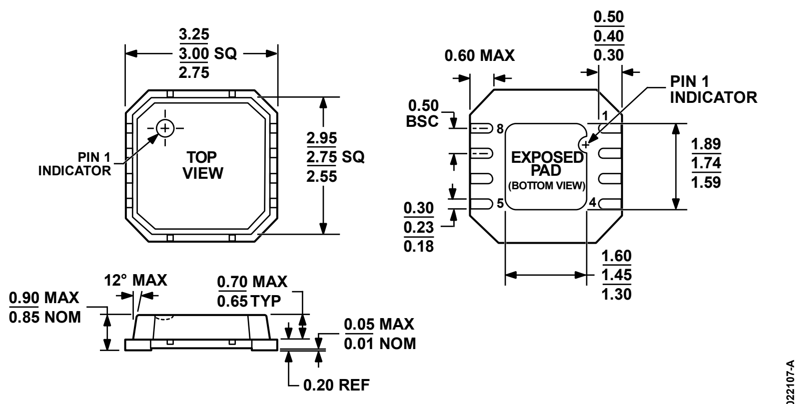



*Figure 54. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]*
*3 mm × 3 mm Body, Very Thin, Dual Lead*
*(CP-8-2)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding | Ordering Quantity |
|---|---|---|---|---|---|
| ADA4899-1YRDZ[1] | −40°C to +125°C | 8-Lead SOIC_N_EP | RD-8-1 | | 1 |
| ADA4899-1YRDZ-R7[1] | −40°C to +125°C | 8-Lead SOIC_N_EP | RD-8-1 | | 1,000 |
| ADA4899-1YRDZ-RL[1] | −40°C to +125°C | 8-Lead SOIC_N_EP | RD-8-1 | | 2,500 |
| ADA4899-1YCPZ-R2[1] | −40°C to +125°C | 8-Lead LFCSP_VD | CP-8-2 | | 250 |
| ADA4899-1YCPZ-R7[1] | −40°C to +125°C | 8-Lead LFCSP_VD | CP-8-2 | HBC | 1,500 |
| ADA4899-1YCPZ-RL[1] | −40°C to +125°C | 8-Lead LFCSP_VD | CP-8-2 | HBC | 5,000 |

[1] Z = RoHS Compliant Part.

# NOTES

## NOTES