



80C196EA CHMOS 16-BIT MICROCONTROLLER

Commercial

Preliminary Datasheet

Product Features

- 40 MHz Operation
- Optional Clock Doubler
- 2 Mbytes of Linear Address Space
- 1 Kbyte of Register RAM
- 3 Kbytes of Code RAM
- Register-Register Architecture
- Stack overflow/underflow monitor with user-defined upper and lower stack pointer boundary limits
- 2 peripheral interrupt handlers (PIH) provide direct hardware handling of up to 16 peripheral interrupts
- Peripheral transaction server (PTS) with high-speed, microcoded interrupt service routines
- Up to 83 I/O port pins
- 2 full-duplex serial ports with dedicated baud-rate generators
- Enhanced synchronous serial unit
- 8 pulse-width modulator (PWM) outputs with 8-bit resolution
- 16-bit watchdog timer
- Sixteen 10-bit A/D channels with auto-scan mode and dedicated results registers
- Serial debug unit provides read and write access to code RAM with no CPU overhead
- Chip-select unit (CSU)
- 3 chip-select pins
- Dynamic demultiplexed/multiplexed address/data bus for each chip-select
- Programmable wait states (0, 1, 2, or 3) for each chip-select
- Programmable bus width (8- or 16-bit) for each chip-select
- Programmable address range for each chip-select
- Event processor array (EPA)
- 4 flexible 16-bit timer/counters
- 17 high-speed capture/compare channels
- 8 output-only channels capture value of any other timer upon compare, providing easy conversion between angle and time domains
- Programmable clock output signal
- 160-pin QFP package
- Complete system development support
- High-speed CHMOS technology

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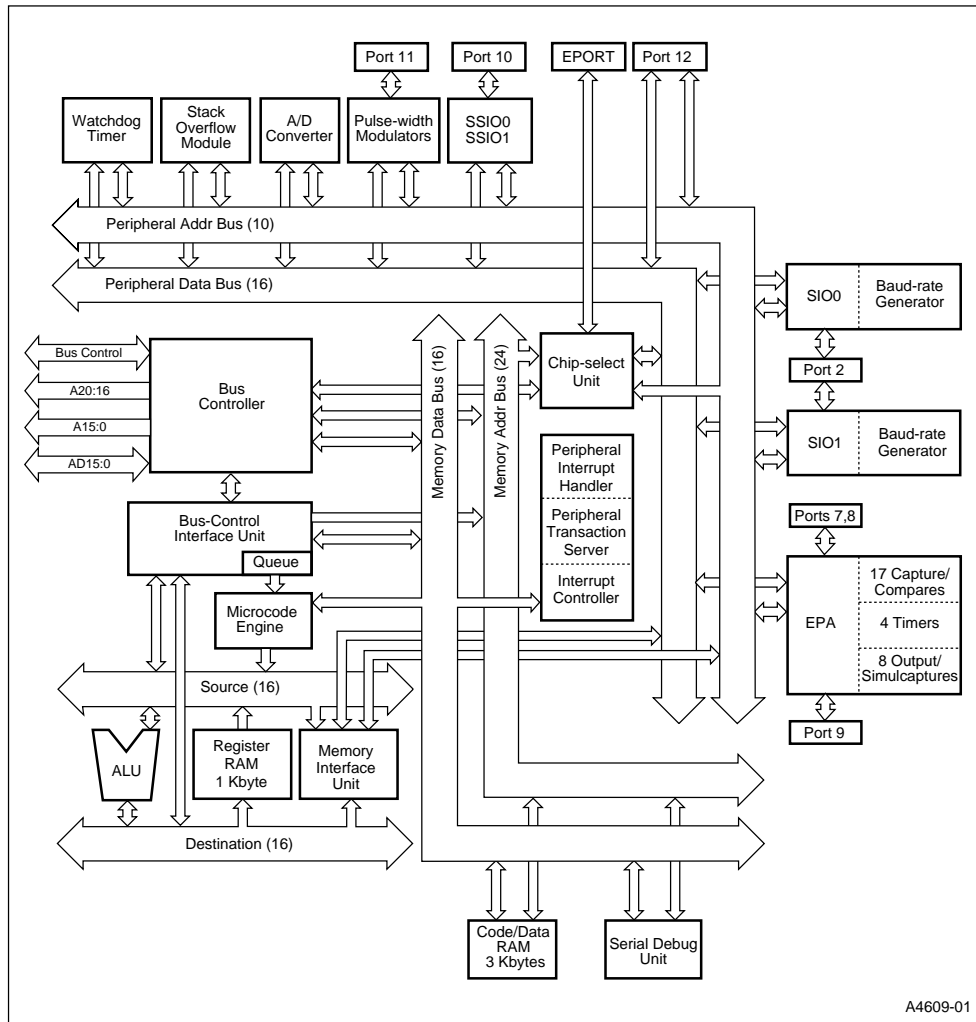
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1.0 Product Overview

The 80C196EA are typically used for high speed event control systems. Commercial applications include modem, motor-control systems, printers, photocopiers, air-conditioner control systems, disk drives and medical instruments. It is especially well suited to applications that benefit from its processing speed and enhanced peripheral set.

Figure 1. 80C196EA Block Diagram



The 80C196EA is highly integrated with an enhanced peripheral set. The serial debug unit (SDU) provides system debug and development capabilities. The SDU can set a single hardware breakpoint and provides read and write access to code RAM through a high-speed, dedicated serial link. A stack overflow/underflow monitor assists in code development by causing an unmaskable interrupt if the stack pointer crosses a user-defined boundary. The 16-channel A/D converter supports an auto-scan mode that operates with no CPU overhead. Each A/D channel has a dedicated result register. The EPA supports high-speed input captures and output compares with 17 programmable, high-speed capture/compare channels. Eight output-only channels provide support for time-base conversions by capturing the value of one of four timers when a compare occurs.

2.0 Nomenclature Overview

Figure 2. Product Nomenclature

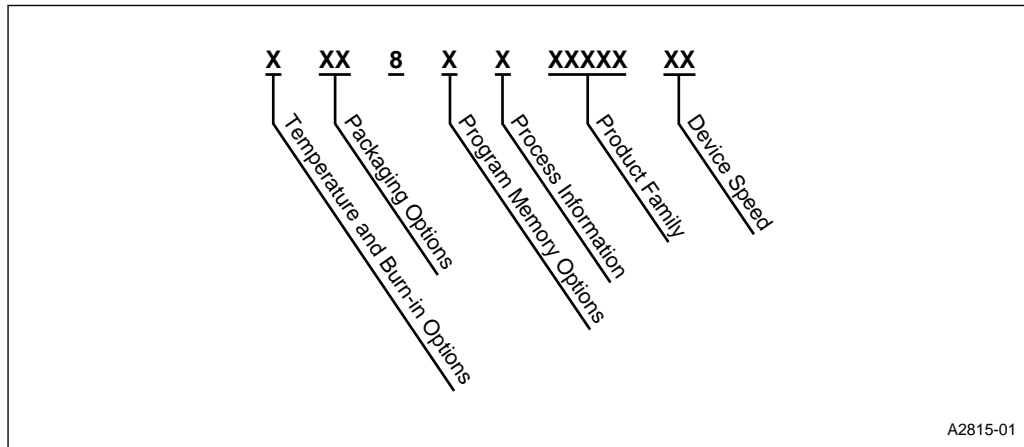


Table 1. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options		Commercial operating temperature range (0° C to 70° C Ambient) with Intel standard burn-in.
Packaging Options	S	QFP
Program Memory Options	0	CPU only - no internal ROM
Process Information	C	CHMOS
Product Family	196EA	
Device Speed	no mark	40 MHz

3.0 Pinout

Figure 3. S80C196EA 160-pin QFP Package

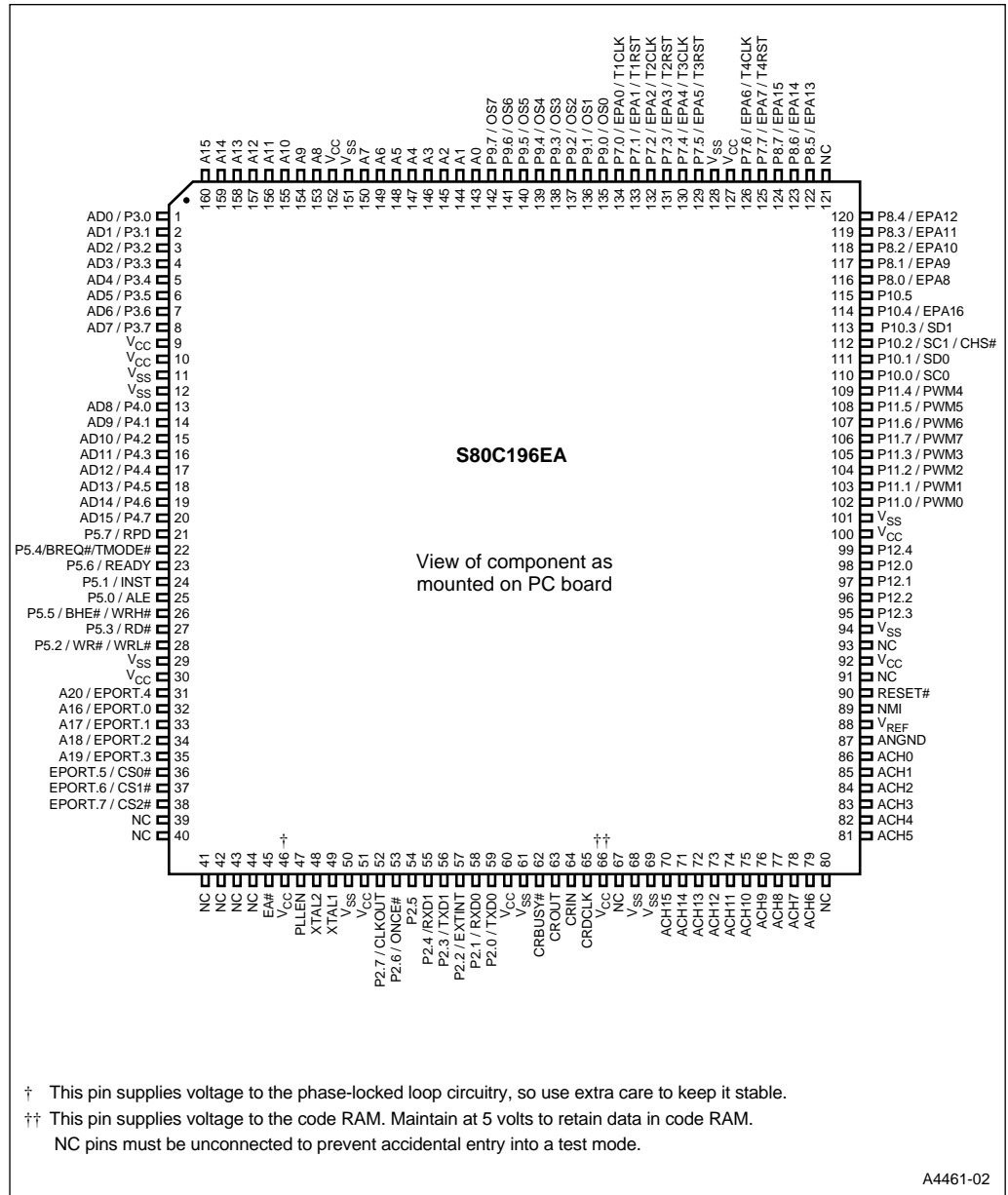


Table 2. 80C196EA 160-pin QFP Package Pin Assignments

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AD0 / P3.0	41	NC	81	ACH5	121	NC
2	AD1 / P3.1	42	NC	82	ACH4	122	P8.5 / EPA13
3	AD2 / P3.2	43	NC	83	ACH3	123	P8.6 / EPA14
4	AD3 / P3.3	44	NC	84	ACH2	124	P8.7 / EPA15
5	AD4 / P3.4	45	EA#	85	ACH1	125	P7.7 / EPA7 / T4RST
6	AD5 / P3.5	46	V _{CC}	86	ACH0	126	P7.6 / EPA6 / T4CLK
7	AD6 / P3.6	47	PLLEN	87	ANGND	127	V _{CC}
8	AD7 / P3.7	48	XTAL2	88	V _{REF}	128	V _{SS}
9	V _{CC}	49	XTAL1	89	NMI	129	P7.5 / EPA5 / T3RST
10	V _{CC}	50	V _{SS}	90	RESET#	130	P7.4 / EPA4 / T3CLK
11	V _{SS}	51	V _{CC}	91	NC	131	P7.3 / EPA3 / T2RST
12	V _{SS}	52	P2.7 / CLKOUT	92	V _{CC}	132	P7.2 / EPA2 / T2CLK
13	AD8 / P4.0	53	P2.6 / ONCE#	93	NC	133	P7.1 / EPA1 / T1RST
14	AD9 / P4.1	54	P2.5	94	V _{SS}	134	P7.0 / EPA0 / T1CLK
15	AD10 / P4.2	55	P2.4 / RXD1	95	P12.3	135	P9.0 / OS0
16	AD11 / P4.3	56	P2.3 / TXD1	96	P12.2	136	P9.1 / OS1
17	AD12 / P4.4	57	P2.2 / EXTINT	97	P12.1	137	P9.2 / OS2
18	AD13 / P4.5	58	P2.1 / RXD0	98	P12.0	138	P9.3 / OS3
19	AD14 / P4.6	59	P2.0 / TXD0	99	P12.4	139	P9.4 / OS4
20	AD15 / P4.7	60	V _{CC}	100	V _{CC}	140	P9.5 / OS5
21	P5.7 / RPD	61	V _{SS}	101	V _{SS}	141	P9.6 / OS6
22	P5.4/BREQ#/TMODE#	62	CRBUSY#	102	P11.0 / PWM0	142	P9.7 / OS7
23	P5.6 / READY	63	CROUT	103	P11.1 / PWM1	143	A0
24	P5.1 / INST	64	CRIN	104	P11.2 / PWM2	144	A1
25	P5.0 / ALE	65	CRDCLK	105	P11.3 / PWM3	145	A2
26	P5.5 / BHE# / WRH#	66	V _{CC}	106	P11.7 / PWM7	146	A3
27	P5.3 / RD#	67	NC	107	P11.6 / PWM6	147	A4
28	P5.2 / WR# / WRL#	68	V _{SS}	108	P11.5 / PWM5	148	A5
29	V _{SS}	69	V _{SS}	109	P11.4 / PWM4	149	A6
30	V _{CC}	70	ACH15	110	P10.0 / SC0	150	A7
31	A20 / EPORT.4	71	ACH14	111	P10.1 / SD0	151	V _{SS}
32	A16 / EPORT.0	72	ACH13	112	P10.2 / SC1	152	V _{CC}
33	A17 / EPORT.1	73	ACH12	113	P10.3 / SD1	153	A8
34	A18 / EPORT.2	74	ACH11	114	P10.4 / EPA16	154	A9
35	A19 / EPORT.3	75	ACH10	115	P10.5	155	A10
36	EPORT.5 / CS0#	76	ACH9	116	P8.0 / EPA8	156	A11
37	EPORT.6 / CS1#	77	ACH8	117	P8.1 / EPA9	157	A12
38	EPORT.7 / CS2#	78	ACH7	118	P8.2 / EPA10	158	A13
39	NC	79	ACH6	119	P8.3 / EPA11	159	A14
40	NC	80	NC	120	P8.4 / EPA12	160	A15

Table 3. Pin Assignment Arranged by Functional Categories (Sheet 1 of 2)

Addr & Data		Input/Output		Input/Output (Cont'd)		Input/Output (Cont'd)	
Name	Pin	Name	Pin	Name	Pin	Name	Pin
A0	143	P2.0 / TXD0	59	EP0RT.7	38	P12.0	98
A1	144	P2.1 / RXD0	58	P7.0 / EPA0 / T1CLK	134	P12.1	97
A2	145	P2.2	57	P7.1 / EPA1 / T1RST	133	P12.2	96
A3	146	P2.3 / TXD1	56	P7.2 / EPA2 / T2CLK	132	P12.3	95
A4	147	P2.4 / RXD1	55	P7.3 / EPA3 / T2RST	131	P12.4	99
A5	148	P2.5	54	P7.4 / EPA4 / T3CLK	130		
A6	149	P2.6	53	P7.5 / EPA5 / T3RST	129	Analog Inputs	
A7	150	P2.7	52	P7.6 / EPA6 / T4CLK	126	Name	Pin
A8	153	P3.0	1	P7.7 / EPA7 / T4RST	125	ACH0	86
A9	154	P3.1	2	P8.0 / EPA8	116	ACH1	85
A10	155	R3.2	3	P8.1 / EPA9	117	ACH2	84
A11	156	P3.3	4	P8.2 / EPA10	118	ACH3	83
A12	157	P3.4	5	P8.3 / EPA11	119	ACH4	82
A13	158	P3.5	6	P8.4 / EPA12	120	ACH5	81
A14	159	P3.6	7	P8.5 / EPA13	122	ACH6	79
A15	160	P3.7	8	P8.6 / EPA14	123	ACH7	78
A16	32	P4.0	13	P8.7 / EPA15	124	ACH8	77
A17	33	P4.1	14	P9.0 / OS0	135	ACH9	76
A18	34	P4.2	15	P9.1 / OS1	136	ACH10	75
A19	35	P4.3	16	P9.2 / OS2	137	ACH11	74
A20	31	P4.4	17	P9.3 / OS3	138	ACH12	73
AD0	1	P4.5	18	P9.4 / OS4	139	ACH13	72
AD1	2	P4.6	19	P9.5 / OS5	140	ACH14	71
AD2	3	P4.7	20	P9.6 / OS6	141	ACH15	70
AD3	4	P5.0	25	P9.7 / OS7	142		
AD4	5	P5.1	24	P10.0 / SC0	110	Bus Control & Status	
AD5	6	P5.2	28	P10.1 / SD0	111	Name	Pin
AD6	7	P5.3	27	P10.2 / SC1	112	ALE	25
AD7	8	P5.4	22	P10.3 / SD1	113	BHE#/WRH#	26
AD8	13	P5.5	26	P10.4 / EPA16	114	BREQ#	22
AD9	14	P5.6	23	P10.5	115	CS0#	36
AD10	15	P5.7	21	P11.0 / PWM0	102	CS1#	37
AD11	16	EP0RT.0	32	P11.1 / PWM1	103	CS2#	38
AD12	17	EP0RT.1	33	P11.2 / PWM2	104	INST	24
AD13	18	EP0RT.2	34	P11.3 / PWM3	105	RD#	27
AD14	19	EP0RT.3	35	P11.4 / PWM4	109	READY	23
AD15	20	EP0RT.4	31	P11.5 / PWM5	108		
		EP0RT.5	36	P11.6 / PWM6	107		
		EP0RT.6	37	P11.7 / PWM7	106	WR#/WRL#	28

Table 3. Pin Assignment Arranged by Functional Categories (Sheet 2 of 2)

Power & Ground		Processor Control	
Name	Pins	Name	Pin
ANGND	87	CLKOUT	52
V _{CC}	9, 10, 30, 46 [†] , 51, 60, 66 ^{††} , 92, 100, 127, 152	EA#	45
V _{SS}	11, 12, 29, 50, 61, 68, 69, 94, 101, 128, 151	EXTINT	57
V _{REF}	88	NMI	89
		ONCE#	53
No Connection		PLEN	47
Name	Pins	RESET#	90
NC ^{†††}	39–44, 67, 69, 80, 91, 93, 121	RPD	21
		TMODE#	22
		XTAL1	49
		XTAL2	48

† This pin supplies voltage to the phase-locked loop circuitry, so use extra care to keep it stable.

†† This pin supplies voltage to code RAM. To retain data, maintain 5 volts.

††† Always leave NC (no connect) pins unconnected to prevent accidental entry into test modes.

Code Debug	
Name	Pin
CRBUSY#	62
CRDCLK	65
CRIN	64
CROUT	63

4.0 Signals

Table 4. Signal Descriptions (Sheet 1 of 3)

Name	Type	Description												
ALE	O	<p>Address Latch Enable</p> <p>This active-high output signal is asserted only during external memory cycles. ALE signals the start of an external bus cycle and indicates that valid address information is available on the system address/data bus.</p> <p>An external latch can use this signal to demultiplex address from the address/data bus.</p>												
BHE#	O	<p>Byte High Enable[†]</p> <p>During 16-bit bus cycles, this active-low output signal is asserted for word and high-byte reads and writes to external memory. BHE# indicates that valid data is being transferred over the upper half of the system data bus. Use BHE#, in conjunction with A0, to determine which memory byte is being transferred over the system bus:</p> <table border="1"> <thead> <tr> <th>BHE#</th> <th>A0</th> <th>Byte(s) Accessed</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>both bytes</td> </tr> <tr> <td>0</td> <td>1</td> <td>high byte only</td> </tr> <tr> <td>1</td> <td>0</td> <td>low byte only</td> </tr> </tbody> </table> <p>BHE# shares a package pin with WRH#.</p> <p>[†] The chip configuration register 0 (CCR0) determines whether this pin functions as BHE# or WRH#. CCR0.2 = 1 selects BHE#; CCR0.2 = 0 selects WRH#.</p>	BHE#	A0	Byte(s) Accessed	0	0	both bytes	0	1	high byte only	1	0	low byte only
BHE#	A0	Byte(s) Accessed												
0	0	both bytes												
0	1	high byte only												
1	0	low byte only												
CLKOUT	O	<p>Clock Output</p> <p>Output of the internal clock generator. CLKOUT has a 50% duty cycle. shares a package pin</p>												
EXTINT	I	<p>External Interrupt</p> <p>In powerdown mode, asserting the EXTINT signal for at least 50 ns causes the device to resume normal operation. The interrupt need not be enabled, but the pin must be configured as a special-function input. If the EXTINT interrupt is enabled, the CPU executes the interrupt service routine. Otherwise, the CPU executes the instruction that immediately follows the command that invoked the power-saving mode.</p> <p>In idle mode, asserting any enabled interrupt causes the device to resume normal operation.</p>												
INST	O	<p>Instruction Fetch</p> <p>This active-high output signal is valid only during external memory bus cycles. When high, INST indicates that an instruction is being fetched from external memory. The signal remains high during the entire bus cycle of an external instruction fetch. INST is low for data accesses, including interrupt vector fetches and chip configuration byte reads. INST is low during internal memory fetches.</p>												
NMI	I	<p>Nonmaskable Interrupt</p> <p>In normal operating mode, a rising edge on NMI generates a nonmaskable interrupt. NMI has the highest priority of all prioritized interrupts. Assert NMI for greater than one state time to guarantee that it is recognized.</p>												
ONCE	I	<p>On-circuit Emulation</p> <p>Holding ONCE during the rising edge of RESET# places the device into on-circuit emulation (ONCE) mode. PLEN must also be held low. This mode puts all pins into a high-impedance state, thereby isolating the device from other components in the system. The value of ONCE is latched when the RESET# pin goes inactive. While the device is in ONCE mode, you can debug the system using a clip-on emulator.</p> <p>To exit ONCE mode, reset the device by pulling the RESET# signal low. To prevent inadvertent entry into ONCE mode, .</p>												

Table 4. Signal Descriptions (Sheet 2 of 3)

Name	Type	Description
RD#	O	Read Read-signal output to external memory. RD# is asserted only during external memory reads.
READY	I	Ready Input This active-high input signal is used to lengthen external memory cycles for slow memory by generating wait states in addition to the wait states that are generated internally. When READY is high, CPU operation continues in a normal manner with wait states inserted as programmed in the chip configuration registers. READY is ignored for all internal memory accesses.
RESET#	I/O	Reset A level-sensitive reset input to and open-drain system reset output from the microcontroller. Either a falling edge on RESET# or an internal reset turns on a pull-down transistor connected to the RESET# pin for 16 state times. In the powerdown and idle modes, asserting RESET# causes the chip to reset and return to normal operating mode. After a device reset, the first instruction fetch is from FF2080H.
RXD	I/O	Receive Serial Data In modes 1, 2, and 3, RXD receive serial port input data. In mode 0, functions as either input or open-drain output for data.
TMODE#	I	Test-Mode Entry If this pin is held low during reset, the device will enter a test mode. The value of several other pins defines the actual test mode. All test modes, except test-ROM execution, are reserved for Intel factory use. If you choose to configure this signal as an input, always hold it high during reset and ensure that your system meets the V_{IH} specification to prevent inadvertent entry into test mode. TMODE# with P5.4 and BREQ#.
TXD	O	Transmit Serial Data In serial I/O modes 1, 2, and 3, TXD transmit serial port output data. In mode 0, the serial clock output. TXD with .
V_{CC}	PWR	Digital Supply Voltage Connect each V_{CC} pin to the digital supply voltage.
V_{SS}	GND	Digital Circuit Ground These pins supply ground for the digital circuitry. Connect each V_{SS} pin to ground through the lowest possible impedance path.
WR#	O	Write [†] This active-low output indicates that an external write is occurring. This signal is asserted only during external memory writes. WR# is multiplexed with . † The chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.
WRH#	O	Write High [†] During 16-bit bus cycles, this active-low output signal is asserted for high-byte writes and word writes to external memory. During 8-bit bus cycles, WRH# is asserted for all write operations. WRH# with BHE#. † The chip configuration register 0 (CCR0) determines whether this pin functions as BHE# or WRH#. CCR0.2 = 1 selects BHE#; CCR0.2 = 0 selects WRH#.

Table 4. Signal Descriptions (Sheet 3 of 3)

Name	Type	Description
WRL#	O	<p>Write Low[†]</p> <p>During 16-bit bus cycles, this active-low output signal is asserted for low-byte writes and word writes to external memory. During 8-bit bus cycles, WRL# is asserted for all write operations.</p> <p>WRL# with WR#.</p> <p>[†] The chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.</p>
XTAL1	I	<p>Input Crystal/Resonator or External Clock Input</p> <p>Input to the on-chip oscillator and the internal clock generators. The internal clock generators provide the peripheral clocks, CPU clock, and CLKOUT signal. When using an external clock source instead of the on-chip oscillator, connect the clock input to XTAL1. The external clock signal must meet the V_{IH} specification for XTAL1.</p>
XTAL2	O	<p>Inverted Output for the Crystal/Resonator</p> <p>Output of the on-chip oscillator inverter. Leave XTAL2 floating when the design uses an external clock source instead of the on-chip oscillator.</p>

5.0 Address Map

Table 5. 80C196EA Address Map

Hex Address	Description (Note 1, Note 2)	Addressing Modes
FFFFFF FF4000	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
FF3FFF FF2140	Program memory	Indirect, indexed, extended (3)
FF213F FF20C0	Special-purpose memory (PIH vectors)	Indirect, indexed, extended (3)
FF20BF FF2080	Program memory (After reset, the first instruction is fetched from FF2080H.)	Indirect, indexed, extended (3)
FF207F FF2000	Special-purpose memory (CCBs, interrupt vectors, PTS vectors)	Indirect, indexed, extended
FF1FFF FF1000	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
FF0FFF FF0400	Internal code/data RAM (identically mapped from page 00H)	Indirect, indexed, extended
FF03FF FF0000	Reserved for in-circuit emulators	—
FEFFFF 1F0000	Overlaid memory (reserved for future devices); locations xF0000–xF03FFH are reserved for in-circuit emulators	Indirect, indexed, extended
1EFFFF 002000	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
001FFF 001FE0	Memory-mapped special-function registers (SFRs)	Indirect, indexed, extended
001FDF 001C00	Peripheral special-function registers (SFRs)	Indirect, indexed, extended, windowed direct
001BFF 001000	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
000FFF 000400	Internal code/data RAM (identically mapped into page FFH)	Indirect, indexed, extended
0003FF 000100	Upper register file (general-purpose register RAM)	Indirect, indexed, windowed direct
0000FF 00001A	Lower register file (general-purpose register RAM)	Direct, indirect, indexed
000019 000000	Lower register file (stack pointer and CPU SFRs)	Direct, indirect, indexed

NOTES:

1. Unless otherwise noted, write 0FFH to reserved memory locations and write 0 to reserved SFR bits.
2. The contents or functions of reserved locations may change in future device revisions, in which case a program that relies on one or more of these locations might not function properly.
3. External memory occupies the boot memory partition, FF2080-FF3FFFH.

6.0 Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-60°C to +150°C
Supply Voltage with Respect to V_{SS}	-0.5 V to +7.0 V
Power Dissipation	1.5 W

OPERATING CONDITIONS

T_A (Ambient Temperature Under Bias)	0°C to +70°C
V_{CC} (Digital Supply Voltage)	4.5 V to 5.5 V
V_{REF} (Analog Supply Voltage)	4.5 V to 5.5 V
F_{XTAL1} (Input frequency for $V_{CC} = 4.5\text{ V} - 5.5\text{ V}$) (Note 1)	20 MHz to 40 MHz

NOTE:

1. This device is static and should operate below 1 Hz, but has been tested only down to 20 MHz.

NOTICE: This document contains information on products in the design phase of development. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

6.1 DC Characteristics

Table 6. DC Characteristics at $V_{CC} = 4.5\text{ V} - 5.5\text{ V}$ (Sheet 1 of 2)

Sym	Parameter	Min	Typ (1)	Max	Units	Test Conditions
I_{CC}	V_{CC} supply current		120	135	mA	XTAL1 = 40 MHz $V_{CC} = 5.5\text{ V}$ Device in Reset
I_{IDLE}	Idle mode current		60	95	mA	XTAL1 = 40 MHz $V_{CC} = 5.5\text{ V}$
I_{PD}	Powerdown mode current		50		μA	$V_{CC} = 5.5\text{ V}$
I_{REF}	A/D reference supply current			5	mA	XTAL1 = 40 MHz $V_{CC} = V_{REF} = 5.5\text{ V}$ Device in Reset
I_{CRVCC}	Code RAM V_{CC} Supply Current			110	μA	$V_{CC} = 5.5\text{ V}$
I_{INJD}	Maximum injection current per port on bidirectional pins	-10		10	mA	(4)
I_{LI}	Input leakage current (Standard inputs except analog inputs)	-10		10	μA	$V_{SS} < V_{IN} < V_{CC}$
I_{LI1}	Input leakage current (analog inputs)	-300		300	nA	$V_{SS} + 100\text{ mV} < V_{IN} < V_{REF} - 100\text{ mV}$
I_{IH}	Input high current (NMI only)			175	μA	$NMI = V_{CC} = 5.5\text{ V}$
V_{IL1}	Input low voltage	-0.5		$0.3 V_{CC}$	V	(2)
V_{IH1}	Input high voltage	$0.7 V_{CC}$		$V_{CC} + 0.5$	V	(2)
V_{IL2}	Input low voltage	-0.5		$0.4 V_{CC}$	V	(3)

NOTES:

1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with $V_{CC} = 5.0\text{ V}$.
2. For P2.7:0, P3.7:0, P4.7:0, P5.7:0, P10.3:0, P11.7:0, P12.4:0, AD15:0, EA#, RESET#, PLEN, NMI, TDI, TCLK, ONCE#, and XTAL1.
3. For P7.7:0, P8.7:0, P9.7:0, and P10.5:4.
4. The maximum injection current is not tested. The device is designed to meet this specification.
5. Pin capacitance is not tested. This value is based on design simulations.

Table 6. DC Characteristics at $V_{CC} = 4.5\text{ V} - 5.5\text{ V}$ (Sheet 2 of 2)

Sym	Parameter	Min	Typ (1)	Max	Units	Test Conditions
V_{IH2}	Input high voltage	$0.7 V_{CC}$		$V_{CC} + 0.5$	V	(3)
V_{OL1}	Output low voltage (output configured as complementary)			0.3 0.45 1.5	V	$I_{OL} = 200\ \mu\text{A}$ $I_{OL} = 3.2\ \text{mA}$ $I_{OL} = 7.0\ \text{mA}$
V_{OH1}	Output high voltage (output configured as complementary)	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V	$I_{OH} = -200\ \mu\text{A}$ $I_{OH} = -3.2\ \text{mA}$ $I_{OH} = -7.0\ \text{mA}$
V_{OL2}	Output low voltage in reset			0.5	V	$I_{OL} = 15\ \mu\text{A}$
I_{OH2}	Output high current in reset	-30 -65 -75		-120 -240 -280	μA	$V_{OH2} = V_{CC} - 1\ \text{V}$ $V_{OH2} = V_{CC} - 2.5\ \text{V}$ $V_{OH2} = V_{CC} - 4\ \text{V}$
I_{OH3}	Output high current in reset on Port 11	-5 -8 -10		-50 -110 -130	μA	$V_{OH3} = V_{CC} - 1\ \text{V}$ $V_{OH3} = V_{CC} - 2.5\ \text{V}$ $V_{OH3} = V_{CC} - 4\ \text{V}$
V_{OH2}	Output high voltage in reset	$V_{CC} - 1$			V	$I_{OH} = -15\ \mu\text{A}$
V_{HYS}	Hysteresis voltage on all inputs except XTAL1	700			mV	
C_S	Pin Capacitance (any pin to V_{SS})			10	pF	(5)
R_{RST}	Pull-up resistor on RESET# pin	9		95	$\text{k}\Omega$	$V_{CC} = 5.5\ \text{V}$, $V_{IN} = 4.0\ \text{V}$

NOTES:

- Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with $V_{CC} = 5.0\ \text{V}$.
- For P2.7:0, P3.7:0, P4.7:0, P5.7:0, P6.7:0, P10.3:0, P11.7:0, P12.4:0, AD15:0, EA#, RESET#, PLEN, NMI, TDI, TCLK, ONCE#, and XTAL1.
- For P7.7:0, P8.7:0, P9.7:0, and P10.5:4.
- The maximum injection current is not tested. The device is designed to meet this specification.
- Pin capacitance is not tested. This value is based on design simulations.

6.2 AC Characteristics — Multiplexed Bus Mode

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 7. AC Characteristics, Multiplexed Bus Mode (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units
F _{XTAL1}	Frequency on XTAL1, PLL in 1x mode	20	40	MHz (1, 8)
	Frequency on XTAL1, PLL in 2x mode	10	20	MHz (8)
f	Operating frequency, $f = F_{XTAL1}$; PLL in 1x mode	20	40	MHz (8)
	Operating frequency, $f = 2F_{XTAL1}$; PLL in 2x mode			
t	Period, $t = 1/f$	25	50	ns
T _{AVDV}	Address Valid to Input Data Valid		3t – 40	ns (2)
T _{RLDV}	RD# Low to Input Data Valid		t – 18	ns (2)
T _{CHDV}	CLKOUT High to Input Data valid		2t – 35	ns (9)
T _{RHDZ}	RD# High to Input Data Float		t + 5	ns
T _{RXDX}	Data Hold after RD# Inactive	0		ns
T _{XHCH}	XTAL1 Rising Edge to CLKOUT High or Low	3	50	ns (9)
T _{CLCL}	CLKOUT Cycle Time	2t		ns (9)
T _{CHCL}	CLKOUT High Period	t – 10	t + 10	ns (9)
T _{CLLH}	CLKOUT Falling to ALE Rising	– 10	10	ns (9)
T _{LLCH}	ALE Falling to CLKOUT Rising	– 10	10	ns (9)
T _{LHLH}	ALE Cycle Time	4t		ns (2)
T _{LHLL}	ALE High Period	t – 10	t + 10	ns
T _{AVLL}	Address Setup to ALE Low	t – 15		ns
T _{LLAX}	Address Hold after ALE Low	t – 15		ns
T _{LLRL}	ALE Low to RD# Low	t – 15		ns
T _{RLCL}	RD# Low to CLKOUT Low	– 10	10	ns (9)
T _{RLRH}	RD# Low to RD# High	t – 12		ns (2)
T _{RHLH}	RD# High to ALE Rising	t – 5	t + 15	ns (3)
T _{RLAZ}	RD# Low to Address Float		5	ns
T _{LLWL}	ALE Low to WR# Low	t – 12		ns
T _{QVWH}	Data Stable to WR# Rising Edge	t – 14		ns (2)
T _{CHWH}	CLKOUT High to WR# Rising Edge	– 10	10	ns (9)
T _{WLWH}	WR# Low to WR# High	t – 10		ns (2)

NOTES:

- 20 MHz is the maximum input frequency when using an external crystal oscillator; however, 40 MHz can be applied with an external clock source.
- If wait states are used, add $2t \times n$, where n = number of wait states.
- Assuming back-to-back bus cycles.
- When forcing wait states using the BUSCON register, add $2t \times n$.
- Exceeding the maximum specification causes additional wait states.
- 8-bit bus only.
- The first falling edge of READY is not synchronized to a CLKOUT edge; therefore, one programmed wait state is required.
- Device is static by design but has been tested only down to 20 MHz.
- Assumes CLKOUT is operating in divide-by-two mode ($f/2$).

Table 7. AC Characteristics, Multiplexed Bus Mode (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units
T_{WHQX}	Data Hold after WR# High	$t - 20$		ns
T_{WHLH}	WR# High to ALE High	$t - 15$	$t + 10$	ns
T_{WHBX}	BHE#, INST Hold after WR# High	$t - 4$		ns
T_{WHAX}	AD15:8, CSx# Hold after WR# High	$t - 4$		ns (6)
T_{RHBX}	BHE#, INST Hold after RD# High	$t - 5$		ns
T_{RHAX}	AD15:8, CSx# Hold after RD# High	$t - 5$		ns (6)
T_{WHSB}	A20:0, CSx# Hold after WR# High	0		ns
T_{RHSH}	A20:0, CSx# Hold after RD# High	0		ns
T_{AVYV}	AD15:0 Valid to READY Setup		$2t - 40$	ns (4)
T_{CLYX}	READY Hold after CLKOUT Low	0	$2t - 40$	ns (5, 7, 9)
T_{LYLH}	Non-READY Time	No Upper Limit		ns

NOTES:

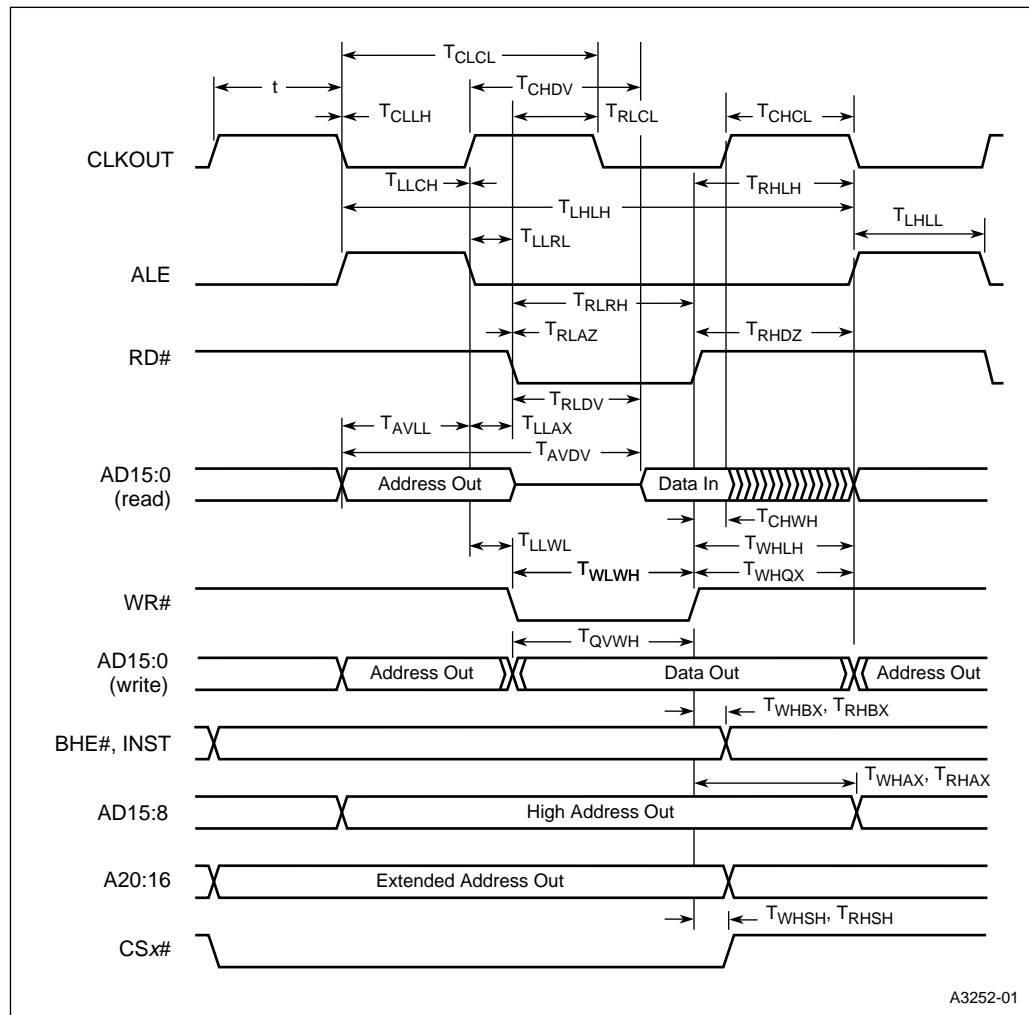
- 20 MHz is the maximum input frequency when using an external crystal oscillator; however, 40 MHz can be applied with an external clock source.
- If wait states are used, add $2t \times n$, where n = number of wait states.
- Assuming back-to-back bus cycles.
- When forcing wait states using the BUSCON register, add $2t \times n$.
- Exceeding the maximum specification causes additional wait states.
- 8-bit bus only.
- The first falling edge of READY is not synchronized to a CLKOUT edge; therefore, one programmed wait state is required.
- Device is static by design but has been tested only down to 20 MHz.
- Assumes CLKOUT is operating in divide-by-two mode ($f/2$).

Table 8. AC Timing Symbol Definitions

Signals				Conditions			
A [†]	Address	L	ALE	W	WR#, WRH#, WRL#	H	High
B	BHE#	Q	Output Data	X	XTAL1	L	Low
C	CLKOUT	R	RD#	Y	READY	V	Valid
D	Input Data	S	CSx#			X	No Longer Valid
						Z	Floating

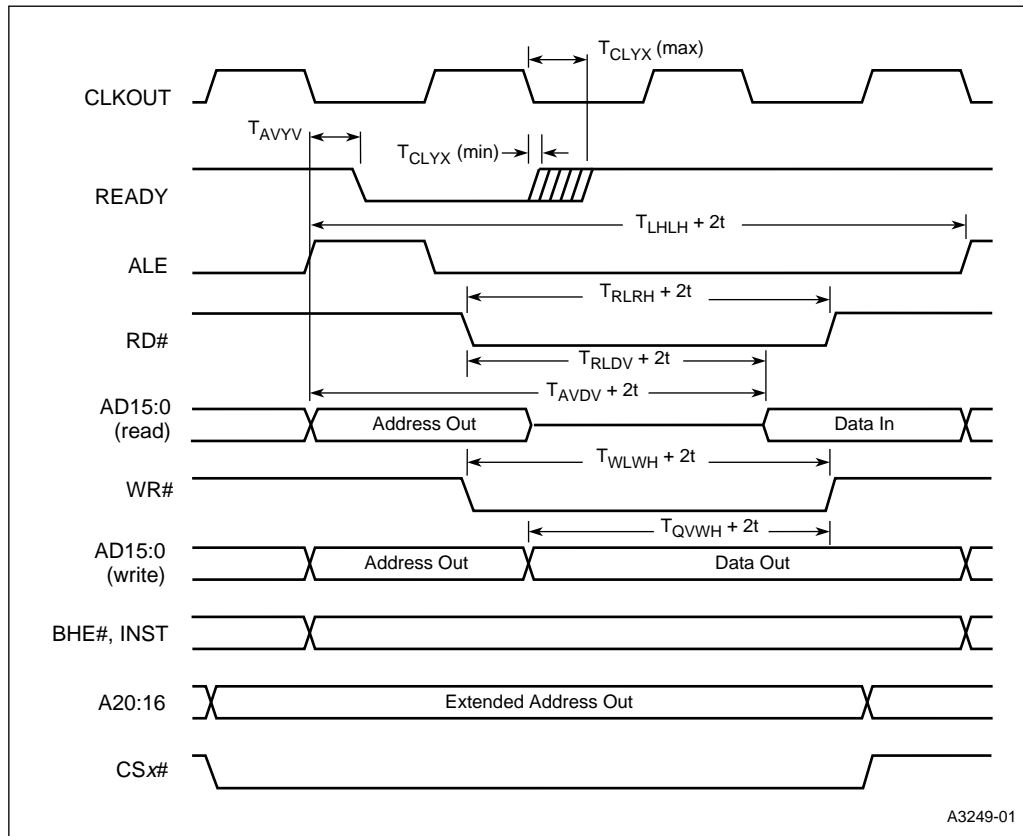
[†] Address bus (demultiplexed mode) or address/data bus (multiplexed mode)

Figure 4. System Bus Timing Diagram (Multiplexed Bus Mode)



A3252-01

Figure 5. READY Timing Diagram (Multiplexed Bus Mode)



6.3 AC Characteristics — Demultiplexed Bus Mode

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 9. AC Characteristics, Demultiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
F _{XTAL1}	Frequency on XTAL1, PLL in 1x mode	20	40	MHz (1,8)
	Frequency on XTAL1, PLL in 2x mode	10	20	MHz (8)
f	Operating frequency, $f = F_{XTAL1}$; PLL in 1x mode	20	40	Mhz
	Operating frequency, $f = 2F_{XTAL1}$; PLL in 2x mode			
t	Period, $t = 1/f$	25	50	ns
T _{AVDV}	Address Valid to Input Data Valid		4t – 23	ns (2)
T _{RLDV}	RD# Low to Input Data Valid		3t – 25	ns (2)
T _{AVWL}	Address Valid to WR# Low	t		ns
T _{AVRL}	Address Valid to RD# Low	t – 8		ns
T _{SLDV}	Chip Select Low to Data Valid		4t – 27	ns (2)
T _{CHDV}	CLKOUT Rising Edge to Input Data Valid		2t – 25	ns (9)
T _{RHDZ}	RD# High to Input Data Float		t – 5	ns
T _{RHRL}	Read High to Next Read Low	t – 5		ns
T _{RXDX}	Data Hold after RD# Inactive	0		ns
T _{XHCH}	XTAL1 High to CLKOUT High or Low	10	35	ns (9)
T _{CLCL}	CLKOUT Cycle Time	2t		ns (9)
T _{CHCL}	CLKOUT High Period	t – 10	t + 10	ns (9)
T _{CLLH}	CLKOUT Falling ALE Rising	– 10	10	ns (9)
T _{RLCL}	RD# Low to CLKOUT Low	– 5	5	ns (9)
T _{RLRH}	RD# Low to RD# High	3t – 12		ns (2)
T _{RHLH}	RD# Rising to ALE Rising	t – 4	t + 12	ns (3)
T _{WLCL}	WR# Low to CLKOUT Falling	– 12	5	ns (9)
T _{QVWH}	Data Stable to WR# Rising Edge	3t – 18		ns (3)
T _{CHWH}	CLKOUT High to WR# Rising Edge	– 5	10	ns (9)
T _{WLWH}	WR# Low to WR# High	3t – 15		ns (2)
T _{WHQX}	Data Hold after WR# Rising Edge	t	t + 15	ns
T _{WHBX}	BHE#, INST Hold after WR# High	t		ns
T _{WHAX}	A20:0, CSx# Hold after WR# High	0		ns
T _{RHBX}	BHE#, INST Hold after RD# High	t		ns
T _{RHAX}	A20:0, CSx# Hold after RD# High	0		ns
T _{AVYV}	A20:0 Valid to READY Setup		3t – 25	ns (4)
T _{CLYX}	READY Hold after CLKOUT Low	0	2t – 28	ns (5, 7,9)
T _{YLYH}	Non READY Time		No Upper Limit	ns

NOTES:

- 20 MHz is the maximum input frequency when using an external crystal oscillator; however, 40 MHz can be applied with an external clock source.
- If wait states are used, add $2t \times n$, where n = number of wait states.
- Assuming back-to-back bus cycles.
- When forcing wait states using the BUSCON register, add $2t \times n$.
- Exceeding the maximum specification causes additional wait states.
- 8-bit bus only.
- The first falling edge of READY is not synchronized to a CLKOUT edge; therefore, one programmed wait state is required.
- Device is static by design but has been tested only down to 20 MHz.
- Assumes CLKOUT is operating in divide-by-two mode ($f/2$).

Figure 6. System Bus Timing Diagram (Demultiplexed Bus Mode)

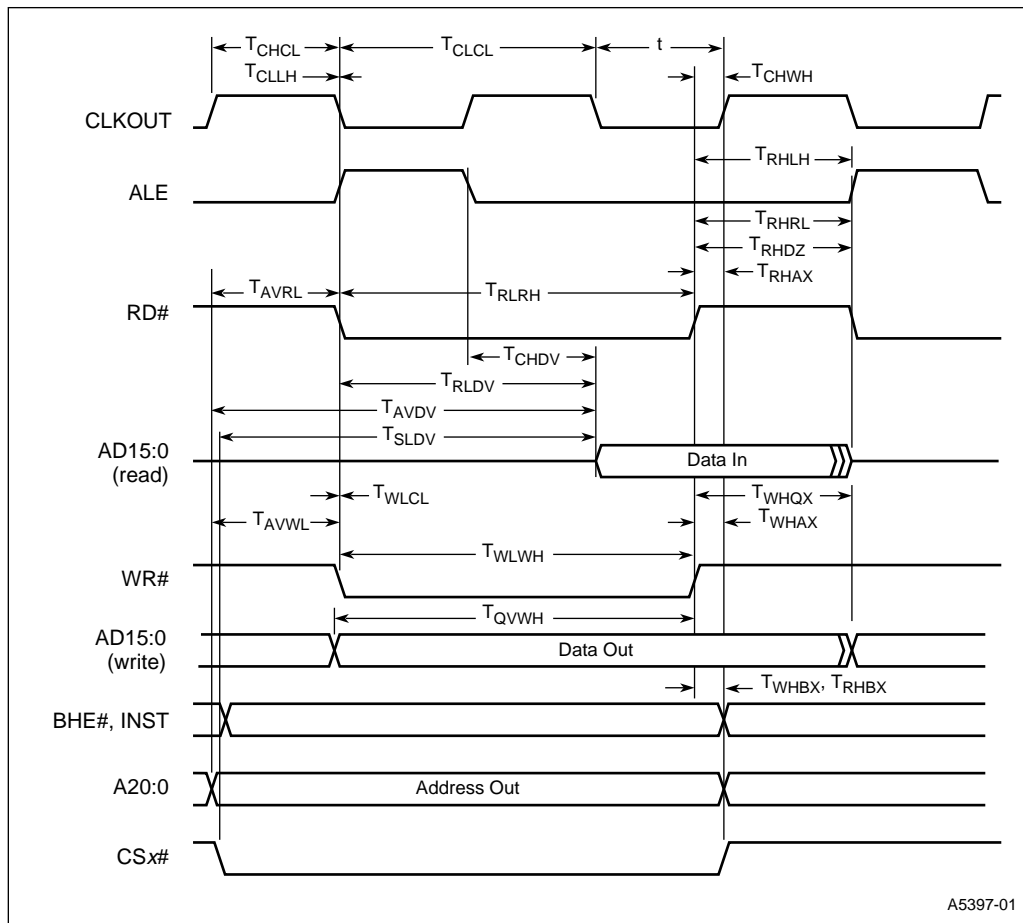
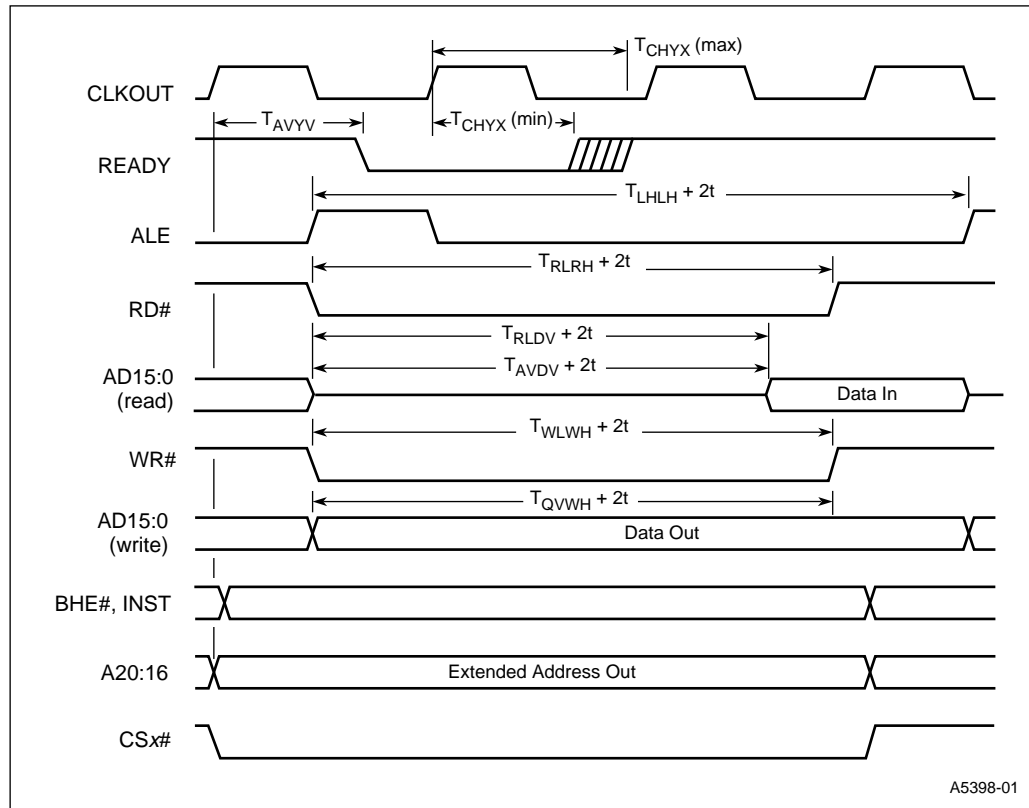


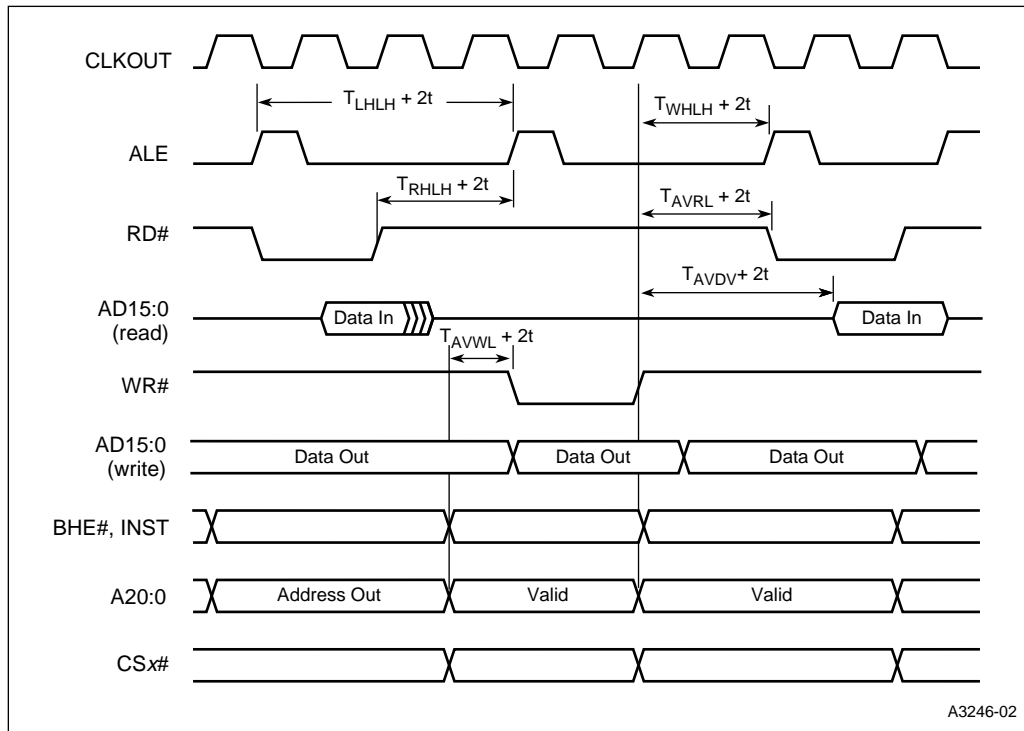
Figure 7. READY Timing Diagram (Demultiplexed Bus Mode)



6.4 Deferred Bus Timing Mode

Deferred Bus Cycle Mode: This bus mode (enabled by setting CCB1.5) reduces bus contention when using the 80C196EA in demultiplexed mode with slow memories. As shown in Figure 8, a delay of $2t$ occurs in the first bus cycle following a chip-select output change and the first write cycle following a read cycle.

Figure 8. Deferred Bus Mode Timing Diagram



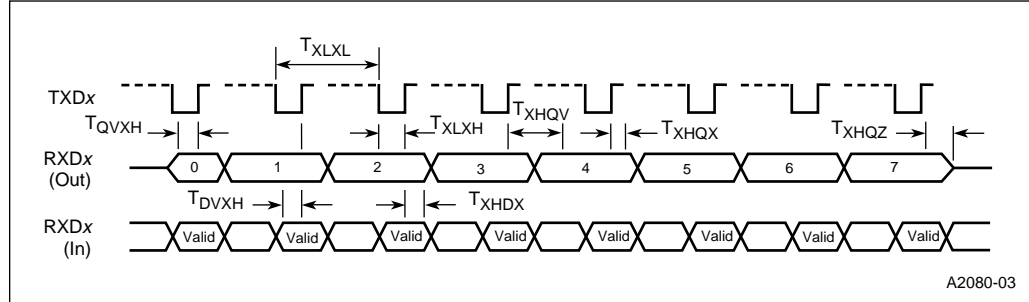
6.5 AC Characteristics — Serial Port, Shift Register Mode

Table 10. Serial Port Timing — Shift Register Mode

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock period			
	SP_BAUD \geq x002H SP_BAUD = x001H ¹	6t 4t		ns ns
T_{XLXH}	Serial Port Clock falling edge to rising edge			
	SP_BAUD \geq x002H SP_BAUD = x001H ¹	4t - 27 2t - 27	4t + 27 2t + 27	ns ns
T_{QVXH}	Output data setup to clock high	4t - 30		ns
T_{XHGX}	Output data hold after clock high	2t - 30		ns
T_{XHGV}	Next output data valid after clock high		2t + 30	ns
T_{DVXH}	Input data setup to clock high	2t + 30		ns
T_{XHDX}	Input data hold after clock high	0		ns
T_{XHQZ}	Last clock high to output float		t + 30	ns

1. The minimum baud-rate (SP_BAUD) register value for receive is x002H and the minimum baud-rate (SP_BAUD) register value for transmit is x001H.

Figure 9. Serial Port Waveform — Shift Register Mode

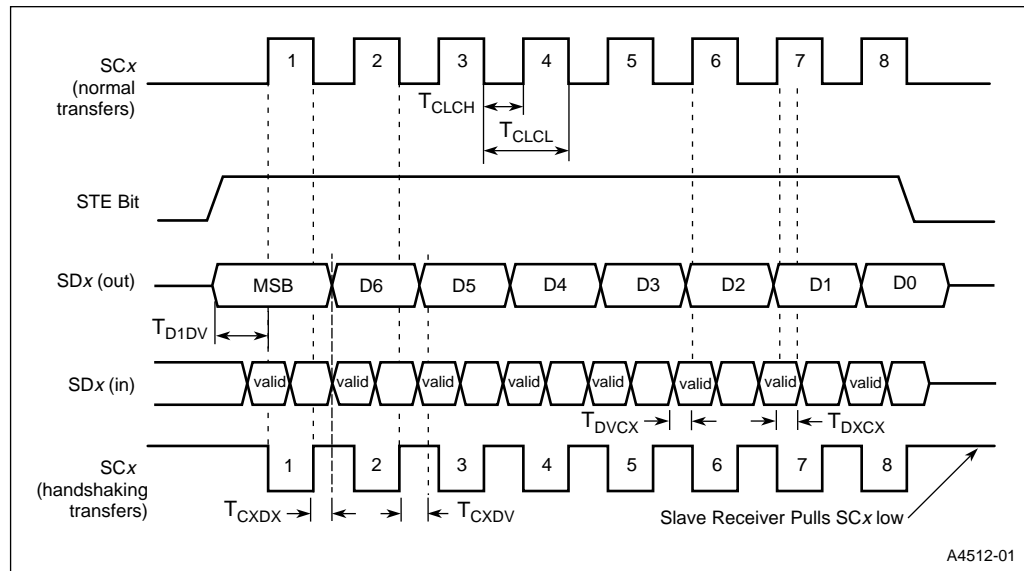


6.6 AC Characteristics — Synchronous Serial Port

Table 11. Synchronous Serial Port Timing

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Synchronous Serial Port Clock period	8t		ns
T_{CLCH}	Synchronous Serial Port Clock falling edge to rising edge	4t		ns
T_{D1DV}	Setup time for MSB output	2t		ns
T_{CXDV}	Setup time for D6:0 output		3t + 20	ns
T_{CXDX}	Output data hold after clock low	t	3t + 20	ns
T_{DVCX}	Setup time for input data	10		ns
T_{DXCX}	Input data hold after clock high	t + 5		ns

Figure 10. Synchronous Serial Port



6.7 A/D Sample and Conversion Times

Two parameters, sample time and conversion time, control the time required for an A/D conversion. The sample time is the length of time that the analog input voltage is actually connected to the sample capacitor. If this time is too short, the sample capacitor will not charge completely. If the sample time is too long, the input voltage may change and cause conversion errors. The conversion time is the length of time required to convert the analog input voltage stored on the sample capacitor to a digital value. The conversion time must be long enough for the comparator and circuitry to settle and resolve the voltage. Excessively long conversion times allow the sample capacitor to discharge, degrading accuracy.

The AD_TIME register programs the A/D sample and conversion times. Use the T_{SAM} and T_{CONV} specifications in [Table 12](#) and [Table 14](#) to determine appropriate values for SAM and CONV; otherwise, erroneous conversion results may occur.

When the SAM and CONV values are known, write them to the AD_TIME register. Do not write to this register while a conversion is in progress; the results are unpredictable.

Use the following formulas to determine the SAM and CONV values.

$$SAM = \frac{T_{SAM} \times f - 2}{8} \qquad CONV = \left[\frac{T_{CONV} \times f - 3}{2 \times B} \right] - 1$$

where:

SAM	equals a number, 1 to 7
CONV	equals a number, 2 to 31
T_{SAM}	is the sample time, in μsec (Table 12 and Table 14)
T_{CONV}	is the conversion time, in μsec (Table 12 and Table 14)
f	is the operating frequency, in MHz
B	is the number of bits to be converted (8 or 10)

At 40 Mhz, to meet T_{SAM} and T_{CONV} minimum specifications:

10-bit mode: SAM= [5, 6, 7] $\Rightarrow T_{SAM} \geq 1\mu s$
 CONV= [18, 19, 20, ..., 31] $\Rightarrow T_{CONV} \geq 10\mu s$

8-bit mode: SAM= [5, 6, 7] $\Rightarrow T_{SAM} \geq 1\mu s$
 CONV= [23, 24, ..., 31] $\Rightarrow T_{CONV} \geq 10\mu s$

6.7.1 AC Characteristics — A/D Converter, 10-bit Mode

Table 12. 10-bit A/D Operating Conditions (1)

Symbol	Description	Min	Max	Units	Notes
T_A	Ambient Temperature	0	70	°C	
V_{CC}	Digital Supply Voltage	4.50	5.50	V	
V_{REF}	Analog Supply Voltage	4.50	5.50	V	(2)
T_{SAM}	Sample Time	1.0		μs	(3)
T_{CONV}	Conversion Time	10.0	15.0	μs	(3)

NOTES:

1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than + 0.5 V because V_{REF} supplies both the resistor ladder and the analog portion of the converter and input port pins.
3. Program the AD_TIME register to meet the T_{SAM} and T_{CONV} specifications.

Table 13. 10-bit Mode A/D Characteristics Over Specified Operating Conditions (7)

Parameter	Typical (2)	Min	Max	Units (1)	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	± 3.0	LSBs	
Full-scale Error	0.25 ± 0.5				
Zero Offset Error	0.25 ± 0.5				
Nonlinearity	1.0 ± 2.0		± 3.0		
Differential Nonlinearity		- 0.75	+ 0.75		
Channel-to-channel Matching	± 0.1	0	± 1.0		
Repeatability	± 0.25	0			
Temperature Coefficients: Offset Full-scale Differential Nonlinearity	0.009 0.009 0.009			LSB/C	
Off-isolation		- 60		dB	(2,3,4)
Feedthrough	- 60				(2,3)
V_{CC} Power Supply Rejection	- 60				(2,3)
Input Series Resistance		750	1.2K	W	(5)
Voltage on Analog Input Pin		ANGND	V_{REF}	V	(6)
Sampling Capacitor	3.0			pF	
DC Input Leakage	± 100	- 300	300	nA	(8)

NOTES:

1. An LSB, as used here, has a value of approximately 5 mV.
2. Most parts will meet these values at 25°C, but they are not tested or guaranteed.
3. DC to 100 KHz.
4. Multiplexer break-before-make guaranteed.
5. Resistance from device pin, through internal multiplexer, to sample capacitor.
6. Applying voltage beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions were performed with processor in idle mode.
8. $100 \text{ mV} < V_{IN} < V_{REF} - 100 \text{ mV}$.

6.7.2 AC Characteristics — A/D Converter, 8-bit Mode

Table 14. 8-bit A/D Operating Conditions (1)

Symbol	Description	Min	Max	Units	Notes
T_A	Ambient Temperature	0	70	°C	
V_{CC}	Digital Supply Voltage	4.50	5.50	V	
V_{REF}	Analog Supply Voltage	4.50	5.50	V	(2)
T_{SAM}	Sample Time	1.0		µs	(3)
T_{CONV}	Conversion Time	8.0	15.0	µs	(3)

NOTES:

1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than +0.5 V because V_{REF} supplies both the resistor ladder and the analog portion of the converter and input port pins.
3. Program the AD_TIME register to meet the T_{SAM} and T_{CONV} specifications.

Table 15. 8-bit Mode A/D Characteristics Over Specified Operating Conditions (7)

Parameter	Typical (2)	Min	Max	Units (1)	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	± 1.0	LSBs	
Full-scale Error	± 0.5				
Zero Offset Error	± 0.5				
Nonlinearity		0	± 1.0		
Differential Nonlinearity		- 0.5	+ 0.5		
Channel-to-channel Matching		0	± 1.0		
Repeatability	± 0.25	0			
Temperature Coefficients: Offset Full-scale Differential Nonlinearity	0.003			LSB/°C	
Off Isolation		- 60		dB	(2,3,4)
Feedthrough	- 60				(2,3)
V_{CC} Power Supply Rejection	- 60				(2,3)
Input Series Resistance		750	1.2K	Ω	(5)
Voltage on Analog Input Pin		ANGND	V_{REF}	V	(6)
Sampling Capacitor	3.0			pF	
DC Input Leakage	±100	- 300	300	nA	(8)

NOTES:

1. An LSB, as used here, has a value of approximately 20 mV.
2. Most parts will need these values at 25°C, but they are not tested or guaranteed.
3. DC to 100 KHz.
4. Multiplexer break-before-make guaranteed.
5. Resistance from device pin, through internal multiplexer, to sample capacitor.
6. Applying voltage beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions were performed with processor in idle mode.
8. $100\text{ mV} < V_{IN} < V_{REF} - 100\text{ mV}$.

6.8 External Clock Drive

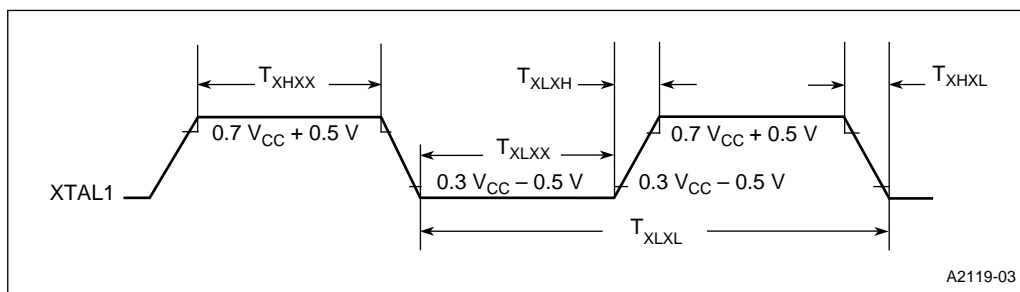
Table 16. External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency (F_{XTAL1})	10	40 (1)	MHz (2)
T_{XLXL}	Oscillator Period (T_{XTAL1})	25	100	ns
T_{XHXX}	High Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXX}	Low Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

NOTES:

- 20 MHz is the maximum input frequency when using an external crystal oscillator; however, 40 MHz can be applied with an external clock source.
- These values represent PLL-bypass mode.

Figure 11. External Clock Drive Waveforms



6.9 Test Output Waveforms

Figure 12. AC Testing Output Waveforms

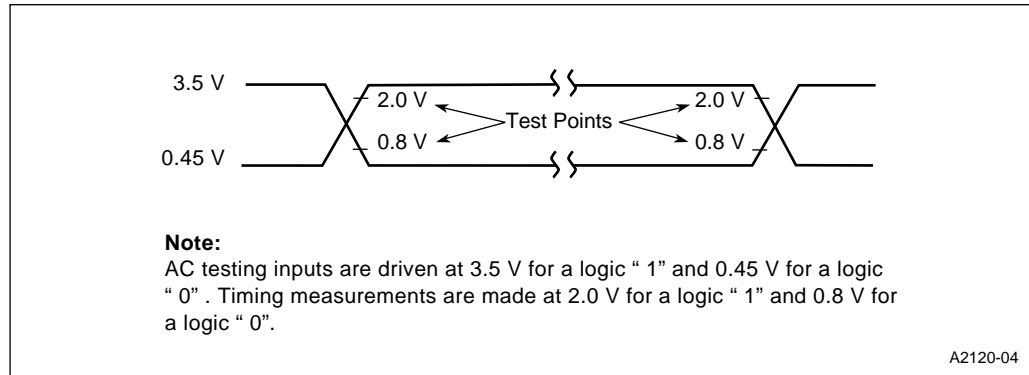
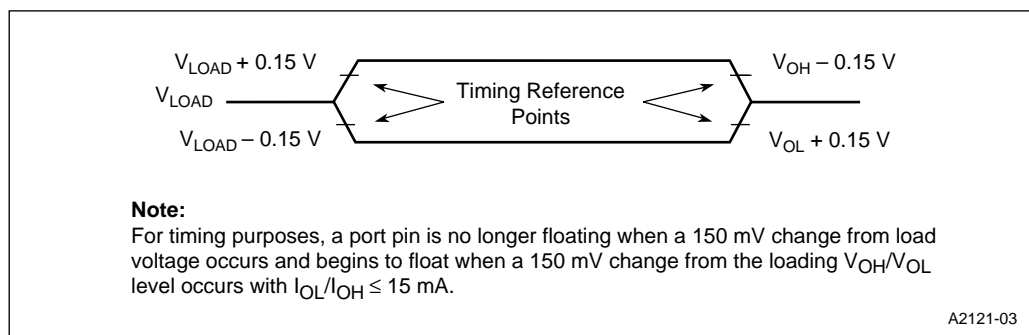


Figure 13. Float Waveforms During 5.0 Volt Testing



7.0 Thermal Characteristics

All thermal impedance data is approximate for static air conditions at 1 W of power dissipation. Values change depending on operating conditions and the application. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology. The *Components Quality and Reliability Handbook* (order number 210997) provides quality and reliability information.

Table 17. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
160-pin QFP	34°C/W	5°C/W

7.1 80C196EA Errata

The 80C196EA may contain design defects or errors known as errata. Characterized errata that may cause the 80C196EA's behavior to deviate from published specifications are documented in a specification update. Specification updates can be obtained from your local Intel sales office or from the World Wide Web (www.intel.com).

8.0 DataSheet Revision History

This is the -001 version of the "80C196EA - Commercial" datasheet.