dsPIC30F601X

dsPIC30F601X Rev. A3 Silicon Errata

dsPIC30F601X (Rev. A3) Silicon Errata

The dsPIC30F601X (Rev. A3) samples you have received have been tested for an operational voltage, VDD, in the range of 4.5 to 5.5 volts. These samples were found to conform to the specifications and functionality described in the following documents:

- DS70030**E** - dsPIC30F Programmer's Reference Manual
- DS70117**B** - dsPIC30F6011, dsPIC30F6012, dsPIC30F6013, dsPIC30F6014 Data Sheet
- DS70119**B** - dsPIC30F6010 Data Sheet
- DS70046**B** - dsPIC30F Family Reference Manual

The exceptions to the specifications in the documents listed above are described in this section. The specific devices for which these exceptions are described are listed below:

- 30F6010
- 30F6011
- 30F6012
- 30F6013
- 30F6014

The errata in this document apply to all devices marked with year codes and week codes prior to "04" and "06", respectively.

The errata described in this section will be fixed in future revisions of dsPIC30F601X silicon.

Silicon Errata Summary

The following list summarizes the errata described in further detail through the remainder of this document:

1. Run-Time Self Programming (RTSP)

   RTSP operations may not be performed on the Program Memory. RTSP operations can however be performed on the on-chip Data EEPROM.

2. Data EEPROM

   Data EEPROM is operational below 24 MIPS.

3. Unsigned MAC

   The unsigned integer mode for the MAC-type DSP instructions does not function as specified.

4. Y-Space Data Dependency

   When an instruction that writes to a location in the address range of Y-data memory is immediately followed by a MAC-type DSP instruction that reads a location also resident in Y-data memory, the operations will not be performed as specified.

5. IPC2 SFR Write Sequence

   A specific write sequence for IPC2 (Interrupt Priority Control 2) SFR is required.

6. Catastrophic Overflow Traps

   When a catastrophic overflow of any of the accumulators causes an arithmetic (math) error trap, the Overflow status bits need to be cleared to exit the trap handler.

7. Interrupting a REPEAT Loop

   When a REPEAT loop is interrupted by two or more interrupts in a nested fashion an Address Error Trap may be caused.

8. 32-bit General Purpose Timers

   The 32-bit General-Purpose Timers do not function as specified for prescaler ratios other than 1:1.

9. 12-bit 100 Ksps A/D Converter

   The 12-bit A/D converter scans one channel less than that specified when configured to perform channel scanning on MUX A inputs and alternately converting a fixed MUX B input simultaneously.

10. 10-bit A/D Converter – Sequential Sampling

    Sampling multiple channels sequentially using any conversion trigger other than the auto-convert feature requires SAMC bits to be non-zero.

11. Data Converter Interface

    In Slave mode, the DCI module does not function correctly when data communication is configured to start one serial clock after the frame synchronization pulse.

12. Quadrature Encoder Interface – Index Pulse

    The Reset On Index Pulse Mode does not work.

13. Motor Control PWM – Time-base Prescaler

    The Motor Control PWM Time base prescaler options – 1:4, 1:16 and 1:64 may produce unexpected results when used to generate center-aligned PWM pulses.

14. Motor Control PWM - Output Override

    The output override function of the PWM module, controlled by the OVDCON register and the OSYNC (PWMCON2<1>) bit, produces unexpected results in certain cases when the module is used in Complementary mode.

15. Power-down Current, IPD

    The device exhibits IPD less than 0.1 μA. However, certain workarounds are required to achieve IPD in this range.

The following sections will describe the errata and work around to these errata, where they may apply.

1. Module: Program Memory – RTSP

For this revision of silicon, run-time self-programming (RTSP) operations should not be performed on the User Program Memory and Configuration Fuse bits. Configuration Fuse bits may be programmed within the MPLAB® IDE using a device programmer, for example, MPLAB ICD 2.

Note that the on-chip Data EEPROM can be self-programmed at run-time.

Work around

None

2. Module: Data EEPROM – Speed

At device throughput greater than 24 MIPS, Table Read instructions (`TBLRDL/TBLRDH`) and instructions that use Program Space Visibility (PSV) do not function correctly when reading data from Data EEPROM.

Work around

When reading data from Data EEPROM, the application should perform a clock-switch operation to lower the frequency of the system clock so that the throughput is less than 24 MIPS. This may be easily performed at any time via the Oscillator Postscaler bits, POST (OSCCON<7:6>), that allow the application to divide the system clock down by a factor of 4, 16 or 64.

3. Module: CPU – Unsigned `MAC`

The US (CORCON<12>) bit controls whether `MAC`-type DSP instructions operate in signed or unsigned mode. The device defaults to a signed mode on power-up (US = `0`).

For this revision of silicon, `MAC`-type DSP instructions do not function as specified in unsigned mode (US = `1`). Also, for this revision, the US bit will always read as '`0`'.

Work around

Ensure that the US bit is not set by the application. In order to perform unsigned integer multiplications, use the MCU Multiply instruction, `MUL.UU`.

4. Module: Y-Space Data Dependency

When an instruction that writes to a location in the address range of Y-data memory (addresses between 0x1800 and 0x27FF) is immediately followed by a MAC-type DSP instruction that reads a location also resident in Y-data memory, the two operations will not be executed as specified. This is demonstrated in Example 1.

EXAMPLE 1:

```
    MOV     #0x090A, W0     ;Load address > =
                            ;0x900 into W0
    MOV     #0x09B0, W10    ;Load address >=
                            ;0x900 into W10
    MOV     W2, [W0++]      ;Perform indirect
                            ;write via W0 to
                            ;address >= 0x900
    MAC     W4*W5, A, [W10]+=2, W5 ;Perform
                            ;read operation
                            ;using Y-AGU
:Unexpected Results!
```

Work around

Work around 1:

Insert a NOP between the two instructions as shown in Example 2.

EXAMPLE 2:

```
    MOV     #0x090A, W0     ;Load address > =
                            ;0x900 into W0
    MOV     #0x09B0, W10    ;Load address >=
                            ;0x900 into W10
    MOV     W2, [W0++]      ;Perform indirect
                            ;write via W0 to
                            ;address >= 0x900
    NOP                     ;No operation
    MAC     W4*W5, A, [W10]+=2, W5 ;Perform
                            ;read operation
                            ;using Y-AGU
:Correct Results!
```

Work around 2:

If Work around #1 is not feasible due to application real-time constraints, the user may take precautions to ensure that a write operation performed on a location in Y-data memory is not immediately followed by a DSP MAC-type instruction that performs a read operation of a location in Y-data memory.

5. Module: Interrupt Controller

A specific write sequence for IPC2 (Interrupt Priority Control 2) SFR is required to prevent possible data corruption in the IEC2 (Interrupt Enable Control 2) SFR. Interrupts must be disabled during this IPC2 SFR write sequence.

Work around

An example of this write sequence is shown in Example 3.

EXAMPLE 3:

```
mov  #IPC2, w0      ;Point w0 to IPC2
mov  #0x4444, w1    ;Write data to go to IPC2
disi #2             ;Disable interrupts for
                    ;next two cycles
mov  w1, IPC2       ;Write the data to IPC2
mov  #IPC2, w0      ;Target w1 to keep IPC2
                    ;address on bus
```

When coding in C, the write sequence shown above can be implemented using inline assembly instructions. The equivalent write sequence using the C30 compiler is shown in Example 4.

EXAMPLE 4:

```
asm volatile(   "push.d   w0\n\t"
                "mov  #IPC2,w0\n\t"
                "mov  #0x4444,w1\n\t"
                "disi #2\n\t"
                "mov  w1, IPC2\n\t"
                "mov  #IPC2, w0\n\t"
                "pop.d  w0");
//Note: There are no commas between
//      the quoted strings in the code
//      segment above.
```

6. Module: Interrupt Controller – Traps

Catastrophic Accumulator Overflow Traps are enabled as follows:

- COVTE (INTCON1<8>) = 1
- SATA/SATB (CORCON <7/6>) = 0

A carry generated out of bit 39 in the accumulator causes a catastrophic overflow of the accumulator since the sign-bit has been destroyed. If a Math Error trap handler has been defined, the processor will vector to the Math Error trap handler upon a catastrophic overflow.

If the respective accumulator overflow status bit, OA or OB (SR<15/14>), is not cleared within the trap handler routine prior to exiting the trap handler routine, the processor will immediately re-enter the trap handler routine.

Work around

If a Math Error Trap occurs due to a catastrophic accumulator overflow, the overflow status flags, OA and/or OB (SR<15/14>), should be cleared within the trap handler routine. Subsequently, the MATHERR (INTCON1<4>) flag bit should be cleared within the trap handler prior to executing the RETFIE instruction.

Since the OA and OB bits are read-only bits, it will be necessary to execute a dummy accumulator-based instruction within the trap service routine in order to clear these status bits. and eventually clear the MATHERR trap flag. This is shown in Example 5.

EXAMPLE 5:

```
.global    __MathError
__MathError:   BTSC    SR, #OA
               CLR     A
               BTSC    SR, #OB
               CLR     B
               BCLR    INTCON1, #MATHERR
               RETFIE
```

7. Module: Interrupting a REPEAT Loop

When interrupt nesting is enabled (or NSTDIS(INTCON1<15>) bit is '0'), the following sequence of events will lead to an Address Error Trap:

1. REPEAT-loop is active
2. An interrupt is generated during the execution of the REPEAT-loop.
3. The CPU executes the Interrupt Service Routine (ISR) of the source causing the interrupt.
4. Within the ISR, when the CPU is executing the first instruction cycle of the 3-cycle RETFIE (Return-from-interrupt) instruction, a second interrupt is generated by a source with a higher interrupt priority.

Work around

Processing of Interrupt Service Routines should be disabled while the RETFIE instruction is being executed. This may be accomplished in two different ways:

1. Place a DISI instruction immediately before the RETFIE instruction in all interrupt service routines of interrupt sources that may be interrupted by other higher priority interrupt sources (with priority levels 1 through 6). This is shown in Example 6 in the Timer1 ISR. In this example, a DISI instruction inhibits level 1 through level 6 interrupts for 2 instruction cycles, while the RETFIE instruction is executed.

EXAMPLE 6:

```
__T1Interrupt:     ;Timer1 ISR
    PUSH    W0     ;This line optional
    .......
    BCLR    IFS0, #T1IF
    POP     W0     ;This line optional
    DISI    #1
    RETFIE     ;Another interrupt occurs
               ;here and it is processed
               ;correctly
```

2. Immediately prior to executing the RETFIE instruction, increase the CPU priority level by modifying the IPL<2:0> (SR<7:5>) bits to '111' as shown in Example 7. This will disable all interrupts between priority levels 1 through 7.

EXAMPLE 7:

```
__T1Interrupt:     ;Timer1 ISR
    PUSH    W0
    .......
    BCLR    IFS0, #T1IF
    MOV.B   #0xE0, W0
    MOV.B   WREG, SR
    POP     W0
    RETFIE     ;Another interrupt occurs
               ;here and it is processed
               ;correctly
```

8. Module: 32-bit General Purpose Timers

Pairs of 16-bit timers may be combined to form 32-bit timers. For example, Timer2 and Timer3 are combined into a single 32-bit timer. For this release of silicon, when a 32-bit timer is prescaled by ratios other than 1:1, unexpected results may occur.

Work around

None. The application may only use the 1:1 prescaler for 32-bit timers.

9. Module: 12-bit 100 Ksps A/D Converter

Input Channel Scanning allows the A/D converter to acquire and convert signals on a selected set of "MUX A" input pins in sequence. This function is controlled by the CSCNA (ADCON2<11>) bit and the ADCSSL SFR.

The ALTS (ADCON2<0>) bit, when set, allows the A/D converter to alternately acquire and convert a "MUX A" input signal and a "MUX B" input signal in an interleaved fashion.

When both CSCNA and ALTS are set, the A/D module should scan MUX A input pins while alternating with a fixed MUX B input pin. However, for this release of silicon, when both features are enabled simultaneously, the last input pin enabled for channel scanning in the ADCSSL SFR, is not scanned. Thus, the A/D converter converts one channel less than the number specified in the scan sequence. Note that this erratum does not affect devices that have a 10-bit 500 Ksps A/D converter.

Work around

The user may enable an extra ("dummy") input pin in the channel-scanning sequence. For example, if it is desirable to scan pins AN3, AN4 and AN5 on the set of MUX A inputs while interleaving conversion from AN6 on the MUX B input, the user may configure the A/D converter as follows:

- ADCON2 = 0x041D
- ADCHS = 0x0600
- ADCSSL = 0x8038

For the configuration above, AN15 is the dummy input that will not be scanned. On the A/D interrupt, the A/D buffer will contain conversions from the following pins in sequence:

- ADCBUF0 = AN3
- ADCBUF1 = AN6
- ADCBUF2 = AN4
- ADCBUF3 = AN6
- ADCBUF4 = AN5
- ADCBUF5 = AN6
- ADCBUF6 = AN3
- ADCBUF7 = AN6

10. Module: 10-bit A/D Converter – Sequential Samping

Sampling multiple channels sequentially using any conversion trigger source other than the auto-convert feature requires SAMC bits to be non-zero. Thus, if the following conditions are all satisfied, the module may not operate as specified:

- Multiple S/H channels are sampled sequentially

  CHPS(ADCON2<9:8>) is not equal to '00' and SIMSAM(ADCON1<3>) = 0
- Auto-convert option is not chosen as the conversion trigger

  SSRC(ADCON1<7:5>) is not equal to '111'
- SAMC(ADCON3<12:8>) is equal to '00000'

Work around

Set the value of the SAMC bits to anything other than '00000'. The module will now operate as specified.

11. Module: Data Converter Interface – Slave Mode

The Data Converter Interface (DCI) module does not function correctly in Slave mode when the following conditions are true:

- The DCI module is configured to transmit/ receive one serial clock (bit clock) after the frame synchronization pulse, DJST(DCICON1<5>) = 0.
- The frame length chosen is longer than 1 word, COFSG(DCICON2<8:5>) > 0000.

Work around

The following work around may be applied to enable DCI communication in Slave mode when it is configured to transmit one serial clock after the frame synchronization pulse is received in a multi-word frame:

1. Set the DJST bit to '1'.
2. Enable an additional time slot immediately following each time slot intended for communication.
3. Enable an additional transmit/receive buffer word (modify COFSG bits) or an additional bit per word (modify WS) for each time slot intended for communication.
4. Shift the data word by 1 bit to the right and load the transmit buffer word(s), such that the LS Bit of the original data word to be transmitted is loaded into the additionally enabled bit of the transmit buffer register, TXBUFn, or the MS bit of the additionally enabled transmit buffer, TXBUFn+1.

This work around is now demonstrated by an example.

Assume, the application needs the DCI module to act as a Slave transmitting 1 serial clock after the frame synchronization pulse is received. Further, assume that the application needs to transmit 16-bit data word on Time Slot 0 and the communication is over a 256*Fs channel. In order to reduce interrupt frequency we enable all 4 transmit buffers. The DCI module SFRs should be initialized as follows before being enabled:

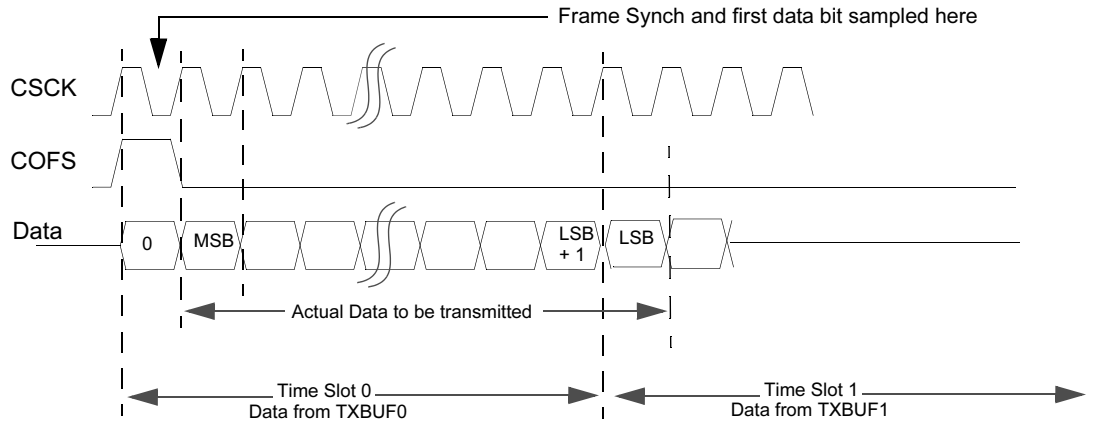
- DCICON1 = 0x0720, DCICON2 = 0x0DEF DCICON3 = 0x0000, TSCON = RSCON = 0x0003

EXAMPLE 8:

```
BCLR    SR, #C
MOV     My1stTxDataWord, W0
RRC     W0, W0
RRC     W1, W1
MOV     W0, TXBUF0
MOV     W1, TXBUF1
MOV     My2ndTxDataWord, W0
RRC     W0, W0
RRC     W1, W1
MOV     W0, TXBUF2
MOV     W1, TXBUF3
```

An example of loading the DCI Transmit buffers for the configuration above is shown in Example 8. A timing diagram in Figure 1 illustrates the various signals for this example. A similar rule may be applied to reading the received data from the RXBUFn SFRs.

FIGURE 1: DCI SLAVE WORK AROUND



Note 1: The Slave mode operation shown in this figure uses the DCI module's operation with DJST = 1, to create a work around for the erratum associated with the DCI module when DJST = 0.

2: Note that the actual data intended for transmission on time slot 0 is now straddled across two time slots – time slot 0 and time slot 1. The MS bit of time slot 0 is '0'. While the MS bit of time slot 1 is actually the LS bit of the data intended for transmission.

3: Data loaded into TXBUF0 contains 15 MS bits of the actual 16-bit data to be transmitted, while the MS bit of TXBUF0 is cleared.

4: Not all serial clock pulses are shown in this timing diagram.

12. Module: QEI – Reset on Index Pulse Mode

For this release of silicon, the QEI module should not be operated in the Reset on Index Pulse mode.

Work around

None

13. Module: Motor Control PWM – Time-base Prescalers

The input clock to the PWM time-base has prescaler options of 1:1, 1:4, 1:16 or 1:64, selected by the PTCKPS (PTCON<3:2>) control bits. In this release of silicon, the options 1:4, 1:16 and 1:64 may produce unexpected results when used to generate center-aligned PWM pulses.

Work around

The prescaler should be set to the 1:1 option (i.e., prescaler should be disabled) in this release of silicon when generating center-aligned PWM pulses.

14. Module: Motor Control PWM – Output Override

The output override function of the PWM module, controlled by the OVDCON register and the OSYNC (PWMCON2<1>) bit, produces unexpected results on the output pins in certain cases when the module is used in Complementary mode. These cases are shown in Table 1. Future releases of silicon will operate as shown in the "Expected Output" columns in Table 1.

Work around

None.

TABLE 1: OUTPUT OVERRIDE: EXPECTED VS. OBSERVED OPERATION

OVDCON	Dead-Time Enabled	Expected Output		Observed Output		Comments
		PWM1H	PWM1L	PWM1H	PWM1L	
0x0100	Yes	Low	PWM	Low	Low	Output on PWM1L pin is shortened by dead-time
0x0200	Yes	PWM	Low	Low	Low	Output on PWM1H pin is shortened by dead-time

Note 1: Other Motor Control PWM SFRs were initialized as follows: PTCON = 0x8002 and PWMCON1 = 0x0011

2: For these settings of OVDCON, the OSYNC (PWMCON<1>) bit should be cleared to '0' for correct eration.

3: Results are shown here for the PWM1H and PWM1L pins only. Similar results will be observed for any other pair of complementary output pins (PWM2H/L, PWM3H/L and PWM4H/L) and any other chosen duty cycle.

15. Module: I_{PD} – Sleep Current

The device exhibits I_{PD} of approximately 100 μA.

Work around

If the application does not use the on-chip A/D converter, it is possible to reduce the I_{PD} to values below 0.1 μA. The following additional measures need to be taken in these circumstances:

1. In the application hardware, the VREF+/RA10 pin (Pin 24) on the dsPIC30F601x device should be connected to the circuit ground (GND).
2. In the application software, the code sequence shown in Example 9 should be executed to bring the device into the power-saving Sleep mode.

EXAMPLE 9:

```
    .include "p30f6014.inc"
    .......
    BCLR    ADCON1, #ADON   ;Required code
    MOV     #0x2000, W0     ;sequence for
    MOV     W0, ADCON2      ;low power-down
    BCLR    PMD1, #ADCMD    ;current.
    PWRSAV  #SLEEP_MODE     ;Device enters
                            ;SLEEP mode here
```

APPENDIX A: REVISION HISTORY

Revision A (12/2003)

Original version of the document.

Revision B (2/2004)

Additional silicon errata were added.

Clarifications/Corrections to dsPIC30F Family Reference Manual were removed.

Revision C (2/2004)

Applicable devices year and week codes were updated.

Revision D (2/2004)

Document status was changed from “Confidential” to “Advance Information”.

Revision E (4/2004)

Errata #13, “Motor Control PWM: Configuration Fuse Bits”, was removed. Added Errata #10.

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