Errata Sheet V1.0

This Errata Sheet refers to:

- The following datasheets:
  AT91M63200 Summary, Rev. 1028DS–05/00
  AT91M63200, Rev. 1028A–10/99
  AT91M43300 Summary, Rev. 1322A–10/99
  AT91M43300, AT91M63200 Electrical Characteristics, Rev. 1090B–05/00
- 176-lead TQFP and 144-ball BGA devices with the following markings:

6. Warning: Additional NWAIT Constraints

When the NWAIT signal is asserted during an external memory access, the following EBI behavior is correct:

– NWAIT is asserted before the first rising edge of the master clock and respects the NWAIT to MCKI rising setup timing as defined in the Electrical Characteristics datasheet.

– NWAIT is sampled inactive and at least one standard wait state remains to be executed, even if NWAIT does not meet the NWAIT to first MCKI rising setup timing (i.e., NWAIT is asserted only on the second rising edge of MCKI).

In these cases, the access is delayed as required by NWAIT and the access operations are correctly performed.

In other cases, the following erroneous behavior occurs:

– 32-bit read accesses are not managed correctly and the first 16-bit data sampling takes into account only the standard wait states. 16- and 8-bit accesses are not affected.

– During write accesses of any type, the NWE rises on the rising edge of the last cycle as defined by the programmed number of wait states. However, NWAIT assertion does affect the length of the total access. Only the NWE pulse length is inaccurate.

At maximum speed, asserting the NWAIT in the first access cycle is not possible, as the sum of the timings “MCKI Falling to Chip Select” and “NWAIT setup to MCKI rising” are generally higher than one half of a clock period. This leads to using at least one standard wait state. However, this is not sufficient except to perform byte or half-word read accesses. Word and write accesses require at least two standard wait states.

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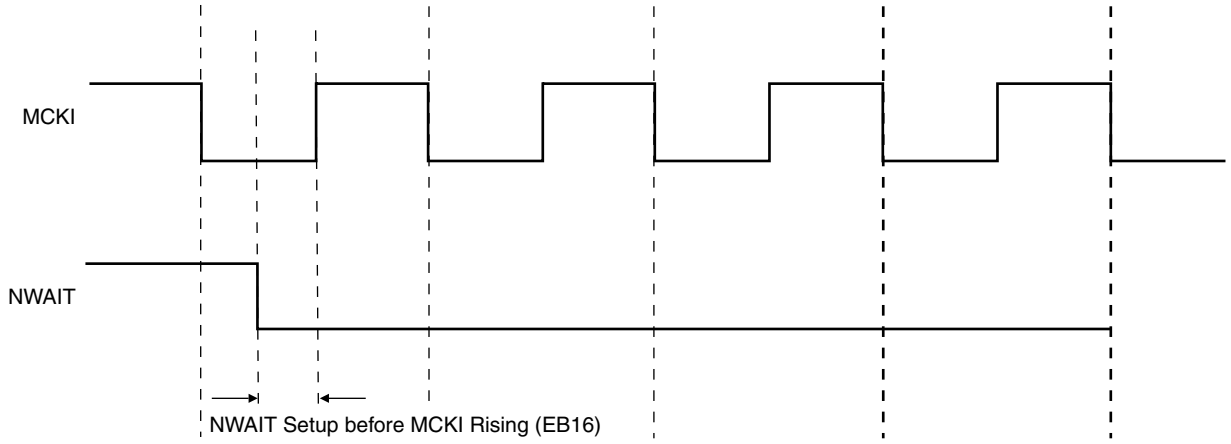
The following waveforms further explain the issue:

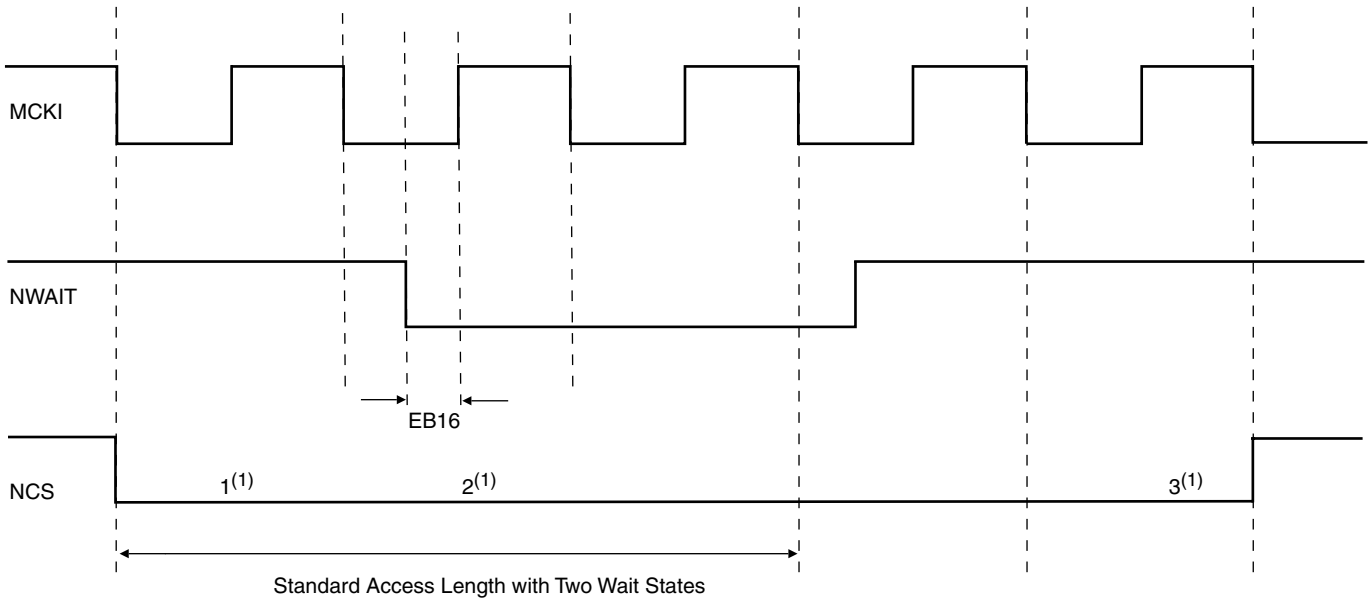
If the NWAIT setup time is satisfied on the first rising edge of MCKI, the behavior is accurate. The EBI operations are not affected when the NWAIT rises.

Figure 1. NWAIT Rising



If the NWAIT setup time is satisfied on the following edges of MCKI and if at least one standard wait state remains to be executed, the behavior is accurate. In the following example, the number of standard wait states is two. The NWAIT setup time on the second rising edge of MCKI must be met.

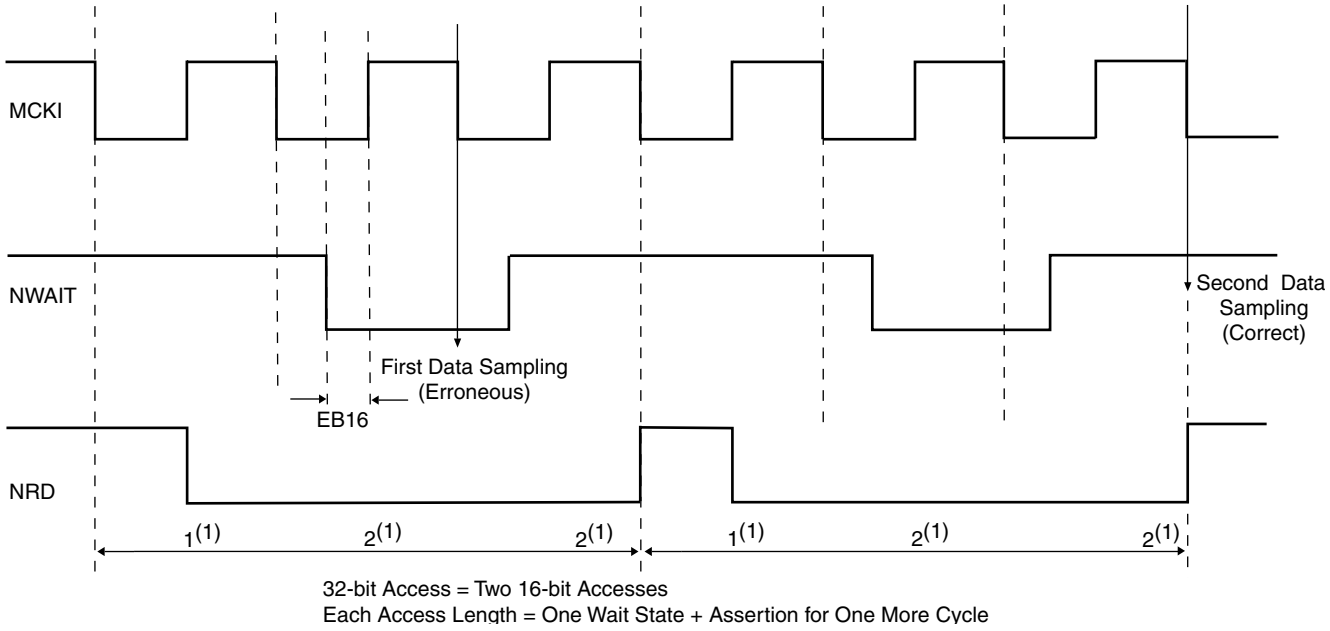
Figure 2. Number of Standard Wait States is Two



Note: 1. These numbers refer to the standard access cycles.

If the first two conditions are not met during a 32-bit read access, the first 16-bit data is read at the end of the standard 16-bit read access. In the following example, the number of standard waits is one. NWAIT assertions do affect both NRD pulse lengths, but first data sampling is not delayed. The second data sampling is correct.

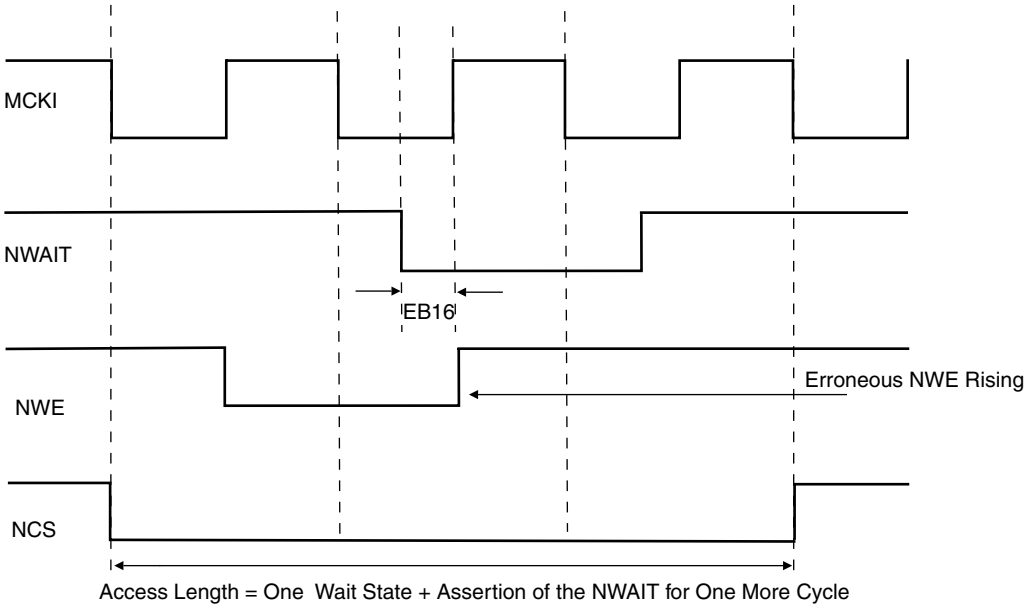
Figure 3. Number of Standard Wait States is One



Note: 1. These numbers refer to the standard access cycles.

If the first two conditions are not met during write accesses, the NWE signal is not affected by the NWAIT assertion. The following example illustrates the number of standard wait states. NWAIT is not asserted during the first cycle, but is asserted at the second and last cycle of the standard access. The access is correctly delayed as the NCS line rises accordingly to the NWAIT assertion. However, the NWE signal waveform is unchanged, and rises too early.

Figure 4. Description of the Number of Standard Wait States



5. **AT91M63200 Datasheet – Page 99**
Problem Fix/Workaround

The reset value of the Status Register does not need to be defined at zero. The status of the SPI is updated at each cycle after the reset and the SPENDRX and SPENDTX bits are set, because the PDC counters are 0.

4. **AT91M63200 Datasheet – Page 141**
Problem Fix/Workaround

The correct description of the CPU bit is:

0 = CPU clock is disabled

1 = CPU clock is enabled

3. **Initializing SPI in Master Mode May Cause a Mode Fault Detection:**
Problem Fix/Workaround

PA26/NPCS0/NSS pin must be pulled up to the V_{DDIO} power supply.

PA26/NPCS0/NSS must be defined as a peripheral pin before programming the SPI peripheral.

2. **SPI in Slave Mode Does not Work**

In transmission, the data to be transmitted (written in SP_TDR) is transferred into the shift register and, consequently, the TDRE bit in SP_SR is set to 1. Though the transfer has not begun, when the following data is written in SP_TDR, it is also transferred into the shift register, crushing the preceding data and setting the bit TDRE to 1.

Problem Fix/Workaround

No workaround available.

1. **Parity Error Bit (PARE) is Set Too Early**

The Parity Error bit on the USART is set as soon as the parity bit is detected. However, the faulty character reception status (RXRDY) is set afterwards, only when the stop bit is detected. This is particularly unfortunate when working in Multi-drop mode, as the PARE bit identifies the Address Bytes. When it is detected, the corresponding character has not yet been transferred in the US_RHR register and, therefore, is not yet available.

Problem Fix/Workaround

No problem fix/workaround to propose.

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