Features

- Utilizes the ARM7TDMI™ ARM Thumb Processor Core
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - Embedded ICE (In-circuit Emulation)
- 2K Bytes (M63200) or 3K Bytes (M43300) Internal RAM
- Fully-programmable External Bus Interface (EBI)
  - Maximum External Address Space of 64M Bytes
  - Up to 8 Chip Selects
  - Software Programmable 8/16-bit External Data Bus
- Multi-processor Interface (M63200 Only)
  - High-performance External Processor Interface
  - 512 x 16-bit Dual-port RAM
- 8-channel Peripheral Data Controller
- 8-level Priority, Individually Maskable, Vectored Interrupt Controller
  - 5 External Interrupts, Including a High-priority, Low-latency Interrupt Request
- 58 Programmable I/O Lines
- 6-channel 16-bit Timer/Counter
  - 6 External Clock Inputs
  - 2 Multi-purpose I/O Pins per Channel
- 3 USARTs
  - 2 Dedicated Peripheral Data Controller (PDC) Channels per USART
  - Support for up to 9-bit Data Transfers
- Master/Slave SPI Interface
  - 2 Dedicated Peripheral Data Controller (PDC) Channels
  - 8- to 16-bit Programmable Data Length
  - 4 External Slave Chip Selects
- Programmable Watchdog Timer
- Power Management Controller (PMC)
  - CPU and Peripherals Can be Deactivated Individually
- IEEE 1149.1 JTAG Boundary-scan on All Active Pins
- Fully Static Operation: 0 Hz to 25 MHz (12 MHz at 1.8V Core, 25 MHz at 2.7V Core)
- 1.8V to 3.6V Core Operating Voltage Range
- 2.7V to 5.5V I/O Operating Voltage Range
- -40°C to +85°C Operating Temperature Range
- AT91M63200 in a 176-lead TQFP Package; AT91M43300 in a 144-ball BGA Package

Description

The AT91M63200 and AT91M43300 are members of the Atmel AT91 16/32-bit microcontroller family which is based on the ARM7TDMI processor core.

This processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications. The AT91 ARM-based MCU family also features Atmel's high-density, in-system programmable, nonvolatile memory technology.

Both products have a direct connection to off-chip memory, including Flash, through the External Bus Interface.

For the AT91M63200, the Multi-processor Interface (MPI) provides a high-performance interface with an external coprocessor or a high bandwidth peripheral.

Both products are manufactured using Atmel's high-density CMOS technology. By combining the ARM7TDMI microcontroller core with on-chip SRAM, a multi-processor interface and a wide range of peripheral functions on a monolithic chip, the AT91M63200 and AT91M43300 provide a highly-flexible and cost-effective solution to many compute-intensive real-time applications.

AT91 ARM® Thumb® Microcontrollers

AT91M63200 AT91M43300

Electrical Characteristics

Rev. 1090B–06/00

Absolute Maximum Ratings*

Operating Temperature (Industrial)	-40°C to +85°C
Voltage on Any Input Pin with Respect to Ground	-0.5V to +5.5V
Maximum Operating Voltage (Core)	3.6V
Maximum Operating Voltage (I/Os)	5.5V
DC Output Current	4 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDCORE}(1)	DC Supply Voltage Core		1.8		3.6	V
V_{DDIO}	DC Supply I/Os	$2.7V \le V_{DDCORE} \le 3.6V$	V_{DDCORE}		V_{DDCORE} + 2.0 or 5.5	V
		$1.8V \le V_{DDCORE} \le 2.7V$	2.7		3.3	
T_A	Ambient Temperature		-40		85	°C
V_{IL}	Low-level Input Voltage		-0.3		0.8	V
V_{IH}	High-level Input Voltage		2		V_{DDIO} + 0.3	V
V_{OL}	Low-level Output Voltage	$2.7 \le V_{DDIO} \le 3.6$; I_O(2) = 2 mA			0.4	V
		$V_{DDCORE} \le V_{DDIO} \le 5.5V$; I_O(2) = 4 mA			0.4	V
V_{OH}	High-level Output Voltage	$2.7 \le V_{DDIO} \le 3.6$; I_O(2) = 2 mA	V_{DDIO} - 0.4			V
		$V_{DDCORE} \le V_{DDIO} \le 5.5V$; I_O(2) = 4 mA	V_{DDIO} - 0.4			V
I_{LEAK}	Input-leakage Current				100	nA
I_{PULL}	Input Pull-up Current				100	µA
I_{CAP}	Input Capacitance				12	pF
I_{SC}	Static Current	$V_{DDIO} = V_{DDCORE} = 3.6V$ MCKI = 0 Hz, NRST = 1		60		µA

Notes: 1. See Table 4.
2. I_O = Output current.

Power Consumption

The values in the following tables are measured values in the operating conditions indicated (i.e. V_{DDIO} = 3.3V, V_{DDCORE} = 3.3V or 1.8V; T = 25°). They represent the power consumption on the V_{DDCORE} power supply.

Table 1. Core Power Consumption

Mode	Conditions	V_{DDCORE} 1.8V	V_{DDCORE} 3.3V	Unit
Reset		0.05	0.41	mW/MHz
Normal	Fetch in ARM mode out of Internal SRAM All peripheral clocks activated	3.1	13.3	
	Fetch in ARM mode out of Internal SRAM All peripheral clocks deactivated	1.8	7.4	
Idle	All peripheral clocks activated	2.0	8.7	
	All peripheral clocks deactivated	0.54	2.4	

Table 2. Core Power Consumption per Peripheral

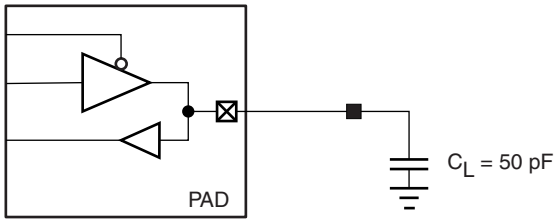
Peripheral	V_{DDCORE} 1.8V	V_{DDCORE} 3.3V	Unit
PIO Controller	0.07	0.32	mW/MHz
Timer Counter channel	0.07	0.28	
Timer Counter Block (3 channels)	0.18	0.75	
USART	0.22	0.99	
SPI	0.22	1.02	

Conditions

Environment Constraints

The output delays are valid for a capacitive load of 50 pF as shown in Figure 1.

Figure 1. Output/Bidir Pad Capacitive Load



Timing Results

The output delays are for a capacitive load of 50 pF as shown in Figure 1.

In order to obtain the timing for other capacitance values, the following equation should be used.

$$t = t_{datasheet} + factor \times (C_{load} - 50pF)$$

Table 3. Derating Factor Due to Capacitive Load Variation

Parameter	Industrial	Units
Factor	0.058	ns/pF

In the tables that follow, the output delays are for industrial conditions only.

Voltage Ranges

Although the core may be supplied between 1.8V and 3.6V, there are two voltage ranges that have been characterized for timing purposes.

These are from 1.8V to 2.2V (core at 2V), and 2.7V to 3.6V (core at 3.3V). Timing values are given for both sets of conditions, as in Table 4.

Table 4. Voltage Ranges for Timing Characterization

	V_{DDCORE}		V_{DDIO}		
Condition	**Minimum**	**Maximum**	**Minimum**	**Maximum**	**Unit**
Core at 2V	1.8	2.2	2.7	3.3	V
Core at 3.3V	2.7	3.6	2.7	5.5	

Clock Waveforms

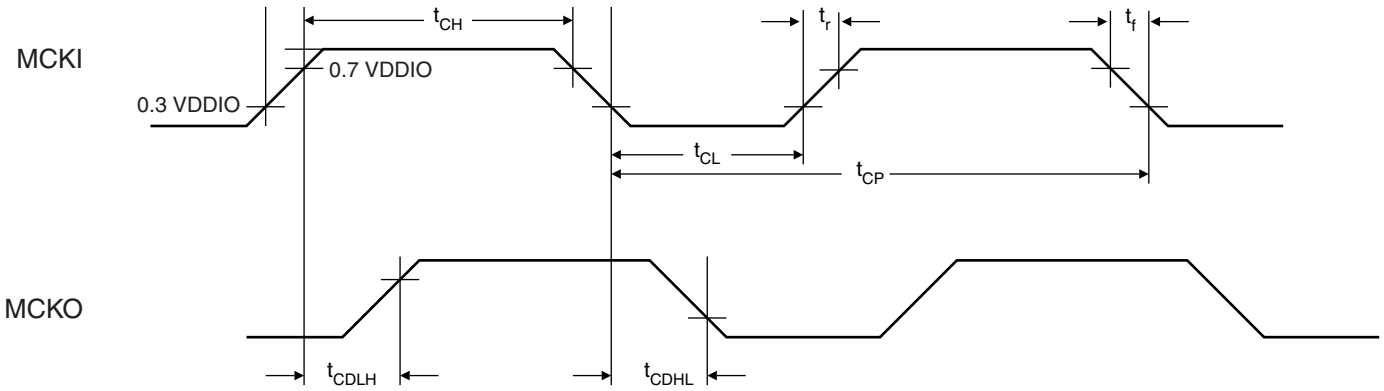
Table 5. Clock Waveform Parameters

Symbol	Parameter	Minimum		Maximum		Units
		Core at 2V	Core at 3.3V	Core at 2V	Core at 3.3V	
$1/(t_{CP})$	Oscillator Frequency			12	25	MHz
t_{CP}	Main Clock Period	83	40			ns
t_{CH}	High Time	TBD	18			
t_{CL}	Low Time	TBD	18			
t_r	Rising Edge			TBD	7	
t_f	Falling Edge			TBD	7	

Table 6. Clock Propagation Times

Symbol	Parameter	Minimum		Maximum		Units
		Core at 2V	Core at 3.3V	Core at 2V	Core at 3.3V	
t_{CDLH}	Rising Edge Propagation Time	TBD	20	TBD	TBD	ns
t_{CDHL}	Falling Edge Propagation Time	TBD	18	TBD	TBD	

Figure 2. Clock Waveform



AC Characteristics

EBI Signals Relative to MCKI

The following tables show timings relative to operating condition limits defined in Table 4. See Figure 3.

Table 7. General Purpose EBI Signals

Symbol	Parameter	Minimum		Maximum		Units
		Core at 2V	Core at 3.3V	Core at 2V	Core at 3.3V	
EBI_1	MCKI Falling to NUB Valid			TBD	20	ns
EBI_2	MCKI Falling to NLB/A0 Valid			TBD	20	ns
EBI_3	MCKI Falling to A7 - A1 Valid			TBD	20	ns
EBI_4	MCKI Falling to A23 - A8 Valid			TBD	20	ns
EBI_5	MCKI Falling to Chip Select	TBD	5	TBD	20	ns
EBI_6	NWAIT Setup before MCKI Rising	TBD	5			ns
EBI_7	NWAIT Hold after MCKI Rising	TBD	4			ns

Table 8. EBI Write Signals

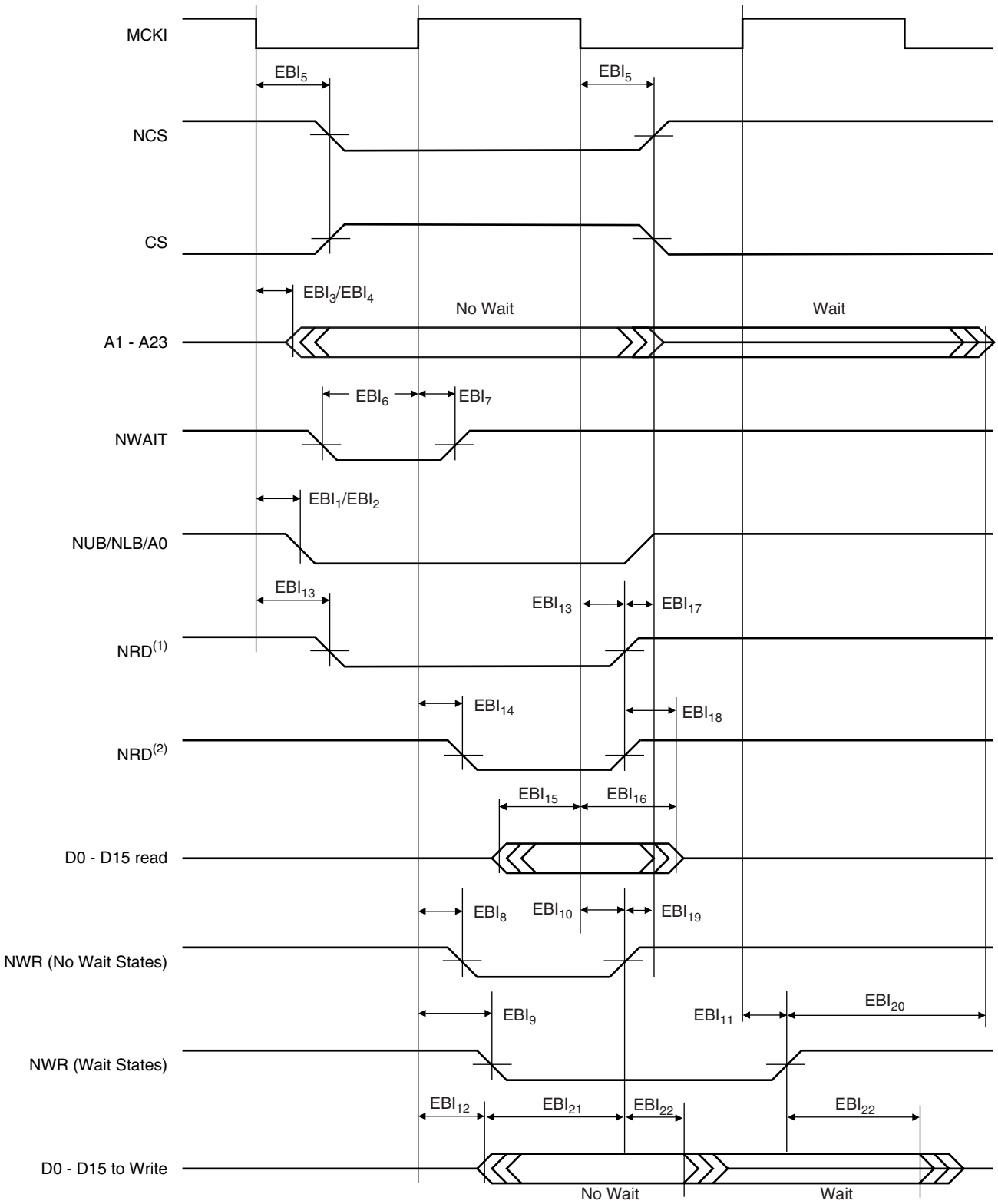
Symbol	Parameter	Minimum		Maximum		Units
		Core at 2V	Core at 3.3V	Core at 2V	Core at 3.3V	
EBI_8	MCKI Rising to NWR Active (No Wait States)			TBD	20	ns
EBI_9	MCKI Rising to NWR Active (Wait States)			TBD	20	ns
EBI_{10}	MCKI Falling to NWR Inactive (No Wait States)			TBD	20	ns
EBI_{11}	MCKI Rising to NWR Inactive (Wait States)			TBD	20	ns
EBI_{12}	MCKI Rising to D0 - D15 Out Valid			TBD	20	ns
EBI_{19}	NWR High to A23 - A1, NUB/NLB/A0, NCS, CS Changes (No Wait States)	TBD	2			ns
EBI_{20}	NWR High to A23 - A1, NCS, CS Changes (Wait States)	$t_{CP/2}$				ns
EBI_{21}	Data Out Valid before NWR High	t_{CH} - 5				ns
EBI_{22}	Data Out Valid after NWR High	$t_{CP/2}$				ns

Table 9. EBI Read Signals

Symbol	Parameter	Minimum		Maximum		Units
		Core at 2V	Core at 3.3V	Core at 2V	Core at 3.3V	
EBI_{13}	MCKI Falling to NRD Valid(1)	TBD	5	TBD	18	ns
EBI_{14}	MCKI Rising to NRD Valid(2)			TBD	20	
EBI_{15}	D0 - D15 in Setup before MCKI Falling	TBD	0			
EBI_{16}	D0 - D15 in Hold after MCKI Falling	TBD	3			
EBI_{17}	NRD High to A23 - A1, NCS, CS Changes	TBD	0			
EBI_{18}	Data Hold after NRD High	TBD	0			

Notes: 1. Early Read Protocol
2. Standard Read Protocol

Figure 3. EBI Signals Relative to MCKI



Notes: 1. Early Read Protocol
2. Standard Read Protocol

Peripheral Signals Relative to MCKI

USART Signals

Table 10. USART Outputs

Symbol	Parameter	Minimum		Maximum		Units
		Core at 2V	Core at 3.3V	Core at 2V	Core at 3.3V	
US_1	MCKI Rising to SCK Output Rising/Falling	TBD	TBD	TBD	25	ns
US_2	MCKI Rising to TXD Toggling	TBD	TBD	TBD	35	ns
US_3	SCK Output Falling to TXD Toggling	TBD	TBD	TBD	10	ns
US_4	SCK Input Falling to TXD Toggling	TBD	TBD	TBD	$2(t_{CP}) + 35$	ns

The inputs can be used synchronously or asynchronously (in relation to MCKI).

For synchronous and asynchronous USART inputs, certain setup/hold constraints must be met. These constraints are shown in Tables 11 and 12 and are represented in Figure 4.

For asynchronous inputs, a minimum pulse-width is necessary as shown in Table 13 and as represented in Figure 4.

Table 11. USART Synchronous Input Setup/Hold Constraints

Symbol	Type of Input	Parameter	Setup	Hold	Units
US_5	Synchronous	RXD Toggling Relative to MCKI Falling	0	5	ns
US_6	Synchronous	SCK Input Rising Relative to MCKI Rising	0	5	ns
US_7	Synchronous	SCK Input Falling Relative to MCKI Rising	0	5	ns

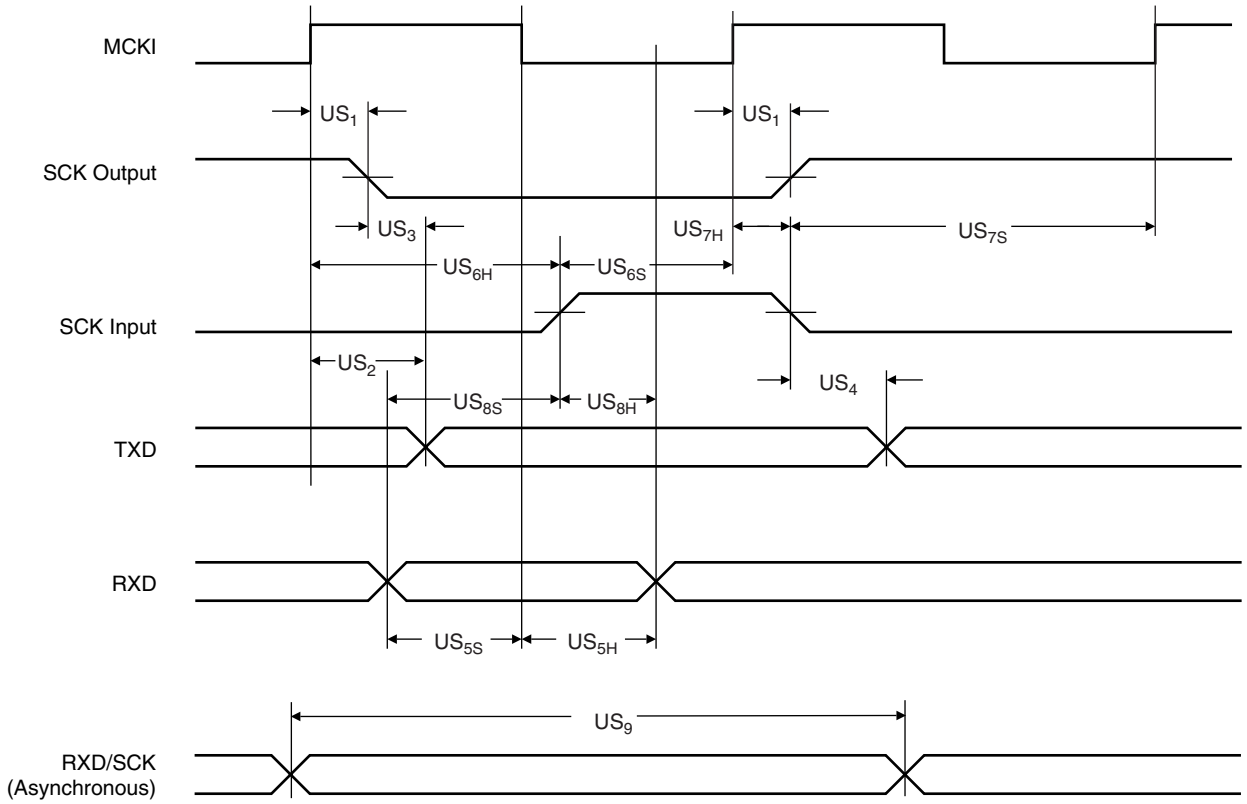
Table 12. USART Asynchronous Input Setup/Hold Constraints

Symbol	Type of Input	Parameter	Setup	Hold	Units
US_8	Asynchronous	RXD Toggling Relative to SCK Input Rising	$t_{CP/2} - 2$	$t_{CP/2} + 2$	ns

Table 13. USART Asynchronous Input Minimum Pulse-width

Symbol	Type of Input	Parameter	Pulse-width	Units
US_9	Asynchronous	RXD/SCK Minimum Pulse-width	$3(t_{CP}/2)$	ns

Figure 4. USART Signals Relative to MCKI

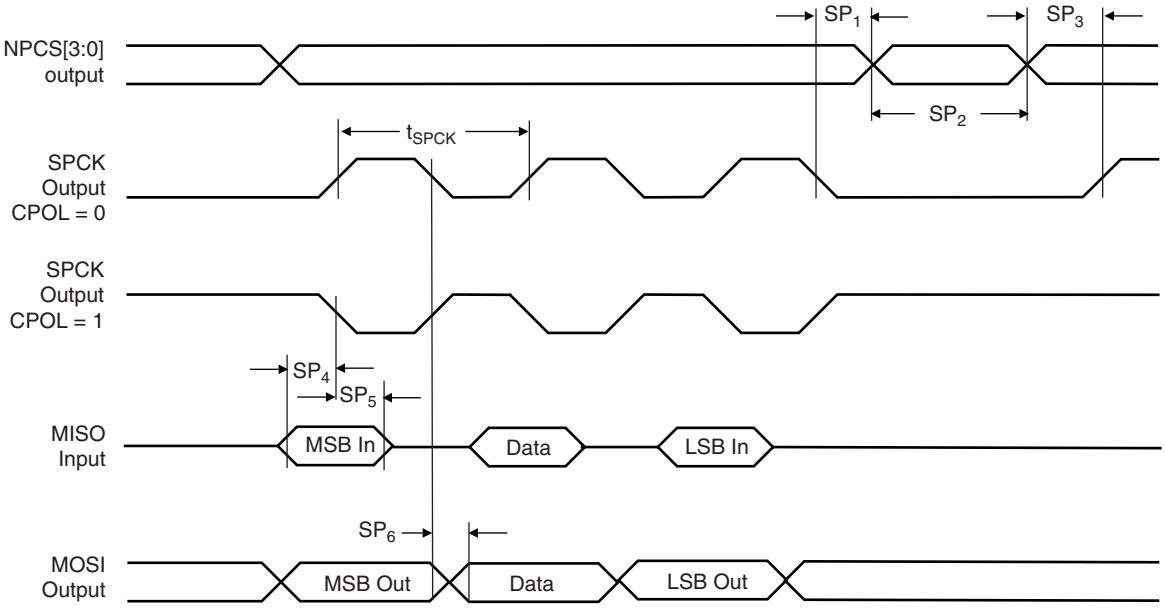


SPI Signals

Table 14. SPI Signals in Master Mode

Symbol	Parameter	Minimum		Maximum		Units
		Core at 2V	Core at 3.3V	Core at 2V	Core at 3.3V	
t_{SPCK}	SPI Operating Period	$4(t_{CP})$		$16320(t_{CP})$		ns
f_{SPCK}	SPI Operating Frequency	$1/16320(t_{CP})$		$1/4(t_{CP})$		GHz
SP_1	Delay before NPCS[3:0]	$4(t_{CP})$		$261120(t_{CP})$		ns
SP_2	Delay between Chip Selects	$6(t_{CP})$		$8160(t_{CP})$		ns
SP_3	Delay before SPCK	$2(t_{CP})$		$8160(t_{CP})$		ns
SP_4	MISO/SPCK Setup Time			TBD	18	ns
SP_5	MISO/SPCK Hold Time	TBD	0			ns
SP_6	MOSI Valid after SPCK Edge			TBD	7	ns

Figure 5. SPI Signals



Timer Counter Signals

Due to internal synchronization of input signals, there is a delay between an input event and a corresponding output event. This delay is 3(t_{CP}) in Waveform Event Detection mode and 4(t_{CP}) in Waveform Total-count Detection mode. In addition there are the following delays relative to MCKI waveforms.

Table 15. Timer Outputs

Symbol	Parameter	Maximum		Units
		Core at 2V	Core at 3.3V	
TC_1	MCKI Rising to TIOA Rising	TBD	22	ns
TC_2	MCKI Rising to TIOA Falling	TBD	22	
TC_3	MCKI Rising to TIOB Rising	TBD	22	
TC_4	MCKI Rising to TIOB Falling	TBD	22	

The inputs can be used synchronously or asynchronously (in relation to MCKI).

For synchronous Timer inputs, certain setup/hold constraints must be met. These constraints are shown in the Table 16 and are represented in Figure 6.

For asynchronous inputs, a minimum pulse-width and a minimum input period are necessary as shown in Tables 17 and 18 and as represented in Figure 6.

Table 16. Synchronous Timer Inputs

Symbol	Type of Input	Parameter	Setup		Hold		Units
			Core at 2V	Core at 3.3V	Core at 2V	Core at 3.3V	
TC_5	Synchronous	TIOA/TIOB Rising Relative to MCKI Rising	TBD	2	TBD	5	ns
TC_6	Synchronous	TIOA/TIOB Falling Relative to MCKI Rising	TBD	2	TBD	5	
TC_7	Synchronous	TCLK Rising Relative to MCKI Rising	TBD	2	TBD	5	
TC_8	Synchronous	TCLK Falling Relative to MCKI Rising	TBD	2	TBD	5	

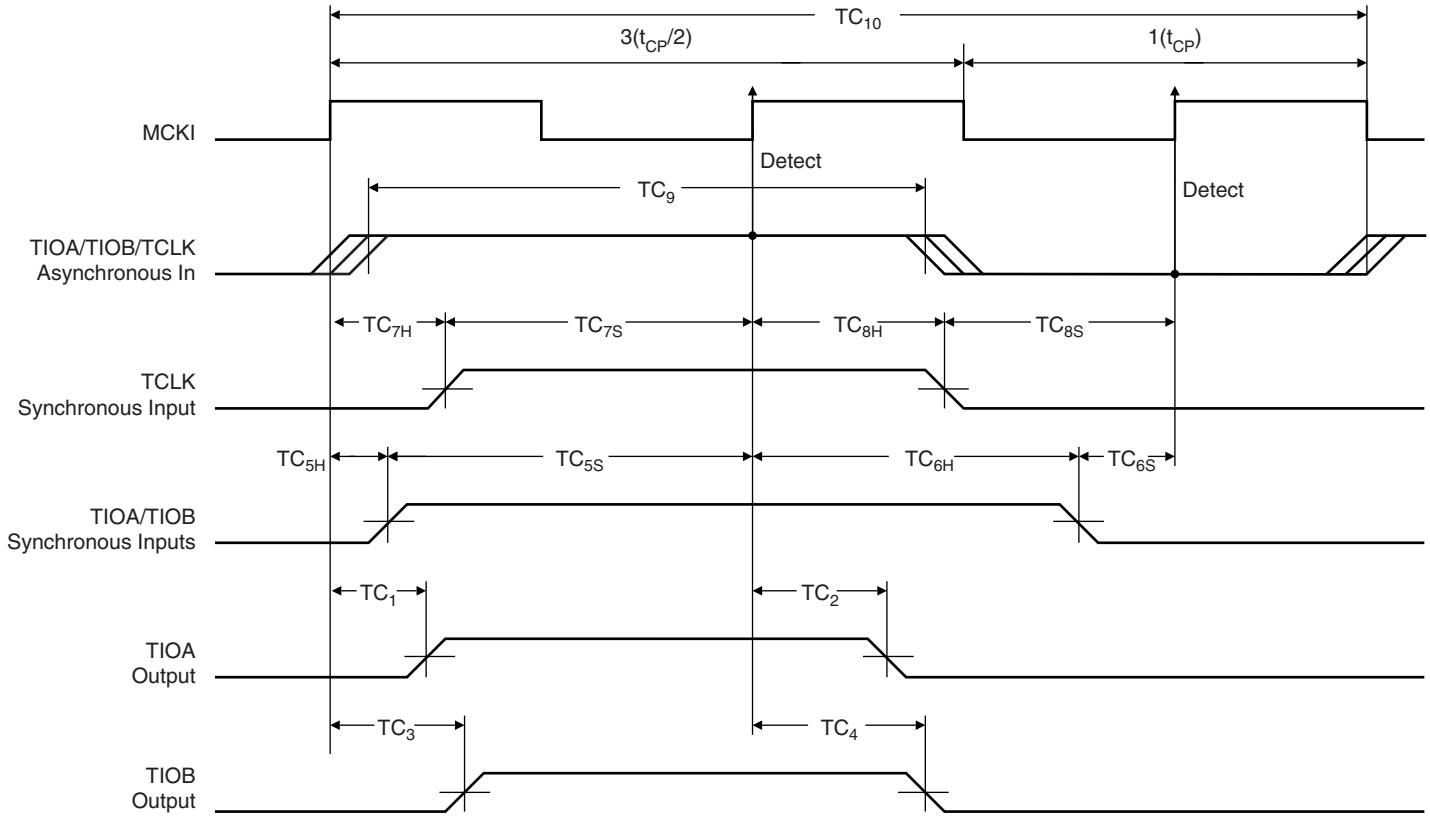
Table 17. Asynchronous Timer Input Minimum Pulse-width

Symbol	Type of Inputs	Parameter	Pulse-width	Units
TC_9	Asynchronous	TCLK/TIOA/TIOB Minimum Pulse-width	3(t_{CP}/2)	ns

Table 18. Asynchronous Timer Input Minimum Input Period

Symbol	Type of Inputs	Parameter	Input Period	Units
TC_{10}	Asynchronous	TCLK/TIOA/TIOB Minimum Input Period	5(t_{CP}/2)	ns

Figure 6. Timer Relative to MCKI

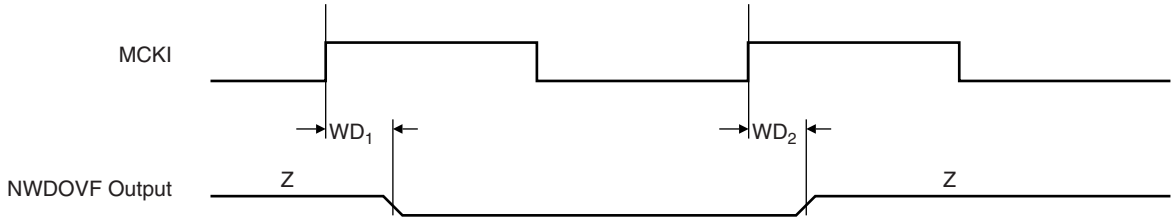


Watchdog Timer Signals

Table 19. Watchdog Timer Outputs

Symbol	Parameter	Maximum		Units
		Core at 2V	Core at 3.3V	
WD_1	MCKI Rising to NWDOVF Rising	TBD	20	ns
WD_2	MCKI Rising to NWDOVF Falling	TBD	20	

Figure 7. Watchdog Signals Relative to MCKI



Reset Signals

Certain setup constraints must be met. These constraints are shown in Table 20 and are represented in Figure 8.

Table 20. Reset Setup Constraints

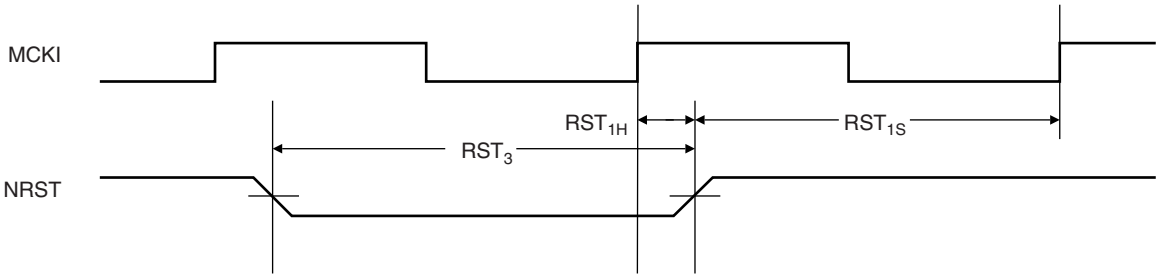
Symbol	Parameter	Setup		Units
		Core at 2V	Core at 3.3V	
RST_1	NRST Rising Related to MCKI Rising	TBD	5	ns

A minimum pulse width is necessary as shown in Table 21 and as represented in Figure 8.

Table 21. Reset Minimum Pulse-width

Symbol	Parameter	Pulse-width	Units
RST_3	NRST Minimum Pulse-width	$10(t_{CP})$	ns

Figure 8. Reset Signals Relative to MCKI



Only the NRST rising edge is synchronized. The falling edge is asynchronous.

Advanced Interrupt Controller Signals

The inputs can be used synchronously or asynchronously (in relation to MCKI).

For synchronous AIC inputs, certain setup/hold constraints must be met. These constraints are shown in Table 22 and are represented in Figure 9.

For asynchronous inputs, a minimum pulse width is necessary as shown in Table 23 and as represented in Figure 9.

Table 22. AIC Synchronous Input Setup/Hold Constraints

Symbol	Type	Parameter	Setup		Hold		Units
			Core at 2V	Core at 3.3V	Core at 2V	Core at 3.3V	
AIC_1	Synchronous	FIQ/IRQ0/IRQ1/IRQ2/IRQ3 Rising. Relative to MCKI Rising	TBD	0	TBD	4	ns
AIC_2	Synchronous	FIQ/IRQ0/IRQ1/IRQ2/IRQ3 Falling. Related to MCKI Rising	TBD	0	TBD	4	ns

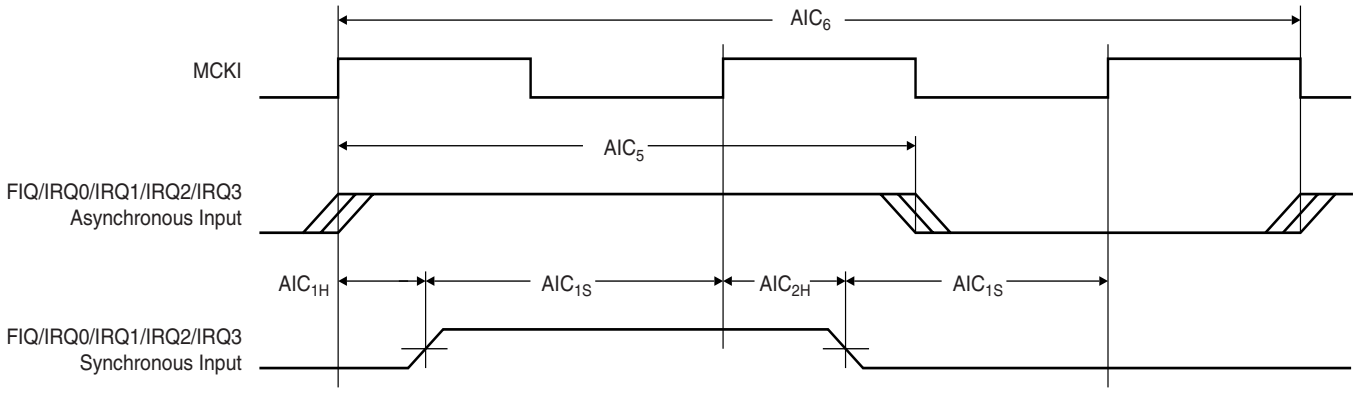
Table 23. AIC Asynchronous Input Minimum Pulse-width

Symbol	Type	Parameter	Pulse-width	Units
AIC_5	Asynchronous	FIQ/IRQ0/IRQ1/IRQ2/IRQ3 Minimum Pulse-width	$3(t_{CP}/2)$	ns

Table 24. AIC Asynchronous Input Minimum Input Period

Symbol	Type	Parameter	Input Period	Units
AIC_6	Asynchronous	AIC Minimum Input Period	$5(t_{CP}/2)$	ns

Figure 9. AIC Signals Relative to MCKI



Parallel I/O Signals

Table 25. PIO Outputs

Symbol	Parameter	Maximum		Units
		Core at 2V	Core at 3.3V	
PIO_1	MCKI Falling to PIO Output Rising	TBD	22	ns
PIO_2	MCKI Falling to PIO Output Falling	TBD	22	ns

The inputs can be used synchronously or asynchronously (in relation to MCKI).

For synchronous PIO inputs, certain setup/hold constraints must be met. These constraints are shown in the Table 26 and are represented in Figure 10.

For asynchronous inputs, a minimum pulse width is necessary as shown in Table 27 and as represented in Figure 10.

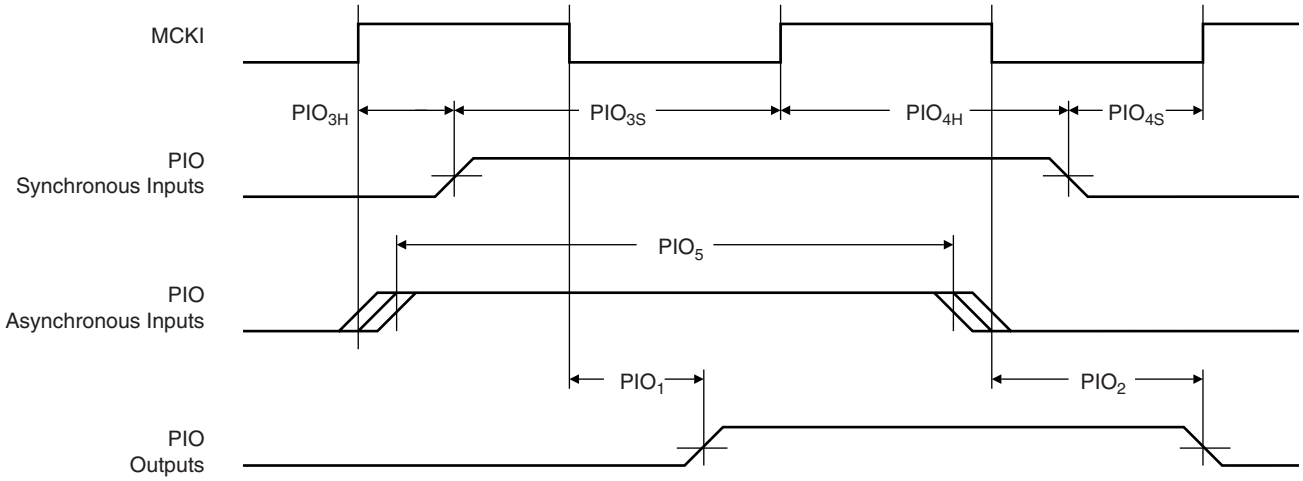
Table 26. PIO Synchronous Input Setup/Hold Constraints

Symbol	Type	Parameter	Setup		Hold		Units
			Core at 2V	Core at 3.3V	Core at 2V	Core at 3.3V	
PIO_3	Synchronous	PIO Input Rising Related to MCKI Rising	TBD	2	TBD	5	ns
PIO_4	Synchronous	PIO Input Falling Related to MCKI Rising	TBD	2	TBD	5	ns

Table 27. PIO Asynchronous Input Minimum Pulse-width

Symbol	Type	Parameter	Pulse-width	Units
PIO_5	Asynchronous	PIO Input Minimum Pulse-width	$3(t_{CP}/2)$	ns

Figure 10. PIO Signals Relative to MCKI



Multi-processor Interface Signals (AT91M63200 Only)

Figure 11. External Arbitration

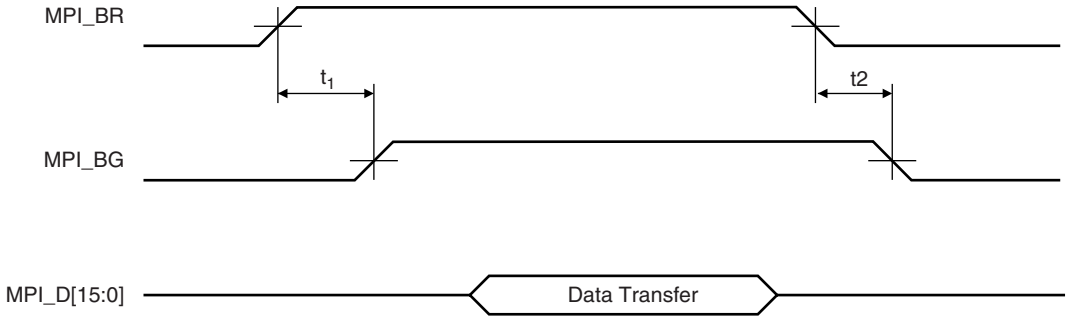


Table 28. External Arbitration

Symbol	Parameter	Minimum		Maximum		Units
		Core at 2V	Core at 3.3V	Core at 2V	Core at 3.3V	
t_1	MPI_BR High to MPI_BG High Delay (30 pf)	t_{CP}		2 x t_{CP} + 12		ns
t_2	MPI_BR Low to MPI_BG Low			TBD	12	

Table 29. MPI Read Access

Symbol	Parameter	Minimum		Maximum		Units
		Core at 2V	Core at 3.3V	Core at 2V	Core at 3.3V	
t_{RC}	Read Cycle Time	TBD	22			ns
t_{AA}	Address Access Time			TBD	22	ns
t_{ACS}	Chip Select Access Time			TBD	22	ns
t_{OE}	Output Enable to Output Valid			TBD	10	ns
t_{LB}, t_{UB}	Byte Select to Output Valid			TBD	10	ns
t_{OH}	Output Hold from Address Change	TBD	0			ns
t_{CLZ}	Chip Select to Output in Low-Z	TBD	0			ns
t_{OLZ}	Output Enable to Output in Low-Z	TBD	0			ns
t_{LBLZ}, t_{UBLZ}	Byte Select to Output in Low-Z	TBD	0			ns
t_{CHZ}	Chip Deselect to Output in High-Z			TBD	7	ns
t_{OHZ}	Output Disable to Output in High-Z			TBD	7	ns
t_{LBHZ}, t_{UBHZ}	Byte Deselect to Output in High-Z			TBD	7	ns

Figure 12. MPI Read Access

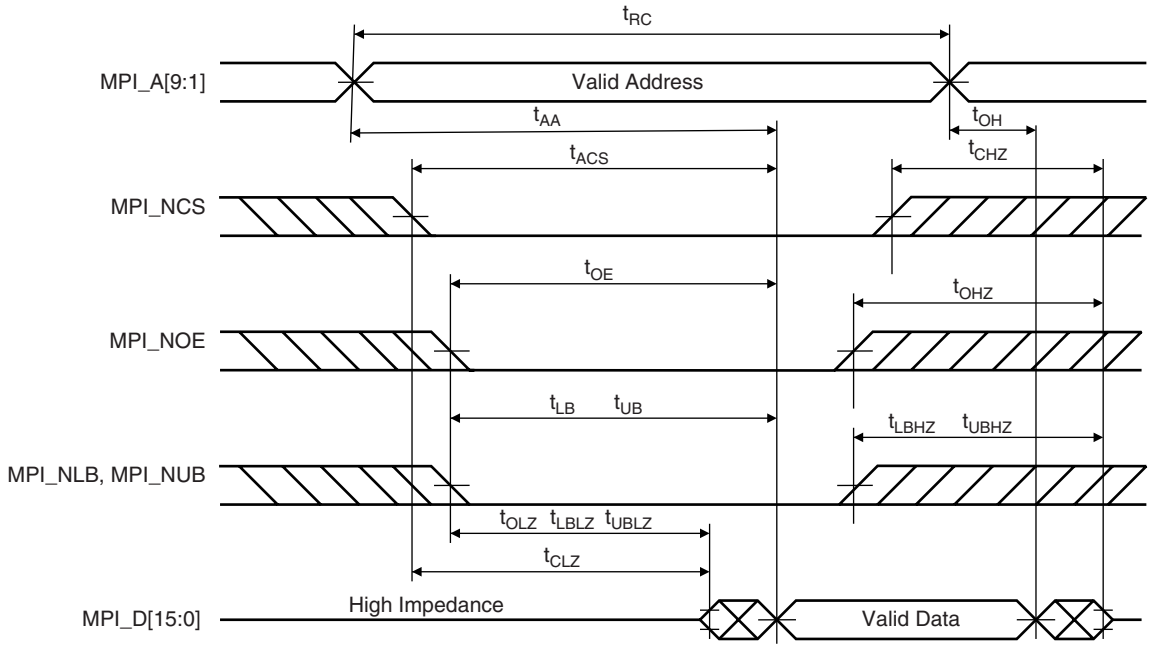


Table 30. MPI Write Access

Symbol	Parameter	Minimum		Maximum		Unit
		Core at 2V	Core at 3.3V	Core at 2V	Core at 3.3V	
t_{WC}	Write Cycle Time	TBD	10			ns
t_{AW}	Address Valid to End of Write	TBD	10			ns
t_{CW}	Chip Select to End of Write	TBD	10			ns
t_{WP}	Write pulse-width	TBD	10			ns
t_{LBW}, t_{UBW}	Byte Select to End of Write	TBD	10			ns
t_{AS}	Address Setup Time	TBD	0			ns
t_{WR}	Write Recovery Time	TBD	0			ns
t_{DW}	Data Valid to End of Write	TBD	10			ns
t_{DH}	Data Hold Time from End of Write	TBD	0			ns
t_{OW}	Write Disable to Output in Low-Z	TBD	10			ns
t_{WHZ}	Write Enable to Output in High-Z			TBD	7	ns

Figure 13. MPI Write Access (MPI_RNW Controlled)

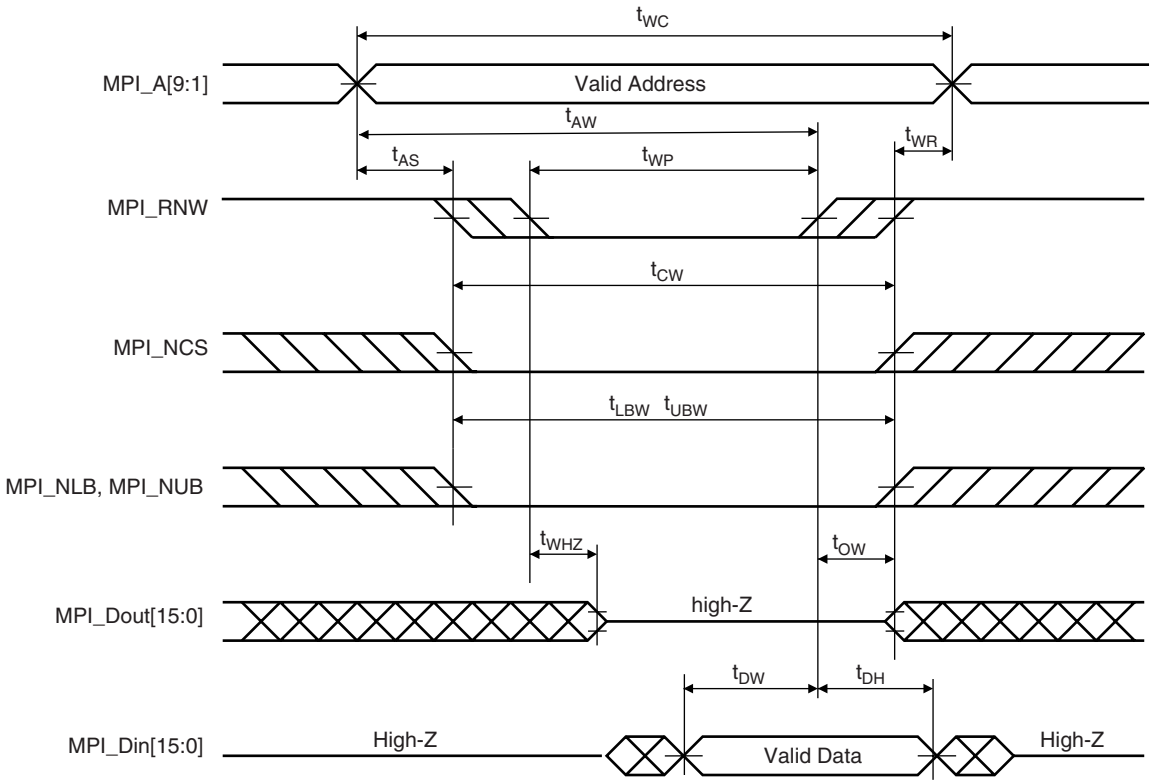


Figure 14. MPI Write Access (MPI_NCS Controlled)

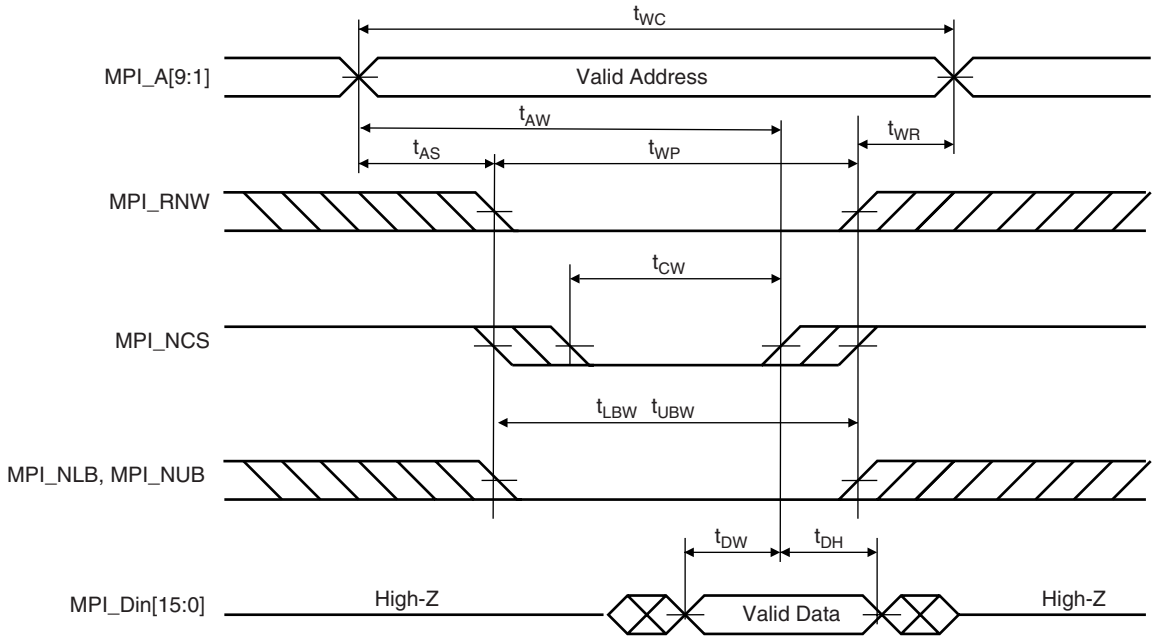
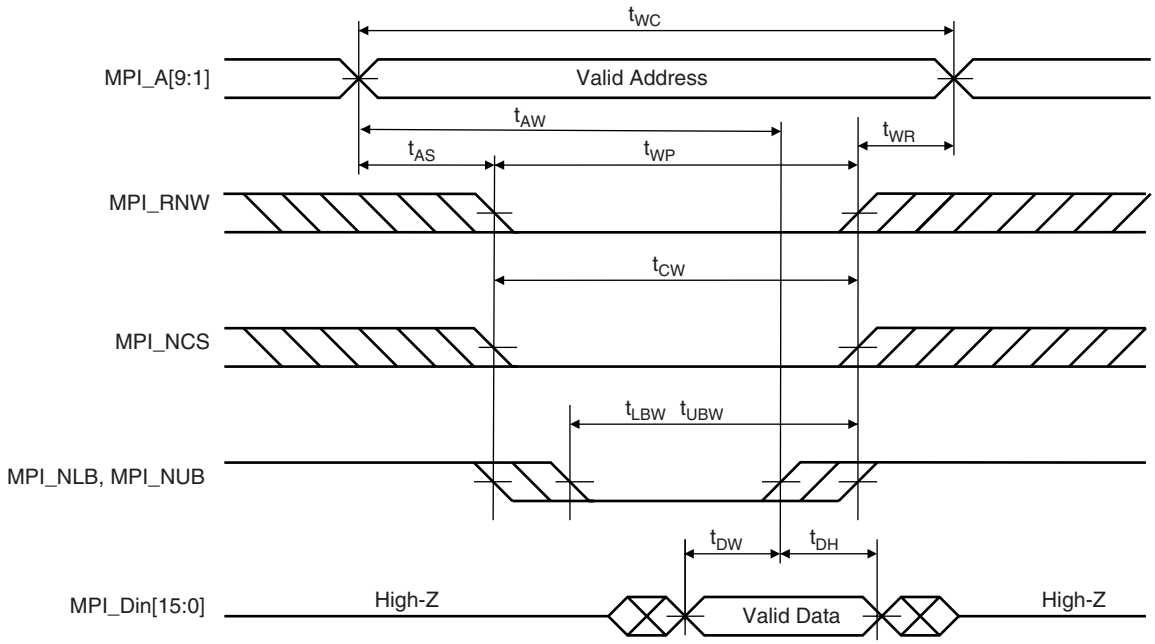


Figure 15. MPI Write Access (MPI_NLB, MPI_NUB Controlled)



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