PIC18F87K90 Family
Silicon Errata and Data Sheet Clarification

The PIC18F87K90 Family devices that you have received conform functionally to the current Device Data Sheet (DS39957**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F87K90 Family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F87K90 Family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A3		
PIC18F65K90	524h	3h		
PIC18F66K90	520h			
PIC18F67K90	510h			
PIC18F85K90	52Ah			
PIC18F86K90	526h			
PIC18F87K90	514h			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC18F6XKXX/8XKXX Family Flash Microcontroller Programming Specification"* (DS39947) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A3		
Analog-to-Digital Converter	A/D Offset	1.	The A/D offset is great than specified in the data sheet's A/D Converter Characteristics table.	X		
Ports	Leakage	2.	I/O port leakage is higher than the D060 spec in the data sheet.	X		
High/Low-Voltage Detect	HLVD Trip	3.	The high-to-low (VDIRMAG = 0) setting of the HLVD may send initial interrupts.	X		
ECCP	Auto-Shutdown	4.	The tri-state setting of the auto-shutdown feature in the enhanced PWM may not successfully drive the pin to tri-state.	X		
EUSART	Synchronous Transmit	5.	When using the Synchronous Transmit mode of the EUSART, at high baud rates, transmitted data may become corrupted.	X		
IPD IDD	Maximum Limit	6.	Maximum current limits may be higher than specified in Table 31-2 of the data sheet.	X		

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

1. Module: Analog-to-Digital Converter (A/D)

The ADC will not meet the Microchip standard ADC specification. ADC may be usable if tested at the user end. The possible issues are high offset error, high DNL error and multiple missing codes. The ADC can be tested and used for relative measurements.

The ADC issues will be fixed in a future revision of this part.

ADC Offset

The ADC may have high offset error up to a maximum of 50 LSB; it can be used if the ADC is calibrated for the offset.

Work around

Method to Calibrate for Offset:

In Single-Ended mode, connect ADC +ve input to ground and take the ADC reading. This will be the offset of the device and can be used to compensate for the subsequent ADC readings on the actual inputs.

Affected Silicon Revisions

A3							
X							

2. Module: Ports

The input leakage will not match the D060 specification in the data sheet. The leakage will meet the 200 nA specification at T_A = 25°C. At T_A = 85°C, the leakage will be up to a max of 2 μA.

Work around

None.

Affected Silicon Revisions

A3							
X							

3. Module: High/Low Voltage Detect (HLVD)

The high-to-low (VDIRMAG = 0) setting of the HLVD may send initial interrupts. High trip points that are close to the intended operating voltage are susceptible to this behavior.

Work around

Select a lower trip voltage that allows consistent start-up, or clear any initial interrupts from the HLVD on start-up.

Affected Silicon Revisions

A3							
X							

4. Module: ECCP

The tri-state setting of the auto-shutdown feature in the enhanced PWM may not successfully drive the pin to tri-state. The pin will remain an output and should not be driven externally. All tri-state settings will be affected.

Work around

None.

Affected Silicon Revisions

A3							
X							

5. Module: EUSART

When using the Synchronous Transmit mode of the EUSART, at high baud rates, transmitted data may become corrupted. One or more bits of the intended transmit message may be incorrect.

Work around

Since this problem is related to the baud rate used, a fixed delay added before loading the TXREGx may not be a reliable work around. Lower the baud rate until no errors occur, or when loading the TXREGx, check that the TRMT bit inside of the TXSTAx register is set instead of checking the TXxIF bit.The following code can be used:

```
while(!TXSTAxbits.TRMT);
// wait to load TXREGx until TRMT is set
```

Affected Silicon Revisions

A3							
X							

6. Module: IPD and IDD

The IPD and IDD limits will not match the data sheet. The values, in bold in Table 31-2, reflect the updated silicon maximum limits.

TABLE 31-2: DC CHARACTERISTICS: POWER-DOWN AND SUPPLY CURRENT PIC18F87K90 FAMILY (INDUSTRIAL)

PIC18F87K90 Family (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Power-Down Current (IPD) Sleep Mode						
	PIC18FXXK90	10	500	nA	-40°C	VDD = 1.8V, Regulator Disabled	
		20	500	nA	+25°C		
		120	600	nA	+60°C		
		630	**2000**	nA	+85°C		
	PIC18FXXK90	50	700	nA	-40°C	VDD = 3.3V, Regulator Disabled	
		60	**900**	nA	+25°C		
		170	**1100**	nA	+60°C		
		700	**5000**	nA	+85°C		
	PIC18FXXK90	350	1300	nA	-40°C	VDD = 5V, Regulator Enabled	
		400	1400	nA	+25°C		
		550	1500	nA	+60°C		
		1350	4000	nA	+85°C		
	Supply Current (IDD)						
	PIC18FXXK90	3.7	8.5	µA	-40°C	VDD = 1.8V, Regulator Disabled	Fosc = 32 kHz, **SEC_RUN** mode, SOSCSEL = 01
		5.4	10	µA	+25°C		
		6.60	13	µA	+85°C		
	PIC18FXXK90	8.7	18	µA	-40°C	VDD = 3.3V, Regulator Disabled	
		10	20	µA	+25°C		
		12	**35**	µA	+85°C		
	PIC18FXXK90	60	150	µA	-40°C	VDD = 5V, Regulator Enabled	
		90	190	µA	+25°C		
		100	240	µA	+85°C		
	PIC18FXXK90	1.2	4	µA	-40°C	VDD = 1.8V, Regulator Disabled	Fosc = 32 kHz, **SEC_IDLE** mode, SOSCSEL = 01
		1.7	5	µA	+25°C		
		2.6	6	µA	+85°C		
	PIC18FXXK90	1.6	7	µA	-40°C	VDD = 3.3V, Regulator Disabled	
		2.8	9	µA	+25°C		
		4.1	**17**	µA	+85°C		
	PIC18FXXK90	60	160	µA	-40°C	VDD = 5V, Regulator Enabled	
		80	180	µA	+25°C		
		100	240	µA	+85°C		

Work around

None.

Affected Silicon Revisions

A3							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39957**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)

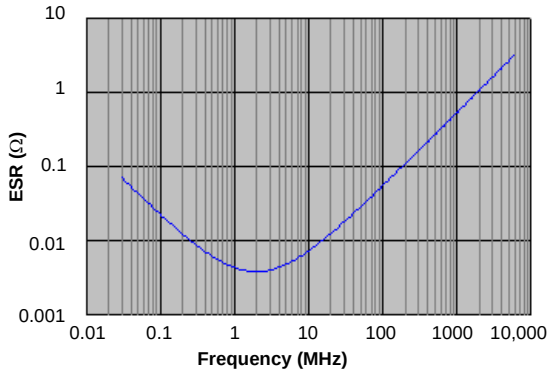
All the text is valid in **Section 2.4 Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)**, except for the recommended capacitor on the VCAP/VDDCORE pin when the internal voltage regulator is enabled.

Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specification can be used.

2. Module: Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)

The note in Figure 2-3 contains specific information for the Murata capacitor. Figure 2-3 now shows a typical frequency vs. ESR performance for all recommended capacitors with a note that applies to all suitable capacitors.

FIGURE 2-3 FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: **Typical data measurement at 25°C, 0V DC bias.**

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TABLE 2-1 SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to 125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to 85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to 125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to 85ºC
Murata	GRM32DR71C106KA01L	10 µF	±10%	16V	-55 to 125ºC
Murata	GRM31CR61C106KC31L	10 µF	±10%	16V	-55 to 85ºC

3. Module: Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)

Section 2.4.1 is added to **Section 2.4 Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)** as shown below:

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the VDDCORE voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

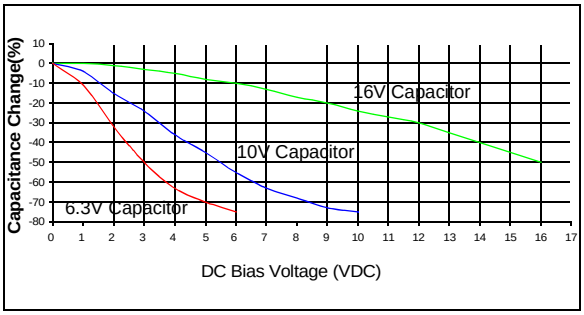
Typical low-cost, 10 μF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R) or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (for example, ±15%, over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 μF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum VDDCORE voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the Vddcore regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

Typical DC bias voltage vs. capacitance change graph for 16V, 10V and 6.3V rated capacitors is shown in Figure 2-4.

FIGURE 2-4 DC BIAS VOLTAGE vs. CAPACITANCE CHANGE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the VDDCORE voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 2.5V VDDCORE voltage. Suggested capacitors are shown in Table 2-1.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (5/2010)

Initial release of this document. Silicon issues 1 (A/D), 2 (BOR), 3 (HLVD). and 4 (Ports).

Rev B Document (11/2010)

Added data sheet clarifications 1-3 (Voltage Regulator Pins – ENVREG and VCAP/VDDCORE). Removed Silicon issue 2 (Brown-out Reset). Changes were made to Silicon issue 3 (HLVD). Added Silicon issues 4 (ECCP), 5 (EUSART) and 6 (IPD and IDD).

NOTES:

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