PIC18F87K22 Family
Silicon Errata and Data Sheet Clarification

The PIC18F87K22 family devices that you have received conform functionally to the current Device Data Sheet (DS39960**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F87K22 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F87K22 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID[(1)]	Revision ID for Silicon Revision[(2)]		
		A3		
PIC18F65K22	530h	3h		
PIC18F66K22	52Ch			
PIC18F67K22	518h			
PIC18F85K22	536h			
PIC18F86K22	532h			
PIC18F87K22	51Ch			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC18F6XKXX/8XKXX Family Flash Microcontroller Programming Specification"* (DS39947) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A3		
Analog-to-Digital Converter	A/D Offset	1.	The A/D offset is greater than specified in the data sheet's A/D Converter Characteristics table.	X		
Ports	Leakage	2.	I/O port leakage is higher than the D060 spec in the data sheet.	X		
High/Low-Voltage Detect	HLVD Trip	3.	The high-to-low (VDIRMAG = 0) setting of the HLVD may send initial interrupts.	X		
ECCP	Auto-Shutdown	4.	The tri-state setting of the auto-shutdown feature in the enhanced PWM may not successfully drive the pin to tri-state.	X		
EUSART	Synchronous Transmit	5.	When using the Synchronous Transmit mode of the EUSART, at high baud rates, transmitted data may become corrupted.	X		
I_{PD} I_{DD}	Maximum Limit	6.	Maximum current limits may be higher than specified in Table 31-2 of the data sheet.	X		

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

1. Module: Analog-to-Digital Converter (A/D)

The ADC will not meet the Microchip standard ADC specification. ADC may be usable if tested at the user end. The possible issues are high offset error, high DNL error and multiple missing codes. The ADC can be tested and used for relative measurements.

The ADC issues will be fixed in a future revision of this part.

ADC Offset

The ADC may have a high offset error up to a maximum of 50 LSB; it can be used if the ADC is calibrated for the offset.

Work around

Method to Calibrate for Offset:

In Single-Ended mode, connect the ADC +ve input to ground and take the ADC reading. This will be the offset of the device and can be used to compensate for the subsequent ADC readings on the actual inputs.

Affected Silicon Revisions

A3							
X							

2. Module: Ports

The input leakage will not match the D060 specification in the data sheet. The leakage will meet the 200 nA specification at T_A = 25ºC. At T_A = 85ºC, the leakage will be up to a max of 2 µA.

Work around

None.

Affected Silicon Revisions

A3							
X							

3. Module: High/Low-Voltage Detect (HLVD)

The high-to-low (VDIRMAG = 0) setting of the HLVD may send initial interrupts. High trip points that are close to the intended operating voltage are susceptible to this behavior.

Work around

Select a lower trip voltage that allows consistent start-up, or clear any initial interrupts from the HLVD on start-up.

Affected Silicon Revisions

A3							
X							

4. Module: ECCP

The tri-state setting of the auto-shutdown feature in the enhanced PWM may not successfully drive the pin to tri-state. The pin will remain an output and should not be driven externally. All tri-state settings will be affected.

Work around

None.

Affected Silicon Revisions

A3							
X							

5. Module: EUSART

When using the Synchronous Transmit mode of the EUSART, at high baud rates, transmitted data may become corrupted. One or more bits of the intended transmit message may be incorrect.

Work around

Since this problem is related to the baud rate used, adding a fixed delay before loading the TXREGx may not be a reliable work around. Lower the baud rate until no errors occur, or when loading the TXREGx, check that the TRMT bit inside of the TXSTAx register is set instead of checking the TXxIF bit.The following code can be used:

```
while(!TXSTAxbits.TRMT);
// wait to load TXREGx until TRMT is set
```

Affected Silicon Revisions

A3							
X							

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6. Module: IPD and IDD

The IPD and IDD limits will not match the data sheet. The values, in bold in **Section 31.2 "DC Characteristics: Power-Down and Supply Current PIC18F87K22 family (Industrial)"**, reflect the updated silicon maximum limits.

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31.2 DC Characteristics: Power-Down and Supply Current PIC18F87K22 family (Industrial)

PIC18F87K22 family (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device	Typ	Max	Units	Conditions		
	Power-Down Current (IPD)(1)						
	All devices	10	500	nA	-40°C	VDD = 1.8V(4) (Sleep mode) Regulator Disabled	
		20	500	nA	+25°C		
		120	600	nA	+60°C		
		630	**2000**	nA	+85°C		
	All devices	50	700	nA	-40°C	VDD = 3.3V(4) (Sleep mode) Regulator Disabled	
		60	**900**	nA	+25°C		
		170	**1100**	nA	+60°C		
		700	**5000**	nA	+85°C		
	All devices	350	1300	nA	-40°C	VDD = 5V(5) (Sleep mode) Regulator Enabled	
		400	1400	nA	+25°C		
		550	1500	nA	+60°C		
		1350	4000	nA	+85°C		
	Supply Current (IDD) Cont.(2,3)						
	All devices	3.7	8.5	µA	-40°C	VDD = 1.8V(4) Regulator Disabled	FOSC = 32 kHz(3) (**SEC_RUN** mode, SOSCSEL = 01)
		5.4	10	µA	+25°C		
		6.60	13	µA	+85°C		
	All devices	8.7	18	µA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		10	20	µA	+25°C		
		12	**35**	µA	+85°C		
	All devices	60	160	µA	-40°C	VDD = 5V(5) Regulator Enabled	
		90	190	µA	+25°C		
		100	240	µA	+85°C		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to VDD or VSS, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: Voltage regulator disabled (ENVREG = 0, tied to VSS, $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 1).

5: Voltage regulator enabled (ENVREG = 1, tied to VDD, SRETEN (WDTCON<4>) = 1 and $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 0).

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31.2 DC Characteristics: Power-Down and Supply Current PIC18F87K22 family (Industrial) (Continued)

PIC18F87K22 family (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device	Typ	Max	Units	Conditions		
	All devices	1.2	4	µA	-40°C	VDD = 1.8V(4) Regulator Disabled	FOSC = 32 kHz(3) (**SEC_IDLE** mode, SOSCSEL = 01)
		1.7	5	µA	+25°C		
		2.6	6	µA	+85°C		
	All devices	1.6	7	µA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		2.8	9	µA	+25°C		
		4.1	**17**	µA	+85°C		
	All devices	60	150	µA	-40°C	VDD = 5V(5) Regulator Enabled	
		80	180	µA	+25°C		
		100	240	µA	+85°C		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to VDD or VSS, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: Voltage regulator disabled (ENVREG = 0, tied to VSS, $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 1).

5: Voltage regulator enabled (ENVREG = 1, tied to VDD, SRETEN (WDTCON<4>) = 1 and $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 0).

Work around

None.

Affected Silicon Revisions

A3							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39960**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

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APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2010)

Initial release of this document. Silicon issues 1 (A/D), 2 (BOR), 3 (HLVD). and 4 (Ports).

Rev B Document (12/2010)

Removed Silicon issue 2 (Brown-out Reset). Changes were made to Silicon issue 3 (HLVD). Added Silicon issues 4 (ECCP), 5 (EUSART) and 6 (I_{PD} and I_{DD}).

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NOTES:

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