

Product Brief

MPC565PB/D
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MPC565/MPC566
Product Brief



This document provides an overview of the MPC565/MPC566 microcontrollers, including a block diagram showing the major modular components, sections that list the major features, and differences between the MPC565/MPC566 and the MPC555. The MPC565 and MPC566 devices are members of the Motorola MPC500 RISC Microcontroller family. The parts herein will be referred to only as MPC565 unless specific parts need to be referenced.

Table 1. MPC565/MPC566 Features

Device	Flash	Code Compression
MPC565	1 Mbyte	Code compression not supported
MPC566	1 Mbyte	Code compression supported

1 Introduction

The MPC565 device offers the following features:

- PowerPC™ core with a floating point unit (FPU) and a burst buffer controller (BBC)
- Unified system integration unit (USIU), a flexible memory controller, and improved interrupt controller
- 1 Mbyte of Flash memory (UC3F)
 - Typical endurance of 100,000 write/erase cycles @ 25°C
 - Typical data retention of 100 years @ 25°C
- 36 Kbytes of static RAM (two CALRAM modules)
 - 8 Kbytes of normal access or overlay access (sixteen 512-byte regions)
 - 4 Kbytes in CALRAM A, 4 Kbytes in CALRAM B
- Three time processor units (TPU3)
 - TPU3 A and TPU3 B are connected to DPTRAM AB (6 Kbytes)
 - TPU3 C is connected to DPTRAM C (4 Kbytes)
- A 22-timer channel modular I/O system (MIOS14)
 - Same as MIOS1 plus a real-time clock sub-module (MRTCSM), 4 counter sub-modules (MCSM), and 4 PWM sub-modules (MPWMSM)
- Three TouCAN modules (TouCAN_A, TouCAN_B, and TouCAN_C)
- Two enhanced queued analog to digital converters (QADC64E A, QADC64E B) with analog multiplexers (AMUX) for 40 total analog channels. These modules are configured so each module can access all 40 of the analog inputs to the part.

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Block Diagram

- Two queued serial multi-channel modules (QSMCM A, QSMCM B), each of which contains a queued serial peripheral interface (QSPI) and two serial controller interfaces (SCI/UART)
- -40°C – 125°C ambient temperature, -40°C – 85°C for suffix C devices, -55°C– 125°C for suffix A devices
- Debug features:
 - A J1850 (DLCMD2) communications module
 - A Nexus debug port (class 3) – IEEE-ISTO 5001-1999
 - JTAG and background debug mode (BDM)
- Packaging and Electrical

1.1 Block Diagram

Figure 1 is a block diagram of the MPC565.

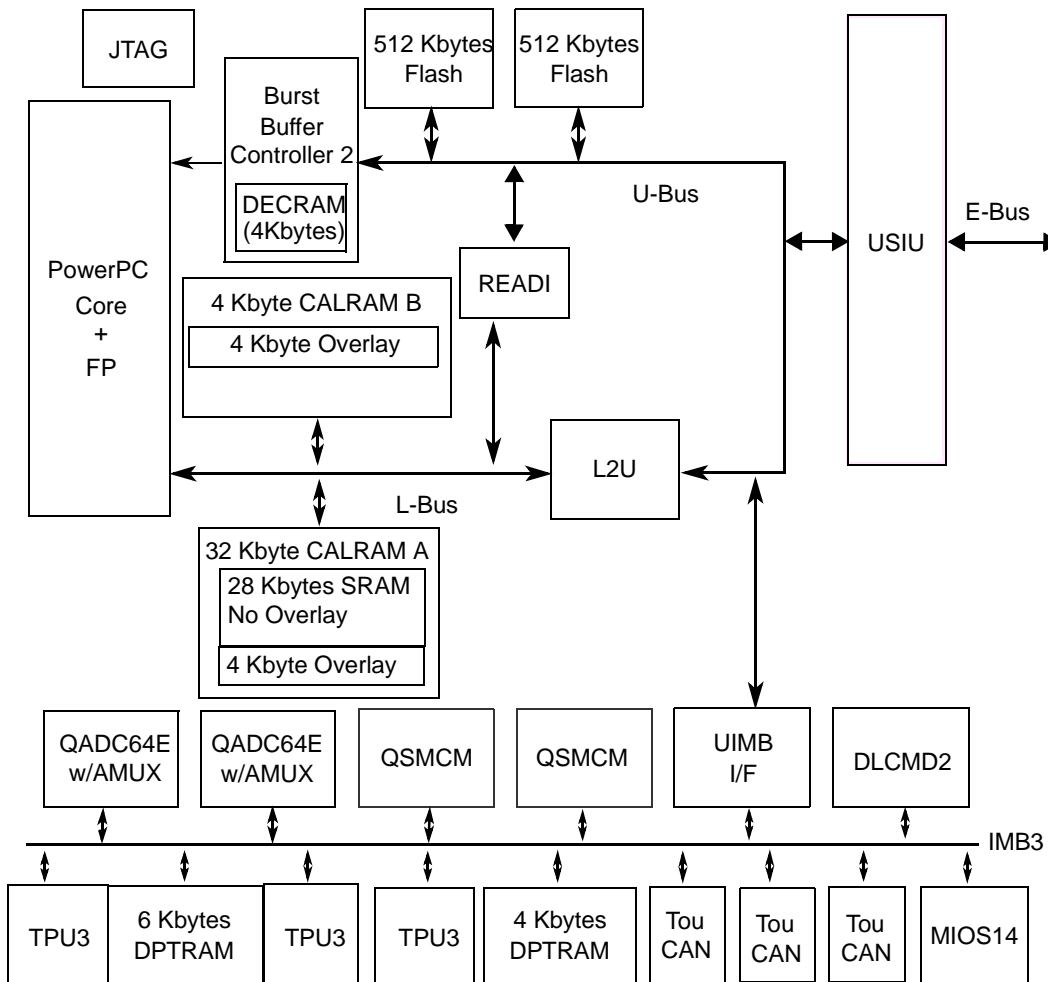


Figure 1. MPC565 Block Diagram

1.2 Detailed Feature List

The MPC565 key features are explained in the following sections.

1.2.1 High Performance CPU System

- Fully static design
- Four major power saving modes
 - On, doze, sleep, deep-sleep and power-down

1.2.2 RISC MCU Central Processing Unit (RCPU)

- High-performance core
 - PowerPC single issue integer core
 - Precise exception model
 - Floating point
 - Code compression (MPC566 only)
 - Compression reduces usage of internal or external Flash memory
 - Compression optimized for automotive (non-cached) applications
 - New compression scheme decreases code size to 40% –50% of source

1.2.3 MPC500 System Interface (USIU)

- MPC500 system interface (USIU, BBC, L2U)
- Periodic interrupt timer, bus monitor, clocks, decremter and time base
- Clock synthesizer, power management, reset controller
- External bus tolerates 5-V inputs, provides 2.6-V outputs
- Enhanced interrupt controller supports a separate interrupt vector for up to eight external and 40 internal interrupts
- IEEE 1149.1 JTAG test access port
- Bus supports multiple master designs
- USIU supports dual-mapping of Flash to move part of internal Flash memory to external bus for development
- External bus, supporting non-wraparound burst for instruction fetches, with up to 8 instructions per memory cycle

1.2.4 Burst Buffer Controller (BBC) Module

- Exception vector table relocation features allow exception table to be relocated to following locations:
 - 0x0000 0000 - 0x0000 1FFF (normal MPC500 exception table location)
 - 0x0001 0000 - 0x0001 1FFF (0 + 64 Kbytes; second page of internal Flash)
 - Second internal Flash module
 - Internal SRAM
 - 0x0FFF_0100 (external memory space; normal MPC500 exception table location)

1.2.5 Flexible Memory Protection Unit

- Flexible memory protection units in BBC (IMPU) and L2U (DMPU)
- Default attributes available in one global entry
- Attribute support for speculative accesses

1.2.6 Memory Controller

- Flexible chip selects via memory controller
- 24-bit address and 32-bit data buses
- 4- to 16-Mbyte (data) or 4-Gbyte (instruction) region size support
- Four-beat transfer bursts, two-clock minimum bus transactions
- Use with SRAM, EPROM, Flash and other peripherals
- Byte selects or write enables
- 32-bit address decodes with bit masks
- Four instruction regions
- Four data regions

1.2.7 1 Mbyte of CDR3 Flash EEPROM Memory (UC3F)

- 1 Mbyte Flash
 - Two UC3F modules, 512 Kbytes each
- Page mode read
- Block (64-Kbyte) erasable
- External 4.75- to 5.25-V VPP program and erase power supply
- Typical endurance of 100,000 write/erase cycles @ 25°C
- Typical data retention of 100 years @ 25°C

1.2.8 36-Kbyte Static RAM (CALRAM)

- 36-Kbyte static calibration RAM
 - Composed of 4-Kbyte and 32-Kbyte CALRAM modules
- Fast access: one clock
- Keep-alive power
- Soft defect detection (SDD)
- 4 Kbyte calibration (overlay) RAM per module (8 Kbytes total)
- Eight 512-byte overlay regions per module (16 regions total)

1.2.9 General Purpose I/O Support (GPIO)

- General-purpose I/O support
- Address (24) and data (32) pins can be used as GPIO in single-chip mode
- 16 GPIO in MIOS14
- Many peripheral pins can be used as GPIO when not used as primary functions
- 5-V outputs with slew rate control

1.2.10 Debug Features

- Extensive system debug support
- On-chip watchpoints and breakpoints
- Program flow tracking
- Background debug mode (BDM)

1.2.10.1 Nexus Debug Port (Class 3)

- Nexus/IEEE – ISTO 5001-1999 debug port (Class 3)
- Nine- or 16-pin interface

1.2.10.2 Message Data Link Controller (DLCMD2) Module

- Two pins muxed with QSMCMB pins. Muxing controlled by QSMCMB PCS3 pin assignment register
- SAE J1850 Class B data communications network interface compatible and ISO compatible for low-speed (<125 Kbps) serial data communications in automotive applications
- 10.4 Kbps variable pulse width (VPW) bit format
- Digital noise filter, collision detection
- Hardware cyclical redundancy check (CRC) generation and checking
- Block mode receive and transmit supported
- 4x receive mode supported (41.6 Kbps)
- Digital loopback mode
- In-frame response (IFR) types 0, 1, 2, and 3 supported
- Dedicated register for symbol timing adjustments
- Inter-module bus 3 (IMB3) slave interface
- Power-saving IMB3 stop mode with automatic wakeup on network activity
- Power-saving IMB3 CLOCKDIS mode
- Debug mode available through IMB3 FREEZE signal or user controllable SOFT_FRZ bit
- Polling and IMB3 interrupt generation with vector lookup available

1.2.11 Integrated I/O System

- True 5-V I/O

1.2.11.1 Time Processor Units (TPU3)

- Three time processing units (TPU3)
 - 16 channels each
- Each TPU3 is a microcoded timer subsystem
- One 6-Kbyte and one 4-Kbyte dual-port TPU RAM (DPTRAM), one (6-Kbyte) shared by two TPU3 modules for TPU microcode and the 4-Kbyte dedicated to the third TPU3 for microcode.

1.2.11.2 22-Channel Modular I/O System (MIOS14)

- 22-channel MIOS timer (MIOS14)
- Six modulus counter submodules (MCSM)
 - Four additional MCSM submodules compared to MIOS1
- 10 double action submodules (DASM).
- 12 dedicated PWM submodules (PWMSM)
 - Four additional PWM submodules compared to MIOS1 (shared with MIOS GPIO pins)
- MIOS real-time clock submodule (MRTCSM) provides low power clock/counter
 - Requires external 32-KHz crystal
 - Uses four pins: two for 32-KHz crystal, two for power/ground.

1.2.12 Two Enhanced Queued Analog-to-Digital Converter Modules (QADC64E)

- Two enhanced queued analog to digital converters (QADC64E A, QADC64E B) with AMUXes for 40 total analog channels.
- 10 bit A/D converter with internal sample/hold
 - Typical conversion time is 4 μ s (250-Kbyte samples/sec)
 - Two conversion command queues of variable length
- Automated queue modes initiated by:
 - External edge trigger/level gate
 - Software command
 - Periodic/interval timer, assignable to both queue 1 and 2
- 64 result registers in each QADC64E module
 - Output data is right or left justified, signed or unsigned
- Synchronized clock mode allows both QADC64Es to see the same conversion clock. This allows the two modules to look like one large QADC with four queues.
- Conversions alternate reference (ALTREF) pin. This pin can be connected to a different reference voltage

1.2.13 Three CAN 2.0B Controller (TouCAN) Modules

- Three TouCAN modules (TouCAN_A, TouCAN_B, and TouCAN_C)
- 16 message buffers each, programmable I/O modes
- Maskable interrupts
- Programmable loopback for self-test operation
- Independent of the transmission medium (external transceiver is assumed)
- Open network architecture, multimaster concept
- High immunity to EMI
- Short latency time for high-priority messages
- Low power sleep mode, with programmable wake up on bus activity
- TouCAN_C pins shared with MIOS14 GPIO pins

1.2.14 Queued Serial Multi-Channel Modules (QSMCM)

- Two queued serial modules with one queued-SPI and two SCI each (QSMCM_A, QSMCM_B)
 - QSMCM_A matches full MPC555 QSMCM functionality
 - QSMCM_B has pins muxed with DLCMD2 module
 - Two pins are muxed with DLCMD2 (J1850) transmit and receive pins (B_PCS3_J1850_TX and B_RXD2_J1850_RX)
 - QSMCM B vs J1850 mux control provided by QPAPCS3 bit in QSMCM pin assignment register (PQSPAR)
- Queued-SPI
 - Provides full-duplex communication port for peripheral expansion or interprocessor communication
 - Up to 32 preprogrammed transfers, reducing overhead
 - Synchronous serial interface with baud rate of up to system clock / 4
 - Four programmable peripheral-select pins support up to 16 devices
 - Special wrap-around mode allows continuous sampling of a serial peripheral for efficient interfacing to serial analog-to-digital (A/D) converters
- SCI
 - UART mode provides NRZ format and half- or full-duplex interface
 - 16 register receive buffer and 16 register transmit buffer on one SCI
 - Advanced error detection, and optional parity generation and detection
 - Word length programmable as 8 or 9 bits
 - Separate transmitter and receiver enable bits, and double buffering of data
 - Wake-up functions allow the CPU to run uninterrupted until either a true idle line is detected, or a new address byte is received

1.2.15 Electrical Specifications and Packaging

- 40 MHz operation (56 MHz operation is optional for the MPC566)
- -40°C – 125°C ambient temperature, -40°C – 85°C for suffix C device, -55°C– 125°C for suffix A devices
- 2.6 V \pm 0.1 V external bus
 - External bus is compatible with external memory devices operating from 2.5 V to 3.4 V.
 - Extended voltage range (2.7 – 3.4 V) degrades data drive timing by 1.1 ns on data writes.
- 2.6 \pm 0.1 V internal logic
- 5-V I/O (5.0 \pm 0.25 V)
- Available in package or bumped die
- Plastic ball grid array (PBGA) packaging
 - 388 ball PBGA
 - 27 mm x 27 mm body size
- 1.0 mm ball pitch

1.3 MPC565 Optional Features

The following features of the MPC565 are optional features and may not appear in certain configurations:

- 56-MHz operation (40-MHz is default)
- MPC566 supports code compression

2 Differences between the MPC565 and the MPC555

The MPC565 is an enhanced version of the MPC555. Most functional features of the MPC555 are unchanged on the MPC565. Table 2 shows the high level differences.

Table 2. Differences Between Modules of the MPC555 and the MPC565

Module	MPC555	MPC565
CPU Core	No Change	
BBC	BBC	BBC with improved code compression ¹
L2U	No Change	
SRAM	26-Kbytes	36-Kbyte CALRAM with overlay features
Flash	448-Kbyte CMF	1-Mbyte UC3F (new programming, etc.)
USIU	USIU	USIU with enhanced interrupt controller
JTAG	No Change	
READI	None	New Module
UIMB	No Change	
QADC64	2 QADC64 (16 channels on each QADC for 32 total channels)	2 QADC64E w/AMUXes (40 channels accessible from either QADC64E)
QSMCM	(1) No Change (2)	
DLCMD2 (J1850)	None	1
MIOS	MIOS1	MIOS14: MIOS1 with real-time clock (MRTCSM), 4 more PWMSMs and 4 more MCSMs
TouCAN	(2) No Change (3)	
TPU3	(2) No Change (3)	
DPTRAM	(6-Kbytes) No Change (6-Kbytes, 4-Kbytes)	
Power Supplies		
—	40 MHz with two power supplies: nominal 3.3-V to 5.0-V power supplies	56 MHz with two power supplies: 5.0-V I/O, 2.6-V internal logic

¹ Available on some options.

2.1 Additional MPC565 Differences

The following are additional differences between the MPC555 and the MPC565.

- SPI (MISO, MOSI, and SCK) pin drive.
 - MPC565 provides 21-ns rise/fall with 200-pf load using CMOS (20%/70%) levels
- GPIO on MODCK1 pin outputs only 2.6 V
 - MODCK1 pin is in keep-alive power section with no 5-V rail available
 - 5.0-V compatibility modes
 - Input is 5-V friendly
 - 2.6-V output has less slew rate control
 - 2.6-V: V_{OH} = 2.3 V
- Power supplies for external bus pins
 - QVDDL is quiet supply to hold non-switching outputs quiet even when noisy supply (NVDDL) sags
 - QVDDL supplies pre-drive and other pad logic
 - NVDDL only supplies final PMOS driver stage
 - QVDDL and NVDDL shorted on customer board after filtering
- Pull-up and pull-down changes during PORESET and HRESET
 - All 2.6-V/5-V pads (external bus: address/data/control) pull down at reset
 - All 5-V pads pull up at reset
 - Additional control granularity in the PDMCR register
- No pull-ups on QSMCM SCI receive pads
- A_RXD1_QGPI1, A_RXD2_QGPI2, B_RXD1_QGPI1 pins do not have weak pull-up during reset or any other time
- CLKOUT has 3 drive strength options
 - Better matches drive to requirements to reduce EMI
 - 25, 50, 100 pf instead of 45 and 90 pf
- Change reset value of ENGCLK to maximum divide (crystal/128)
 - For a 4-MHz crystal, this is 31.25 KHz
 - ENGCLK is selectable between 2.6 V and 5 V
- A daisy chain between UC3F modules allows either module to provide the reset configuration word (RCW)
- Censorship operation
 - A RCW bit controls whether or not the entire UC3F can be erased while censorship is violated
- BBC SPRs (PPC regs) access in two clocks instead of one clock
- CALRAM internal protection block size is 8 Kbytes
 - Instead of 4 Kbytes on MPC555 LRAM
- CALRAM causes machine check exception instead of data storage interrupt (DSI) exception in certain cases
 - For non-overlay CPU core accesses, a DSI exception is taken
 - For overlay accesses and any non-core access (slave mode), a machine check exception is taken

- CALRAM causes DSI exception only if the data relocation (DR) bit in the core machine state register, MSR[DR], is set.
 - L2U on MPC555 already followed this protocol, but the LRAM did not. Now all L-bus peripherals follow this protocol.
 - The MSR[DR] bit is described in the reference manual for more information.
- Four additional PRDS control bits were added to the USIU to allow more granularity of PRDS control on a part
- BBC includes a 4-Kbyte DECRAM that can be used if compression is not used or is not available.

3 SRAM Keep-Alive Power Behavior

The SRAM has three keep-alive power pins (VDDSRAM1, VDDSRAM2, and VDDSRAM3). These pins provide keep-alive power to the SRAM arrays in the CALRAM modules and the DPTRAM modules.

The VDDSRAM1 pin powers the 32-Kbyte CALRAM A during keep-alive while power is off to the MPC565 (except for the keep-alive power supplies). CALRAM A keeps all of its 32 Kbytes powered during power down.

The VDDSRAM2 pin powers the 4-Kbyte CALRAM B module. The VDDSRAM3 pin powers the DPTRAM modules during keep-alive as well as during normal operation. The CALRAM modules only power their arrays from the VDDSRAM pins during keep-alive. During normal operation, they are powered by the normal internal VDD of the part.

The DPTRAM modules (6 Kbytes and 4 Kbytes) and the 4-Kbyte DECRAM in the BBC module power their arrays via the VDDSRAM3 pin during keep-alive and are supplied by VDD during normal operation.

4 MPC565 Memory Map

The internal memory map is organized as a single 4-Mbyte block. This is shown in Figure 3. This block can be moved to one of eight different locations. The internal memory space is divided into the following sections:

- Flash memory (1 Mbyte) — U-bus memory
- Static RAM memory (36 Kbytes CALRAM) — L-bus memory
- Control registers and IMB3 modules (64 Kbytes), partitioned as
 - USIU and flash control registers
 - UIMB interface and IMB3 modules
 - CALRAM and READI control registers (L-bus control register space)

The internal memory block can reside in one of eight possible 4-Mbyte memory spaces. These eight locations are the first eight 4-Mbyte memory blocks starting with address 0x0000 0000, as shown in Figure 2. There is a user programmable register in the USIU to configure the internal memory map to one of the eight possible locations. Programmability of internal memory map location allows multiple chip system.

The IMB3 address space block in Figure 3 shows memory allocation for IMB3 modules. It does not show the actual memory space required for individual modules. All modules are mapped to the low address, numerically, of the memory allocated for that module in the IMB3 address space.

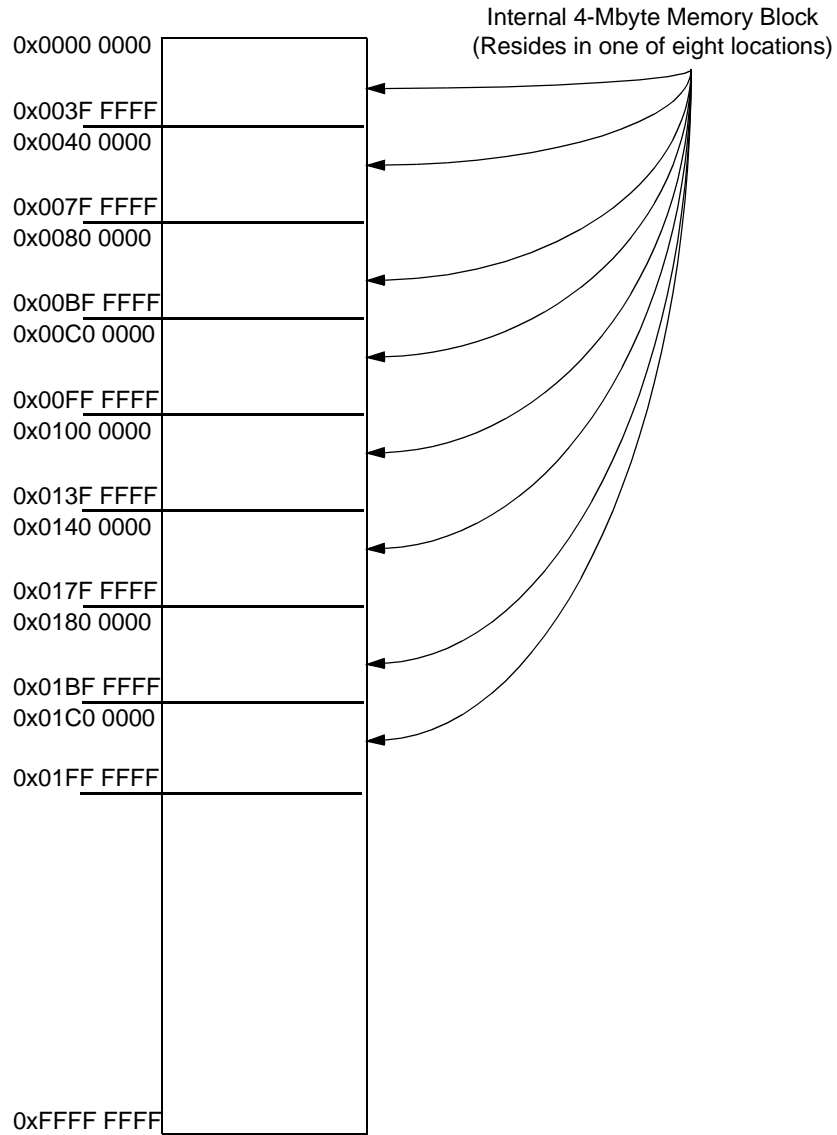


Figure 2. Memory Map

Freescale Semiconductor, Inc.

Additional MPC565 Differences

0x00 0000	UC3F_A Flash 512 Kbytes	USIU Control Registers	0x2F C000
0x07 FFFF		UC3F_A Control (64 bytes)	0x2F C800
0x08 0000	UC3F_B Flash 512 Kbytes	UC3F_B Control (64 bytes)	0x2F C840
0x0F FFFF			0x2F C87F
0x10 0000	Reserved for Flash (2,016 Kbytes)		
0x2F 7FFF		DPTRAM_AB Registers (64 bytes)	0x30 0000
0x2F 8000	DECRAM 4 Kbytes	DPTRAM_C Registers (64 bytes)	0x30 0040
0x2F 8FFF		DLCMD2 (16 bytes)	0x30 0080
0x2F 9000	Reserved	Reserved (3952 bytes)	0x30 0090
0x2F 9FFF			
0x2F A000	BBC Control Registers 8 Kbytes	DPTRAM_C (4 Kbytes)	0x30 1000
0x2F BFFF		DPTRAM_AB (6 Kbytes)	0x30 2000
0x2F C000	USIU & Flash Control 16 Kbytes	Reserved (2 Kbytes)	0x30 3800
0x2F FFFF		TPU3_A (1 Kbytes)	0x30 4000
0x30 0000	UIMB I/F & IMB Modules 32 Kbytes	TPU3_B (1 Kbytes)	0x30 4400
0x30 7FFF		QADC64_A (1 Kbytes)	0x30 4800
0x30 8000	Reserved for IMB 480 Kbytes	QADC64_B (1 Kbytes)	0x30 4C00
0x37 FFFF		QSMCM_A (1 Kbytes)	0x30 5000
0x38 0000	CALRAM/ Readi Control 256 bytes	QSMCM_B (1 Kbytes)	0x30 5400
0x38 00FF		Reserved (1 Kbytes)	0x30 5800
0x38 0100	Reserved (L-bus Control) ~32 Kbytes	TPU3_C (1 Kbytes)	0x30 5C00
0x38 3FFF		MIOS14 (4 Kbytes)	0x30 6000
0x38 4000	Reserved (L-bus Mem) 444 Kbytes	TOUCAN_A (1 Kbytes)	0x30 7000
0x3F 6FFF		TOUCAN_B (1 Kbytes)	0x30 7400
0x3F 7000	All 4-Kbytes can be Overlay Section	TOUCAN_C (1 Kbytes)	0x30 7800
0x3F 7FFF	CALRAM_B (4 Kbyte)	Reserved (896 bytes)	0x30 7900
0x3F 8000		UIMB Control Registers (128 bytes)	0x30 7F80
	CALRAM_A (32 Kbyte)		0x30 7FFF
0x3F FFFF	4-Kbyte Overlay Section		

Figure 3. Internal Memory Block

5 MPC565 Pinout Diagram

Figure 4 shows the pinout for the MPC565.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	VDD	ANA_B_P0B0	VBI	VRL	AM8	AM8_P0B0	AM8_P0A0	AM8_P0A0	VSSA	AM8_P0A0	AM8_P0A0	AM8_P0A0	AM8_P0A0	AM8_P0A0	AM8_P0A0	AM8_P0A0	AM8_P0A0	AM8_P0A0	AM8_P0A0	AM8_P0A0	AM8_P0A0	AM8_P0A0	AM8_P0A0	AM8_P0A0	VSS
B	VSS	ANA_AV_A_P0B1	ALTRF	AM6	AM6_P0B0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	VDD
C	VDRTRC	VSS	VDD	AM5_AK_A_P0B1	AM7	AM7_P0B0	AM7_P0A0	AM7_P0A0	AM7_P0A0	AM7_P0A0	AM7_P0A0	AM7_P0A0	AM7_P0A0	AM7_P0A0	AM7_P0A0	AM7_P0A0	AM7_P0A0	AM7_P0A0	AM7_P0A0	AM7_P0A0	AM7_P0A0	AM7_P0A0	AM7_P0A0	AM7_P0A0	VDD
D	EXTAL32	VDRSRM2	VSS	VDD	AM6	AM6_P0B0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	AM6_P0A0	VDD
E	XTAL32	B_CNTRX	VDRSRM1	VSS	VDD	AM5_AK_A_P0B1	AM5_AK_A_P0A0	AM5_AK_A_P0A0	AM5_AK_A_P0A0	AM5_AK_A_P0A0	AM5_AK_A_P0A0	AM5_AK_A_P0A0	AM5_AK_A_P0A0	AM5_AK_A_P0A0	AM5_AK_A_P0A0	AM5_AK_A_P0A0	AM5_AK_A_P0A0	AM5_AK_A_P0A0	AM5_AK_A_P0A0	AM5_AK_A_P0A0	AM5_AK_A_P0A0	AM5_AK_A_P0A0	AM5_AK_A_P0A0	AM5_AK_A_P0A0	VDD
F	VSSRTRC	C_TRU014	C_TRU015	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L	MD1L
G	C_TRU010	C_TRU011	C_TRU012	C_TRU013	C_TRU014	C_TRU015	C_TRU016	C_TRU017	C_TRU018	C_TRU019	C_TRU020	C_TRU021	C_TRU022	C_TRU023	C_TRU024	C_TRU025	C_TRU026	C_TRU027	C_TRU028	C_TRU029	C_TRU030	C_TRU031	C_TRU032	C_TRU033	C_TRU034
H	C_TRU039	C_TRU040	C_TRU041	C_TRU042	C_TRU043	C_TRU044	C_TRU045	C_TRU046	C_TRU047	C_TRU048	C_TRU049	C_TRU050	C_TRU051	C_TRU052	C_TRU053	C_TRU054	C_TRU055	C_TRU056	C_TRU057	C_TRU058	C_TRU059	C_TRU060	C_TRU061	C_TRU062	C_TRU063
J	C_TRU064	C_TRU065	C_TRU066	C_TRU067	C_TRU068	C_TRU069	C_TRU070	C_TRU071	C_TRU072	C_TRU073	C_TRU074	C_TRU075	C_TRU076	C_TRU077	C_TRU078	C_TRU079	C_TRU080	C_TRU081	C_TRU082	C_TRU083	C_TRU084	C_TRU085	C_TRU086	C_TRU087	C_TRU088
K	C_TRU089	C_TRU090	C_TRU091	C_TRU092	C_TRU093	C_TRU094	C_TRU095	C_TRU096	C_TRU097	C_TRU098	C_TRU099	C_TRU100	C_TRU101	C_TRU102	C_TRU103	C_TRU104	C_TRU105	C_TRU106	C_TRU107	C_TRU108	C_TRU109	C_TRU110	C_TRU111	C_TRU112	C_TRU113
L	MD10	MD11	MD12	MD13	MD14	MD15	MD16	MD17	MD18	MD19	MD20	MD21	MD22	MD23	MD24	MD25	MD26	MD27	MD28	MD29	MD30	MD31	MD32	MD33	MD34
M	MD35	MD36	MD37	MD38	MD39	MD40	MD41	MD42	MD43	MD44	MD45	MD46	MD47	MD48	MD49	MD50	MD51	MD52	MD53	MD54	MD55	MD56	MD57	MD58	MD59
N	MD60	MD61	MD62	MD63	MD64	MD65	MD66	MD67	MD68	MD69	MD70	MD71	MD72	MD73	MD74	MD75	MD76	MD77	MD78	MD79	MD80	MD81	MD82	MD83	MD84
P	MD85	MD86	MD87	MD88	MD89	MD90	MD91	MD92	MD93	MD94	MD95	MD96	MD97	MD98	MD99	MD100	MD101	MD102	MD103	MD104	MD105	MD106	MD107	MD108	MD109
R	MD110	MD111	MD112	MD113	MD114	MD115	MD116	MD117	MD118	MD119	MD120	MD121	MD122	MD123	MD124	MD125	MD126	MD127	MD128	MD129	MD130	MD131	MD132	MD133	MD134
T	MD135	MD136	MD137	MD138	MD139	MD140	MD141	MD142	MD143	MD144	MD145	MD146	MD147	MD148	MD149	MD150	MD151	MD152	MD153	MD154	MD155	MD156	MD157	MD158	MD159
U	MD160	MD161	MD162	MD163	MD164	MD165	MD166	MD167	MD168	MD169	MD170	MD171	MD172	MD173	MD174	MD175	MD176	MD177	MD178	MD179	MD180	MD181	MD182	MD183	MD184
V	MD185	MD186	MD187	MD188	MD189	MD190	MD191	MD192	MD193	MD194	MD195	MD196	MD197	MD198	MD199	MD200	MD201	MD202	MD203	MD204	MD205	MD206	MD207	MD208	MD209
W	MD210	MD211	MD212	MD213	MD214	MD215	MD216	MD217	MD218	MD219	MD220	MD221	MD222	MD223	MD224	MD225	MD226	MD227	MD228	MD229	MD230	MD231	MD232	MD233	MD234
Y	MD235	MD236	MD237	MD238	MD239	MD240	MD241	MD242	MD243	MD244	MD245	MD246	MD247	MD248	MD249	MD250	MD251	MD252	MD253	MD254	MD255	MD256	MD257	MD258	MD259
AA	MD260	MD261	MD262	MD263	MD264	MD265	MD266	MD267	MD268	MD269	MD270	MD271	MD272	MD273	MD274	MD275	MD276	MD277	MD278	MD279	MD280	MD281	MD282	MD283	MD284
AB	MD285	MD286	MD287	MD288	MD289	MD290	MD291	MD292	MD293	MD294	MD295	MD296	MD297	MD298	MD299	MD300	MD301	MD302	MD303	MD304	MD305	MD306	MD307	MD308	MD309
AC	MD310	MD311	MD312	MD313	MD314	MD315	MD316	MD317	MD318	MD319	MD320	MD321	MD322	MD323	MD324	MD325	MD326	MD327	MD328	MD329	MD330	MD331	MD332	MD333	MD334
AD	MD335	MD336	MD337	MD338	MD339	MD340	MD341	MD342	MD343	MD344	MD345	MD346	MD347	MD348	MD349	MD350	MD351	MD352	MD353	MD354	MD355	MD356	MD357	MD358	MD359
AE	MD360	MD361	MD362	MD363	MD364	MD365	MD366	MD367	MD368	MD369	MD370	MD371	MD372	MD373	MD374	MD375	MD376	MD377	MD378	MD379	MD380	MD381	MD382	MD383	MD384
AF	MD385	MD386	MD387	MD388	MD389	MD390	MD391	MD392	MD393	MD394	MD395	MD396	MD397	MD398	MD399	MD400	MD401	MD402	MD403	MD404	MD405	MD406	MD407	MD408	MD409

NOTE: This is a top down view of the balls.

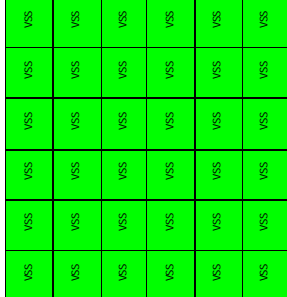


Figure 4. MPC565 Pinout Diagram

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