PIC32MX575/675/695/775/795 Family Silicon Errata and Data Sheet Clarification

The PIC32MX575/675/695/775/795 family devices that you have received conform functionally to the current Device Data Sheet (DS61156**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MX575/675/695/775/795 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A0**).

Data Sheet clarifications and corrections start on page 11, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with the REAL ICE™ in-circuit emulator:

1. Using the appropriate interface, connect the device to the REAL ICE in-circuit emulator.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MX575/675/695/775/795 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A0
PIC32MX575F256H	0x4317053	0x0
PIC32MX675F256H	0x430B053	0x0
PIC32MX775F256H	0x4303053	0x0
PIC32MX575F512H	0x4309053	0x0
PIC32MX675F512H	0x430C053	0x0
PIC32MX695F512H	0x4325053	0x0
PIC32MX775F512H	0x430D053	0x0
PIC32MX795F512H	0x430E053	0x0
PIC32MX575F256L	0x4333053	0x0
PIC32MX675F256L	0x4305053	0x0

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"PIC32MX Flash Programming Specification"* (DS61145) for detailed information on Device and Revision IDs for your specific device.

TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A0
PIC32MX775F256L	0x4312053	0x0
PIC32MX575F512L	0x430F053	0x0
PIC32MX675F512L	0x4311053	0x0
PIC32MX695F512L	0x4341053	0x0
PIC32MX775F512L	0x4307053	0x0
PIC32MX795F512L	0x4307053	0x0

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"PIC32MX Flash Programming Specification"* (DS61145) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A0
I^2C™	Start condition	1.	The I^2C modules may encounter a bus collision when performing a Start condition.	X
Ethernet	RMII 10 MB	2.	Pause frames are sent at 10x the normal rate.	X
ADC	Interrupt Generation	3.	The interrupt generated by the module cannot be cleared when the module is disabled.	X
Parallel Master Port	Slave Mode	4.	A PMP interrupt used to wake the device will not be reflected in the interrupt flag until the end of the write strobe.	X
Output Compare	Electrical Specification	5.	OC Fault detection is not asynchronous.	X
SPI	—	6.	The SPIBUSY and SRMT bits assert 1 bit time before the end of the transaction.	X
UART	—	7.	The TXBF bit deasserts one PB clock after the interrupt is generated.	X
USB	USB PLL	8.	The USBPLL does not automatically suspend in Idle mode.	X
Output Compare	PWM	9.	In PWM mode, the output waveform is one PB clock longer than the expected value.	X
Output Compare	PWM Fault Input Mode	10.	A Fault interrupt will not be generated if firmware clears the Fault while the Fault is still asserted.	X
DMA	Pattern Match	11.	In Pattern Match mode, the DMA module may not append all of the CRC results to the result buffer.	X
Timers	External Clock	12.	In Synchronized External Clock mode, the first period of the count is short.	X
SPI	Frame Slave Mode	13.	Outgoing data corruption occurs when the frame signal is coincident with the clock.	X
CAN	—	14.	TXABAT, TXLARB and TXERR may erroneously be cleared by an aborted read of the CiFIFOCONn register.	X
CAN	—	15.	Requested aborts to a TX message via setting CxCON.ABAT or clearing CiFIFOCON.TXREQ may not complete.	X
CAN	—	16.	The CFIFOCONx.FRESET and CFIFOCONx.UINC bits are not settable via a normal SFR write.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A0
CAN	DeviceNet™	17.	DeviceNet filtering does not function.	X
Output Compare	PWM Fault Input Mode	18.	A Fault may be erroneously cleared due to an aborted read.	X
SPI	Slave Mode	19.	In Slave mode, a TX buffer under-run condition will not assert the TX interrupt flag.	X
USB	—	20.	The TOKBUSY bit does not correctly indicate status when a transfer completes within the Start of Frame (SOF) threshold.	X
USB	Host Mode	21.	In Host mode, the interval between the first two SOF packets may be less than what is specified by the USB specification.	X
WDT	—	22.	When code-protect is enabled, the WDT is not held in Reset during the POR RAM Clear Sequence (RCS).	X
Oscillator	Clock Switch and Two -Speed Start-Up	23.	Clock switching and Two-Speed Start-up may cause a general exception when the reserved bit 8 of the DDPCON register is '0'.	X
Oscillator	Clock Switch	24.	Clock source switching may cause a general exception or POR when switching from a slow clock to a fast clock.	X
SPI	Slave Mode	25.	A wake-up interrupt may not be clearable.	X
PORTS	—	26.	I/O pins do not tri-state immediately, if previously driven high.	X
SPI	—	27.	Byte writes to the SPISTAT register are not decoded correctly.	X
SPI	Frame Mode	28.	Recovery from an underrun requires multiple SPI clock periods.	X
CAN	—	29.	The TXBAT bit status may be incorrect after an abort.	X
UART	IrDA®	30.	The IrDA minimum bit time is not detected at all baud rates.	X
UART	IrDA	31.	TX data is corrupted when BRG values greater than 0x200 are used.	X
JTAG	—	32.	On 64-pin devices, the TMS pin requires an external pull-up.	X
UART	—	33.	The TRMT bit is asserted before the transmission is complete.	X
UART	UART Receive Buffer Overrun Error Status	34.	The OERR bit does not get cleared on a module Reset. The OERR bit retains its value even after the UART module is reinitialized.	X
ADC	Conversion Trigger from INT0 Interrupt	35.	The ADC module conversion triggers occur on the rising edge of the INT0 signal even when INT0 is configured to generate an interrupt on the falling edge.	X
JTAG	Boundary Scan	36.	Pin 100 on 100-pin packages and pin A1 on 121-pin packages do not respond to boundary scan commands.	X
DMA	Suspend Status	37.	The DMABUSY status bit may not reflect the correct status if the DMA module is suspended.	X
Voltage Regulator	BOR	38.	Device may not exit BOR state if BOR event occurs.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A0**).

1. Module: I²C™

The I²C modules, with the exception of I²C1 and I²C2, may encounter a bus collision when performing a Start condition.

Work around

1. Use another I²C node on the bus to sequence I²C bus transactions such as the Start event.
2. Connect an unused general-purpose I/O pin to the SDAx pin of the I²C module to be used.
   The user software must perform the following sequence of operations in order to execute a Start condition on the I²C bus:
   a) With the I²C module disabled, clear the LAT bit of the general-purpose I/O pin that is connected to the SDAx pin. Then, clear the corresponding TRIS bit to make sure the I/O pin is pulled low.
   b) Enable the I²C module by setting the ON bit (I2CxCON<15>); but do not configure the I2CxBRG register at this time.
   c) Execute a software delay loop of at least 10 µs.
   d) Set the TRIS bit of the I/O pin connected to the SDAx pin. This will make it an input pin, thereby ensuring that it goes to a high logic state.
   e) Execute a software delay loop of at least 10 usec.
   f) Configure the I2CxBRG register with the value required by the application.
   g) Issue a Start condition by setting the SEN bit (I2CxCON<0>) as needed. I²C communications can now proceed normally.

Affected Silicon Revisions

A0							
X							

2. Module: Ethernet

In 10 MB RMII mode only, pause frames are sent at 10x the normal rate. This reduces the available network bandwidth if the device is connected to the network via a hub. This does not reduce functionality or violate specifications.

Work around

If bandwidth is a concern, connect the PIC32 device to a network using an Ethernet switch.

Affected Silicon Revisions

A0							
X							

3. Module: ADC

The interrupt generated by the ADC module cannot be cleared when the ADC module is disabled.

Work around

Ensure the interrupt is serviced and the interrupt flag is cleared before turning off the ADC module.

Affected Silicon Revisions

A0							
X							

4. Module: Parallel Master Port

In Slave mode, a PMP interrupt will wake the device; however, the interrupt source will not be reflected in the interrupt flag until the end of the write strobe.

Work around

There are two possible solutions to this issue:

1. If multiple wake-up sources are to be used, firmware can poll all of the configured wake-up source interrupt flags. If none are set, assume the source was the PMP.
2. Firmware can wait for a period exceeding the write strobe length, and then poll the PMP interrupt flag.

Affected Silicon Revisions

A0							
X							

5. Module: Output Compare

The Fault input detection is not asynchronous. There is a 1 to 2 Peripheral Bus (PB) clock delay between the Fault input assertion and the shutdown of the appropriate OCMP output pin.

Work around

Ensure that the device driven by the OCMP module can tolerate this shutdown delay.

Affected Silicon Revisions

A0							
X							

6. Module: SPI

The SPIBUSY and SRMT bits assert 1 bit time before the end of the transaction.

Work around

Firmware must provide a 1 bit time delay between the assertion of these bits and performing any operation that requires the transaction to be complete.

Affected Silicon Revisions

A0							
X							

7. Module: UART

The UxSTA.TXBF bit clears one PB clock cycle after the interrupt is generated. When using a PB bus divisor other than 1:1 and polling the UART transmit interrupt flag with the next instruction reading the UxSTA.TXBF bit, the result may not reflect the actual TXBF status.

Work around

There are two possible solutions to this issue:

1. Only use a PB bus divisor of 1:1.
2. If firmware is polling the transmit interrupt flag and the TXBF flag, insert a read of the UxSTA register between these operations and discard the result. This read will ensure the status of the TXBF flag is correct when the next read of this register occurs.

Affected Silicon Revisions

A0							
X							

8. Module: USB

When U1CNFG1.USBSIDL is set, the USBPLL does not automatically suspend in Idle mode.

Work around

Use firmware to manually suspend the USB clock before entering Sleep mode.

Affected Silicon Revisions

A0							
X							

9. Module: Output Compare

In PWM mode, the output waveform is one PB clock longer than the expected value.

Work around

Load OCRS with a value one less than the number expected to achieve the desired output.

Affected Silicon Revisions

A0							
X							

10. Module: Output Compare

In PWM mode, if firmware attempts to clear the OCFLT bit while the Fault still exists, a second interrupt will not be generated for this Fault when firmware exits the Interrupt Service Routine (ISR). The OCFLT bit will remain set while a Fault is detected.

Work around

In the ISR, clear the OSxFLT bit, and test the OCxFLT bit before exiting the ISR. If the bit is set, set the OCx interrupt to generate a second interrupt.

Affected Silicon Revisions

A0							
X							

11. Module: DMA

In Pattern Match mode, the DMA module may not append all of the CRC results to the result buffer.

Work around

Use firmware to read the CRC result and append it to the result buffer.

Affected Silicon Revisions

A0							
X							

12. Module: Timers

When the Timer module is first enabled and the prescaler value is greater than 1, the number of input clocks required to increment the timer from 0 to 1 is one input clock, not the value stated by the prescaler.

Work around

None.

Affected Silicon Revisions

A0							
X							

13. Module: SPI

Outgoing data will be corrupted when in Frame Slave mode with FRMCNT > 0 and the frame pulse is coincident with the clock.

Work around

1. There is no work around for operation when the Frame pulse is coincident with the clock.
2. Provide a frame signal that precedes the clock signal.

Affected Silicon Revisions

A0							
X							

14. Module: CAN

TXABAT, TXLARB and TXERR may erroneously be cleared by an aborted read of the CiFIFOCONn register. An aborted read occurs when a load instruction in the CPU pipeline has started execution, but is aborted due to an interrupt.

Work around

Disable interrupts before reading the contents of the CiFIFOCONn register, and then re-enable interrupts after reading the register.

Affected Silicon Revisions

A0							
X							

15. Module: CAN

Requested aborts to a TX message via setting CxCON.ABAT or clearing CiFIFOCON.TXREQ may not complete. The CAN bus protocol is not violated.

Work around

1. After a general abort request, firmware should poll until CxCON.BUSY = 0 or wait two message times. If CxCON.ABAT remains high, the message was successfully aborted and the module must be reset by clearing and setting bit CxCON.ON.
2. After a FIFO specific abort request, firmware should poll until CxCON.BUSY = 0 or wait two message times. If CFIFOCONx.TXREQ remains high, the message was successfully aborted and the FIFO must be reset by setting CFIFOCONx.FRESET and polling until CFIFOCONx.FRESET = 0.

Affected Silicon Revisions

A0							
X							

16. Module: CAN

The CFIFOCONx.FRESET and CFIFOCONx.UINC bits are not settable via a normal Special Function Register (SFR) write.

Work around

Use the SET register operations to change the state of these bits.

Affected Silicon Revisions

A0							
X							

17. Module: CAN

The DeviceNet™ message filtering does not function.

Work around

Use hardware to filter the Standard Identifier (SID) and use firmware to decode the DeviceNet identifier.

Affected Silicon Revisions

A0							
X							

18. Module: Output Compare

The Output Compare module may reinitialize or clear a Fault on an aborted read of the OCxCON register. An aborted read occurs when a read instruction in the CPU pipeline has started execution, but is aborted due to an interrupt.

Work around

Disable interrupts before reading the contents of the OCxCON register, and then re-enable interrupts after reading the register.

Affected Silicon Revisions

A0							
X							

19. Module: SPI

In Slave mode with TXISEL = 0, a TX buffer underrun condition will not assert the TX interrupt flag.

Work around

None.

Affected Silicon Revisions

A0							
X							

20. Module: USB

The TOKBUSY bit does not correctly indicate status when a transfer completes within the Start of Frame threshold.

Work around

Use a firmware semaphore to track when a token is written to U1TOK. Firmware then clears the semaphore when the transfer is complete.

Affected Silicon Revisions

A0							
X							

21. Module: USB

In Host mode, the interval between the first two SOF packets may be less than what is specified by the USB specification.

Work around

None.

Affected Silicon Revisions

A0							
X							

22. Module: WDT

When code-protect is enabled, the WDT is not held in reset during the POR RAM Clear Sequence (RCS). If the WDT period does not exceed the RCS period, the WDT will reset the part and the RCS sequence will restart.

Work around

Use WDT periods equal to or longer than 128 ms. Since the RCS and WDT run concurrently, firmware will have a reduced period in which to service the WDT for the first time.

Affected Silicon Revisions

A0							
X							

23. Module: Oscillator

Clock switching and Two-Speed Start-up may cause a general exception when the reserved bit 8 of the DDPCON register is '0'.

Work around

Ensure that the reserved bit 8 of the DDPCON register to set to '1'. For example,

```
DDPCON |= 0x100;
```

Affected Silicon Revisions

A0							
X							

24. Module: Oscillator

Clock source switching may cause a general exception or POR when switching from a slow clock to a fast clock.

Work around

Clock source switches should be performed by first switching to the FRC, and then switching to the target clock source.

Note: If the peripheral library is being used, clock switching is performed automatically through the FRC.

Affected Silicon Revisions

A0							
X							

25. Module: SPI

In Slave mode, when entering Sleep mode after a SPI transfer with SPI interrupts enabled, a false interrupt may be generated that wakes the device. This interrupt can be cleared; however, entering Sleep may cause the condition to occur again.

Work around

Do not use SPI in Slave mode as a wake-up source from Sleep.

Affected Silicon Revisions

A0							
X							

26. Module: PORTS

When an I/O pin is set to output a logic high signal, and is then changed to an input using the TRISx registers, the I/O pin should immediately tri-state and let the pin float. Instead, the pin will continue to partially drive a logic high signal out for a period of time.

Work around

The pin should be driven low, prior to being tri-stated, if it is desirable for the pin to tri-state quickly.

Affected Silicon Revisions

A0							
X							

27. Module: SPI

Byte writes to the SPISTAT register are not decoded correctly. A byte write to byte zero of SPISTAT is actually performed on both byte zero and byte one. A byte write to byte one of SPISTAT is ignored.

Work around

Only perform word operations on the SPISTAT register.

Affected Silicon Revisions

A0							
X							

28. Module: SPI

In Frame mode the module is not immediately ready for further transfers after clearing the SPITUR bit. The SPITUR bit will be cleared by hardware before the SPI state machine is prepared for the next operation.

Work around

Firmware must wait at least four bit times before writing to the SPI registers after clearing the SPITUR bit.

Affected Silicon Revisions

A0							
X							

29. Module: CAN

When an abort request occurs concurrently with a successful message transmission, and additional messages remain in the FIFO, these remaining messages are not transmitted and the TXABAT bit does not reflect the abort.

Work around

The actual FIFO status can be determined by the FIFO pointers CFIFOCI and CFIFOUA.

Affected Silicon Revisions

A0							
X							

30. Module: UART

The UART module is not fully IrDA® compliant. The module does not detect the 1.6 µs minimum bit width at all baud rates as defined in the IrDA specification. The module does detect the 3/16 bit width at all baud rates.

Work around

None.

Affected Silicon Revisions

A0							
X							

31. Module: UART

In IrDA mode with baud clock output enabled, the UART TX data is corrupted when the BRG value is greater than 0x200.

Work around

Use the Peripheral Bus (PB) divisor to lower the PB frequency such that the required UART BRG value is less than 0x201.

Affected Silicon Revisions

A0							
X							

32. Module: JTAG

On 64-pin devices an external pull-up resistor is required on the TMS pin for proper JTAG.

Work around

Connect a 100k-200k pull-up to the TMS pin.

Affected Silicon Revisions

A0							
X							

33. Module: UART

The TRMT bit is asserted during the STOP bit generation, not after the STOP bit has been sent.

Work around

If firmware needs to be aware when the transmission is complete, firmware should add a half bit time delay after the TRMT bit is asserted.

Affected Silicon Revisions

A0							
X							

34. Module: UART

The OERR bit does not get cleared on a module Reset. If the OERR bit is set and the module is disabled, the OERR bit retains its status even after the UART module is reinitialized.

Work around

The user software must check this bit in the UART module initialization routine and clear it if it is set.

Affected Silicon Revisions

A0							
X							

35. Module: ADC

When the ADC module is configured to start conversion on an external interrupt (SSRC<2:0> = 001), the start of conversion always occurs on a rising edge detected at the INT0 pin, even when the INT0 pin has been configured to generate an interrupt on a falling edge (INT0EP = 0).

Work around

Generate ADC conversion triggers on the rising edge of the INT0 signal.

Alternatively, use external circuitry to invert the signal appearing at the INT0 pin, so that a falling edge of the input signal is detected as a rising edge by the INT0 pin.

Affected Silicon Revisions

A0							
X							

36. Module: JTAG

Pin 100 on 100-pin packages and pin A1 on 121-pin packages do not respond to boundary scan commands.

Work around

None.

Affected Silicon Revisions

A0							
X							

37. Module: DMA

If the DMA module is suspended by setting the DMA Suspend bit (SUSPEND) in the DMA Controller Control register (DMACON), the DMA Module Busy Bit (DMABUSY) in the DMACON register may continue to show a Busy status, when the DMA module completes transaction.

Work around

Use the Channel Busy bit (CHBUSY) in the DMA Channel Control Register (DCHxCON) to check the status of the DMA channel.

Affected Silicon Revisions

A0							
X							

38. Module: Voltage Regulator

Device may not exit BOR state if BOR event occurs.

Work arounds

Work around 1:

VDD must remain within the published specification (see parameter DC10 of the device data sheet).

Work around 2:

Reset device by providing POR condition.

Affected Silicon Revisions

A0							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS61156**F**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

APPENDIX A: REVISION HISTORY

Rev A Document (8/2009)

Initial release of this document; issued for revision A0 silicon.

Includes silicon issues 1 (I^2C™), 2 (Ethernet), 3 (ADC), 4 (Parallel Master Port), 5 (Output Compare), 6 (SPI) and 7 (UART).

Rev B Document (11/2009)

Added silicon issues 8 (USB), 9-10 (Output Compare), 11 (DMA), 12 (Timers), 13 (SPI), 14-17 (CAN), 18 (Output Compare), 19 (SPI), 20-21 (USB), 22 (WDT), 23 (Oscillator) and 24 (Oscillator).

Rev C Document (9/2010)

The document title was changed to PIC32MX575/675/ /695/775/795 Family Silicon Errata and Data Sheet Clarification.

Added devices to Table 1: Silicon DEVREV Values.

Modified silicon issue 1 (I^2C™).

Added silicon issues 25 (SPI), 26 (PORTS), 27-28 (SPI), 29 (CAN), 30-31 (UART), 32 (JTAG), 33 (UART) and 34 (UART), and added data sheet clarification issue 1 (Revision History).

Rev D Document (11/2010)

Removed data sheet clarification 1.

Added silicon issues 35 (ADC), 36 (JTAG) and 37 (DMA).

Rev E Document (12/2010)

Added silicon issue 38 (Voltage Regulator).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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