PIC24FJ256GA110 Family Data Sheet Errata

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39905**B**), the following clarifications and corrections should be noted. Any silicon issues related to the PIC24FJ256GA110 family will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

1. Module: Electrical Characteristics

The following tables are changed with the new or modified values shown in bold text:

- Table 27-4:
  DC Characteristics: Operating Current (I_{DD})
- Table 27-5:
  DC Characteristics: Idle Current (i_{IDLE})
- Table 27-6:
  DC Characteristics: Power-Down Current (I_{PD})

TABLE 27-4: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
Operating Current (IDD)(2)						
DC20	0.83	1.2	mA	-40°C	2.0V(3)	1 MIPS
DC20a	0.83	1.2	mA	+25°C		
DC20b	0.83	1.2	mA	+85°C		
DC20d	1.1	**1.7**	mA	-40°C	3.3V(4)	
DC20e	1.1	**1.7**	mA	+25°C		
DC20f	1.1	**1.7**	mA	+85°C		
DC23	3.3	**4.5**	mA	-40°C	2.0V(3)	4 MIPS
DC23a	3.3	**4.5**	mA	+25°C		
DC23b	3.3	**4.6**	mA	+85°C		
DC23d	4.3	6.0	mA	-40°C	3.3V(4)	
DC23e	4.3	6.0	mA	+25°C		
DC23f	4.3	6.0	mA	+85°C		
DC24	18.2	24.0	mA	-40°C	2.5V(3)	16 MIPS
DC24a	18.2	24.0	mA	+25°C		
DC24b	18.2	24.0	mA	+85°C		
DC24d	18.2	24.0	mA	-40°C	3.3V(4)	
DC24e	18.2	24.0	mA	+25°C		
DC24f	18.2	24.0	mA	+85°C		
DC31	15.0	**35.0**	µA	-40°C	2.0V(3)	LPRC (31 kHz)
DC31a	15.0	**35.0**	µA	+25°C		
DC31b	20.0	**50.0**	µA	+85°C		
DC31d	57.0	75.0	µA	-40°C	3.3V(4)	
DC31e	57.0	75.0	µA	+25°C		
DC31f	95.0	124.0	µA	+85°C		

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows: OSCI driven with external square wave from rail to rail. All I/O pins are configured as inputs and pulled to VDD. $\overline{MCLR}$ = VDD; WDT and FSCM are disabled. CPU, SRAM, program memory and data memory are operational. No peripheral modules are operating and all of the Peripheral Module Disable (PMD) bits are set.

3: On-chip voltage regulator disabled (ENVREG tied to VSS).

4: On-chip voltage regulator enabled (ENVREG tied to VDD), Low-Voltage Detect (LVD) and Brown-out Detect (BOD) are enabled.

TABLE 27-5: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
Idle Current (IIDLE)(2)						
DC40	220	**310**	µA	-40°C	2.0V(3)	1 MIPS
DC40a	220	**310**	µA	+25°C		
DC40b	220	**310**	µA	+85°C		
DC40d	300	390	µA	-40°C	3.3V(4)	
DC40e	300	390	µA	+25°C		
DC40f	320	420	µA	+85°C		
DC43	0.85	1.1	mA	-40°C	2.0V(3)	4 MIPS
DC43a	0.85	1.1	mA	+25°C		
DC43b	0.87	1.2	mA	+85°C		
DC43d	1.1	1.4	mA	-40°C	3.3V(4)	
DC43e	1.1	1.4	mA	+25°C		
DC43f	1.1	1.4	mA	+85°C		
DC47	4.4	5.6	mA	-40°C	2.5V(3)	16 MIPS
DC47a	4.4	5.6	mA	+25°C		
DC47b	4.4	5.6	mA	+85°C		
DC47c	4.4	5.6	mA	-40°C	3.3V(4)	
DC47d	4.4	5.6	mA	+25°C		
DC47e	4.4	5.6	mA	+85°C		
DC50	1.1	1.4	mA	-40°C	2.0V(3)	FRC (4 MIPS)
DC50a	1.1	1.4	mA	+25°C		
DC50b	1.1	1.4	mA	+85°C		
DC50d	1.4	1.8	mA	-40°C	3.3V(4)	
DC50e	1.4	1.8	mA	+25°C		
DC50f	1.4	1.8	mA	+85°C		
DC51	4.3	6.0	µA	-40°C	2.0V(3)	LPRC (31 kHz)
DC51a	4.5	6.0	µA	+25°C		
DC51b	**10.0**	25	µA	+85°C		
DC51d	**44.0**	**60.0**	µA	-40°C	3.3V(4)	
DC51e	44.0	60.0	µA	+25°C		
DC51f	70.0	**115.0**	µA	+85°C		

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IIDLE current is measured with core off, OSCI driven with external square wave from rail to rail. All I/O pins are configured as inputs and pulled to VDD. $\overline{MCLR}$ = VDD; WDT and FSCM are disabled. No peripheral modules are operating and all of the Peripheral Module Disable (PMD) bits are set.

3: On-chip voltage regulator disabled (ENVREG tied to VSS).

4: On-chip voltage regulator enabled (ENVREG tied to VDD), Low-Voltage Detect (LVD) and Brown-out Detect (BOD) are enabled.

TABLE 27-6: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
Power-Down Current (I_{PD})(2)						
DC60	0.1	1.0	µA	-40°C	2.0V(3)	Base Power-Down Current(5)
DC60a	0.15	1.0	µA	+25°C		
DC60b	3.7	18.0	µA	+85°C		
DC60c	0.2	**1.4**	µA	-40°C	2.5V(3)	
DC60d	0.25	**1.4**	µA	+25°C		
DC60e	4.2	27.0	µA	+85°C		
DC60f	3.6	**10.0**	µA	-40°C	3.3V(4)	
DC60g	4.0	10.0	µA	+25°C		
DC60h	11.0	36.0	µA	+85°C		
DC61	1.75	3	µA	-40°C	2.0V(3)	Watchdog Timer Current: ΔI_{WDT}(5)
DC61a	1.75	3	µA	+25°C		
DC61b	1.75	3	µA	+85°C		
DC61c	2.4	4	µA	-40°C	2.5V(3)	
DC61d	2.4	4	µA	+25°C		
DC61e	2.4	4	µA	+85°C		
DC61f	2.8	5	µA	-40°C	3.3V(4)	
DC61g	2.8	5	µA	+25°C		
DC61h	2.8	5	µA	+85°C		
DC62	2.5	7.0	µA	-40°C	2.0V(3)	RTCC + Timer1 w/32 kHz Crystal: $\Delta RTCC + \Delta I_{TI32}$(5)
DC62a	2.5	7.0	µA	+25°C		
DC62b	3.0	7.0	µA	+85°C		
DC62c	2.8	7.0	µA	-40°C	2.5V(3)	
DC62d	3.0	7.0	µA	+25°C		
DC62e	3.0	7.0	µA	+85°C		
DC62f	3.5	10.0	µA	-40°C	3.3V(4)	
DC62g	3.5	10.0	µA	+25°C		
DC62h	4.0	10.0	µA	+85°C		

Note 1: Data in the Typical column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base I_{PD} is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled high. WDT, etc., are all switched off, and the Peripheral Module Disable (PMD) bits for all unused peripherals are set.

3: On-chip voltage regulator disabled (ENVREG tied to V_{SS}).

4: On-chip voltage regulator enabled (ENVREG tied to V_{DD}), Low-Voltage Detect (LVD) and Brown-out Detect (BOD) are enabled.

5: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

2. Module: Electrical Specifications

DC specification, BO10, for the device Brown-out Reset voltage (V_{BOR}), has been added to Table 27-3 of the device data sheet. It is shown in **bold** below (bold text from original table removed for clarity).

3. Module: Electrical Specifications

The DC specification for the Internal Reference Band Gap Voltage, V_{BG}, has been added to Table 27-10 of the device data sheet. It is shown in **bold** below (bold text from original table removed for clarity).

TABLE 27-3: DC CHARACTERISTICS: TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
Operating Voltage							
DC10	Supply Voltage						
	VDD		2.2	—	3.6	V	Regulator enabled
	VDD		VDDCORE	—	3.6	V	Regulator disabled
	VDDCORE		2.0	—	2.75	V	Regulator disabled
DC12	VDR	RAM Data Retention Voltage(2)	1.5	—	—	V	
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	—	VSS	—	V	
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.5	—	—	V/ms	0-3.3V in 0.1s 0-2.5V in 60 ms
BO10	**VBOR**	**Brown-out Reset Voltage**	**—**	**2.05**	**—**	**V**	

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This is the limit to which VDD can be lowered without losing RAM data.

TABLE 27-10: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param No.	Symbol	Characteristics	Min	Typ	Max	Units	Comments
	VRGOUT	Regulator Output Voltage	—	2.5	—	V	
	VBG	**Internal Band Gap Reference**	**—**	**1.2**	**—**	**V**	
	CEFC	External Filter Capacitor Value	4.7	10	—	µF	Series resistance < 3 Ohm recommended; < 5 Ohm required.
	TVREG		—	50	—	µs	ENVREG tied to VDD
	TPWRT		—	64	—	ms	ENVREG tied to VSS

4. Module: Pin Diagrams

In the 64-pin device pin diagram on page 2, the reference to SCK1 on pin 35 is deleted. The correct complete designation for this pin is “RPI45/INT0/CN72/RF6”.

The SCK1 function is available only through Peripheral Pin Select (PPS), and is not permanently multiplexed to any one pin on this device.

5. Module: Memory Organization (SFR Space)

In Table 3-5 of the device data sheet (Interrupt Controller Register Map), bits 4 and 3 of INTCON2 are incorrectly shown as unimplemented. These positions are actually implemented as INT4EP and INT3EP, respectively.

An amended partial version of the table with the correct footnote is shown in Table 3-5 (additions in **bold**).

6. Module: Memory Organization (SFR Space)

In Table 3-18 of the device data sheet (PORTG Register Map), the footnote references on the Bit 1 and Bit 0 columns are incorrect. These bits, and their corresponding I/O channels, are actually available on 80-pin devices.

An amended version of the table with the correct footnote is shown in Table 3-18 (additions and changes in **bold**).

TABLE 3-5: INTERRUPT CONTROLLER REGISTER MAP (PARTIAL REPRESENTATION)

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	—	—	—	—	—	—	—	—	—	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	**INT4EP**	**INT3EP**	INT2EP	INT1EP	INT0EP	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 3-18: PORTG REGISTER MAP

File Name	Addr	Bit 15(1)	Bit 14(1)	Bit 13(1)	Bit 12(1)	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1(2)	Bit 0(2)	All Resets
TRISG	02F0	TRISG15	TRISG14	TRISG13	TRISG12	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	TRISG3	TRISG2	TRISG1	TRISG0	F3CF
PORTG	02F2	RG15	RG14	RG13	RG12	—	—	RG9	RG8	RG7	RG6	—	—	RG3	RG2	RG1	RG0	xxxx
LATG	02F4	LATG15	LATG14	LATG13	LATG12	—	—	LATG9	LATG8	LATG7	LATG6	—	—	LATG3	LATG2	LATG1	LATG0	xxxx
ODCG	02F6	ODG15	ODG14	ODG13	ODG12	—	—	ODG9	ODG8	ODG7	ODG6	—	—	ODG3	ODG2	ODG1	ODG0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Reset values shown are for 100-pin devices.

Note 1: Bits unimplemented in 64-pin and 80-pin devices; read as '0'.

2: **Bits unimplemented in 64-pin devices; read as '0'.**

7. Module: Interrupt Controller

In Register 6-4 (INTCON2), bits 4 and 3 of INTCON2, currently shown as unimplemented, are in fact implemented as INT4EP and INT3EP, respectively.

An amended partial version of this register is shown below (changes in **bold**).

8. Module: Timer2/3 and Timer4/5

In the bulleted list in the 3rd paragraph of **Section 11.0 "Timer2/3 and Timer4/5"**, it is stated that the ADC event trigger is only associated with Timer4/5. In fact, the trigger is only associated with Timer2/3. This is correctly noted in all other occurrences in the chapter.

REGISTER 6-4: INTCON2: INTERRUPT CONTROL REGISTER 2 (PARTIAL REPRESENTATION)

R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	**R/W-0**	**R/W-0**	R/W-0	R/W-0	R/W-0
—	—	—	**INT4EP**	**INT3EP**	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 13-**5** Unimplemented: Read as '0'

bit 4 **INT4EP: External Interrupt 4 Edge Detect Polarity Select bit**
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 3 **INT3EP: External Interrupt 3 Edge Detect Polarity Select bit**
1 = Interrupt on negative edge
0 = Interrupt on positive edge

9. Module: 10-Bit High-Speed A/D Converter

In Register 20-1 (AD1CON1), the descriptions provided for the various combinations of the SSRC<2:0> bits (ADCON1<7:5>) are incorrect. Specifically, while the number and type of trigger sources are reported correctly, several are associated with the wrong bit combinations.

The correct order of trigger sources is listed below (changes in **bold**).

10. Module: Special Features

In Register 24-3 (CW3), the explanatory text with Configuration bits, WPFP<8:0> (CW3<8:0>), is changed to agree with the text of **Section 24.4.2 "Code Segment Protection"**. The new register text is as follows (change in **bold**):

"Designates the **512-byte** program code page that is the boundary of the protected code segment, starting with Page 0 at the bottom of program memory."

REGISTER 20-1: AD1CON1: A/D CONTROL REGISTER 1 (PARTIAL REPRESENTATION)

bit 7-5 SSRC2:SSRC0: Conversion Trigger Source Select bits

111 = Internal counter ends sampling and starts conversion (auto-convert)
110 = **CTMU event ends sampling and starts conversion**
101 = Reserved
100 = **Timer5 compare ends sampling and starts conversion**
011 = **Reserved**
010 = Timer3 compare ends sampling and starts conversion
001 = Active transition on INT0 pin ends sampling and starts conversion
000 = Clearing SAMP bit ends sampling and starts conversion

REVISION HISTORY

Rev A Document (7/2008)
Initial release of this data sheet errata. Includes Data Sheet Clarification 1 (Electrical Characteristics).

Rev B Document (1/2009)
Added Data Sheet Clarifications 2-3 (Electrical Characteristics), 4 (Pin Diagrams), 5-6 (Memory Organization), 7 (Interrupt Controller), 8 (Timer2/3 and Timer4/5), 9 (10-Bit High-Speed A/D Converter) and 10 (Special Features).

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