# dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 Family Silicon Errata and Data Sheet Clarification

The dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 family devices that you have received conform functionally to the current Device Data Sheet (DS70591**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A0**).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICkit 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

**Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 silicon revisions are shown in Table 1.

**TABLE 1: SILICON DEVREV VALUES**

| Part Number | Device ID(1) | Revision ID for Silicon Revision(2) |
|---|---|---|
| | | A0 |
| dsPIC33FJ32GS406 | 0x4000 | 0x3000 |
| dsPIC33FJ32GS606 | 0x4002 | |
| dsPIC33FJ32GS608 | 0x4004 | |
| dsPIC33FJ32GS610 | 0x4006 | |
| dsPIC33FJ64GS406 | 0x4001 | |
| dsPIC33FJ64GS606 | 0x4003 | |
| dsPIC33FJ64GS608 | 0x4005 | |
| dsPIC33FJ64GS610 | 0x4007 | |

**Note 1:** The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

**2:** Refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for detailed information on Device and Revision IDs for your specific device.

**TABLE 2: SILICON ISSUE SUMMARY**

| Module | Feature | Item Number | Issue Summary | Affected Revisions(1) |
|---|---|---|---|---|
| | | | | A0 |
| ECAN | WAKIF bit | 1. | The WAKIF bit in the CxINTF register cannot be cleared by software instruction after the device is interrupted from Sleep due to activity on the CAN bus. | X |
| Reserved | — | 2. | — | — |
| SPI | $\overline{SS1}$ Pin | 3. | The $\overline{SS1}$ pin function does not work. | X |
| JTAG | Boundary Scan | 4. | The boundary scan cells for the RD3 and RD13 pins are swapped. | X |
| PWM | Secondary Master Time Base Synchronization | 5. | The external time base synchronization output pin, SYNCO2, does not work. | X |
| Interrupts | Exit from Doze Mode on Interrupt | 6. | An interrupt with a priority level lower than the CPU priority level will trigger the dsPIC® DSC device to exit the Doze mode, but an interrupt request will not be generated. | X |
| ADC | Current Consumption in Sleep Mode | 7. | If the ADC module is in an enabled state when the device enters Sleep mode, the power-down current ($I_{PD}$) of the device may exceed the device data sheet specifications. | X |
| PWM | External Period Reset Mode (XPRES) | 8. | When using the External Period Reset mode, PWM period will get reset immediately if the Reset signal is active at the end of the PWM ON time. | X |
| High Speed PWM | PWM Module Enable | 9. | A glitch may be observed on the PWM pins when the PWM module is enabled after assignment of pin ownership to the PWM module. | X |
| ECAN | Error Interrupt Flag | 10. | The ERRIF status bit does not get set when a CAN error condition occurs. | X |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

## Silicon Errata Issues

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. The shaded column in the "Affected Silicon Revisions" table included in each issue indicates that the issue applies to the most current revision of silicon (**A0**).

### 1. Module: ECAN

The WAKIF bit in the CxINTF register cannot be cleared by software instruction after the device is interrupted from Sleep due to activity on the CAN bus.

When the device wakes up from Sleep due to CAN bus activity, the ECAN module is placed in operational mode. The ECAN event interrupt occurs due to the WAKIF flag. Trying to clear the flag in the Interrupt Service Routine (ISR) may not clear the flag. The WAKIF bit being set will not cause repetitive Interrupt Service Routine execution.

**Work around**

Although the WAKIF bit does not clear, the device Sleep and ECAN Wake function continue to work as expected. If the ECAN event is enabled, the CPU will enter the Interrupt Service Routine due to the WAKIF flag getting set. The application can maintain a secondary flag, which tracks the device Sleep and Wake events.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 2. Module: Reserved

The issue in the previous version of the document has been removed.

### 3. Module: SPI

The $\overline{ASS1}$ pin is provided as an alternative pin for the slave select function of the SPI1 module. However, the alternate slave select function ($\overline{ASS1}$) on this pin does not work. All other functions multiplexed on the same pin work as expected.

**Work around**

Use the $\overline{SS1}$ pin for the slave select function.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 4. Module: JTAG

The boundary scan cells for the RD3 and RD13 pins are swapped. When running the boundary scan test, an input to the RD3 pin excites the RD13 pin, and vice versa.

This erratum does not affect any other functionality on the RD3 and RD13 pins.

**Work around**

None.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 5. Module: PWM

The SYNCO2 pin can be used to transmit synchronization pulses to generate an identical PWM time base on another device. However, the SYNCO2 function does not work as expected. As a result of this erratum, the secondary master time base cannot be used for synchronizing a slave device.

All other functions multiplexed on the same pin work as expected.

**Work around**

A spare PWMxL/PWMxH pin can be used as the synchronization source output instead of the SYNCO2 pin using the following procedure:

1. Configure the spare PWMxL/PWMxH pin to operate on the same time base, period, and phase as the synchronizing (or reference) PWM channel.
2. Set up the duty cycle for the spare PWMxL/PWMxH pin to the desired pulse width for the synchronization signal (typically 100 ns at the highest PWM resolution).
3. Connect the spare PWMxL/PWMxH pin to the synchronization input of the slave PWM generator.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 6. Module: Interrupts

When the dsPIC® DSC device is operating in Doze mode, any interrupt should trigger the device to exit Doze mode and generate an interrupt request (IRQ) regardless of the interrupt priority level. However, if the interrupt priority level is lower than the CPU priority level, the interrupt request will not be generated. As a result, the CPU will not detect that it has exited Doze mode.

**Work around**

Any interrupt that is expected to wake the CPU from Doze mode must be configured for an interrupt priority level higher than the CPU priority level. This work around can be implemented in software right before the device enters Doze mode and reverted to the desired priority level after it wakes up from Doze mode.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 7. Module: ADC

If the ADC module is in an enabled state when the device enters Sleep mode as a result of executing a `PWRSAV #0` instruction, the device power-down current ($I_{PD}$) may exceed the specifications listed in the device data sheet. This may happen even if the ADC module is disabled by clearing the ADON bit prior to entering Sleep mode.

**Work around**

In order to remain within the $I_{PD}$ specifications listed in the device data sheet, the user software must completely disable the ADC module by setting the ADC Module Disable bit in the corresponding Peripheral Module Disable register (PMDx), prior to executing a `PWRSAV #0` instruction.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 8. Module: PWM

The External Period Reset mode is used to reset the PWM period when the selected reset signal is asserted during the OFF time of the PWM. If the reset signal is asserted during the PWM ON time, then the reset signal must be ignored.

However, on the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 devices, the reset signal is not ignored at the end of the PWM ON time. Therefore, the PWM period will be reset immediately after the end of the PWM ON time.

**Work around**

Ensure that the External Period Reset signal is asserted during the PWM OFF time.

**Affected Silicon Revisions**

| A0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 9. Module: High Speed PWM

The PENH and PENL bits in the IOCONx register are used to assign ownership of the pins to either the PWM module or the GPIO module. The correct procedure to configure the PWM module is to first assign pin ownership to the PWM module and then enabling it using the PTEN bit in the PTCON register.

If the PWM module is enabled using the above sequence, then a glitch may be observed on the PWM pins before actual switching of the PWM outputs begins. This glitch may cause momentary turn ON of power MOSFETs that are driven by the PWM pins and may cause damage to the application hardware.

**Work around**

Follow the given sequence to avoid any glitches from appearing on the PWM outputs at the time of enabling.

1. Configure the respective PWM pins to digital inputs using the TRISx registers. This step will put the PWM pins in a high-impedance state. The PWM outputs must be maintained in a safe state by using pull-up or pull-down resistors.
2. Assign pin ownership to the GPIO module by configuring IOCONx<PENH> = 0 and IOCONx<PENL> = 0.
3. Specify the PWM override state to the desired safe state for the PWM pins using the OVRDAT<1:0> bit-field in the IOCONx register.
4. Override the PWM outputs by setting IOCONx<OVRENH> = 1 and IOCONx<OVRENL> = 1.
5. Enable the PWM module by setting PTCON<PTEN> = 1.
6. Remove the PWM Overrides by making IOCONx<OVRENH> = 0 and IOCONx<OVRENL> = 0.
7. Assign pin ownership to the PWM module by setting IOCONx<PENH> = 1 and IOCONx<PENL> = 1.

The code in Example 1 illustrates the use of this work around.

**EXAMPLE 1: CONFIGURE PWM MODULE TO PREVENT GLITCHES ON PWM1H AND PWM1L PINS AT THE TIME OF ENABLING**

```
TRISAbits.TRISA4 = 1;   // Configure PWM1H/RA4 as digital input
                        // Ensure output is in safe state using pull-up or
                        // pull-down resistors
TRISAbits.TRISA3 = 1;   // Configure PWM1L/RA3 as digital input
                        // Ensure output is in safe state using pull-up or
                        // pull-down resistors

IOCON1bits.PENH = 0;    // Assign pin ownership of PWM1H/RA4 to GPIO module
IOCON1bits.PENL = 0;    // Assign pin ownership of PWM1L/RA3 to GPIO module

IOCON1bits.OVRDAT = 0;  // Configure override state of the PWM outputs to
                        // desired safe state.

IOCON1bits.OVRENH = 1;  // Override PWM1H output
IOCON1bits.OVRENL = 1;  // Override PWM1L output

PTCONbits.PTEN = 1;     // Enable PWM module

IOCON1bits.OVRENH = 0;  // Remove override for PWM1H output
IOCON1bits.OVRENL = 0;  // Remove override for PWM1L output

IOCON1bits.PENH = 1;    // Assign pin ownership of PWM1H/RA4 to PWM module
IOCON1bits.PENL = 1;    // Assign pin ownership of PWM1L/RA3 to PWM module
```

**Affected Silicon Revisions**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **A0** | | | | | | | |
| X | | | | | | | |

## 10. Module: ECAN

The ERRIF status flag (CiINTF<5>) does not get set when a CAN error condition occurs. However, the corresponding CiIF interrupt flag will get set on a CAN error condition, and an interrupt will be correctly generated if enabled.

**Work around**

Do not inspect the state of the ERRIF bit to determine if a CAN error interrupt has occurred. Instead, inspect the individual error condition status flags TXBO, TXBP, RXBP, TXWAR, RXWAR and EWARN (CiINTF<13:8>).

**Affected Silicon Revisions**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **A0** | | | | | | | |
| X | | | | | | | |

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70591**C**):

| **Note:** | Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity. |
|---|---|

### 1. Module: DC Characteristics: I/O Pin Input Specifications

The maximum value for parameter DI19 ($V_{IL}$ specifications for SDAx and SCLx pins) was stated incorrectly in Table 31-9 of the current device data sheet. Also, parameters DI28 and DI29 ($V_{IH}$ specifications for SDAx and SCLx pins) were not stated. The correct values are shown in bold type in Table 3.

**TABLE 3: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ | Max | Units | Conditions |
| | $V_{IL}$ | Input Low Voltage | | | | | |
| DI18 | | **SDAx, SCLx** | $V_{SS}$ | — | 0.3 $V_{DD}$ | V | SMBus disabled |
| DI19 | | **SDAx, SCLx** | $V_{SS}$ | — | **0.8** | V | SMBus enabled |
| | $V_{IH}$ | Input High Voltage | | | | | |
| **DI28** | | **SDAx, SCLx** | **0.7 $V_{DD}$** | **—** | **5.5** | **V** | **SMBus disabled** |
| **DI29** | | **SDAx, SCLx** | **2.1** | **—** | **5.5** | **V** | **SMBus enabled** |

# APPENDIX A: REVISION HISTORY

Rev A Document (10/2009)

Initial release of this document; issued for revision A0. Includes silicon issues 1 (ECAN), 2 (SPI), 3 (SPI) 4 (JTAG), 5 (PWM) and 6 (Interrupts).

Rev B Document (6/2010)

Removed silicon issue 2 (SPI) and marked its location as reserved.

Updated the work around in silicon issue 5 (PWM).

Added silicon issues 7 (ADC), 8 (PWM) and 9 (High Speed PWM) and data sheet clarification 1 (DC Characteristics: I/O Pin Input Specifications).

Rev C Document (11/2010)

Updated the Device IDs in Table 1 for the following devices:

- dsPIC33FJ32GS606
- dsPIC33FJ32GS608
- dsPIC33FJ32GS610
- dsPIC33FJ64GS406
- dsPIC33FJ64GS606
- dsPIC33FJ64GS608

Added silicon issue 10 (ECAN).

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