



# MICROCHIP PIC18F6310/6410/8310/8410

## PIC18F6310/6410/8310/8410 Rev. C1 Silicon Errata

The PIC18F6310/6410/8310/8410 Rev. C1 parts you have received conform functionally to the Device Data Sheet (DS39635B), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F6310/6410/8310/8410 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

All of the issues listed here will be addressed in future revisions of the PIC18F6310/6410/8310/8410 silicon.

The following silicon errata apply only to PIC18F6310/6410/8310/8410 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F6310	0000 1011 111	0 0110
PIC18F6410	0000 0110 111	0 0110
PIC18F8310	0000 1011 110	0 0110
PIC18F8410	0000 0110 110	0 0110

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

### 1. Module: Master Synchronous Serial Port (MSSP)

Configured in SPI slave mode, the MSSP will generate a write collision if SSPBUF is updated and the previous SSPBUF contents have not been transferred to the shift register.

Reinitializing the MSSP, by clearing and setting the SSPEN bit (SSPCON1<5>) prior to rewriting SSPBUF, will *not* prevent the error condition.

#### Work around

Prior to updating the SSPBUF register with a new value, verify that the previous contents have been transferred by reading the BF bit (SSPSTAT<0>). If the previous byte has *not* been transferred:

- Update SSPBUF
- If necessary, clear the WCOL bit (SSPCON1<7>)

#### Date Codes that pertain to this issue:

All engineering and production devices.

### 2. Module: MSSP – Serial Peripheral Interface (SPI)

In SPI mode, the Buffer Full flag (BF bit in the SSPSTAT register), the Write Collision Detect bit (WCOL in SSPCON1) and the Receive Overflow Indicator bit (SSPOV in SSPCON1) are not reset upon disabling the SPI module (by clearing the SSPEN bit in the SSPCON1 register).

For example, if SSPBUF is full (BF bit is set) and the MSSP module is disabled and re-enabled, the BF bit will remain set. In SPI Slave mode, a subsequent write to SSPBUF will result in a write collision. Also, if a new byte is received, a receive overflow will occur.

#### Work around

If if the buffer is full, before disabling the MSSP module, ensure that:

- SSPBUF is read (thus clearing the BF flag)
- WCOL is clear

If the module is configured in SPI Slave mode, ensure that the SSPOV bit is clear before disabling the module.

#### Date Codes that pertain to this issue:

All engineering and production devices.

### 3. Module: MSSP – I<sup>2</sup>C™

In the 10-Bit Slave mode, the I<sup>2</sup>C™ mode does not work correctly.

#### Work around

None.

#### Date Codes that pertain to this issue:

All engineering and production devices.

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## 4. Module: MSSP – I<sup>2</sup>C

When configured for I<sup>2</sup>C™ slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer Register (SSPBUF) is not read within a window after the SSPIF interrupt (PIR1<3>) has occurred.

### **Work around**

The issue can be resolved in either of these ways:

- Prior to the I<sup>2</sup>C slave reception, enable the clock stretching feature.

This is done by setting the SEN bit (SSPCON2<0>).

- Each time the SSPIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

### **Date Codes that pertain to this issue:**

All engineering and production devices.

## REVISION HISTORY

### Rev A Document (11/2009)

Initial release of this document. Includes silicon issues 1 (MSSP), 2 (MSSP – SPI) and 3-4 (MSSP – I<sup>2</sup>C).

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